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https://doi.org/10.1002/jsid.2058

5009-ppi, 10000-cd/m^2, OLED/OS/Si Structure Display with Built-in CPU and Display Driver

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Abstract

This study developed a 5009-ppi, 10000-cd/m^2 organic light-emitting diode display featuring c-axis-aligned crystalline oxide semiconductor field-effect transistors (FETs) monolithically stacked over silicon (Si) FETs. It was demonstrated that a built-in central processing unit (Cortex-M0) enables amplifier offset compensation and that functional circuits beyond a display driver can operate on a Si substrate.

Author Keywords

CAAC-OS; Si; microdisplay; OLED; high definition; high luminance

1. Introduction

The market for augmented reality (AR) and virtual reality (VR) microdisplays is continuously expanding. However, some head-mounted AR and VR displays have been reported to cause user discomfort due to the screen door effect and motion blur [1,2]. To address this problem and achieve more realistic images, high-definition, high-aperture-ratio pixels and a high frame rate are required. Consequently, organic light-emitting diode (OLED) microdisplays must achieve higher definition [3,4]. In high-definition pixels utilizing OLED-on-silicon (OLEDoS) technology, the drive transistor must operate within a video voltage range in which a current on the order of nanoamperes or less flows. However, in OLEDoS technology, all pixel transistors are silicon (Si) field-effect transistors (FETs), which have high current supply capability, making it difficult to control ultralow currents [5].

A previously reported high-definition display achieved a definition exceeding 5000 ppi using a pixel circuit incorporating a c-axis-aligned crystalline oxide semiconductor (CAAC-OS) FET [6,7]. This CAAC-OS FET can be monolithically stacked over a Si FET circuit [8], where a Si complementary metal–oxide–semiconductor (CMOS) circuit enables various on-chip functions and enhances the layout flexibility of the display driver [9]. Thus, in a display with an OLED/OS/Si structure, CAAC-OS FETs enable the formation of fine pixels with a current on the order of nanoamperes or less. Furthermore, arrangement of multiple drivers in the Si layer allows for controlling high-definition pixels. Therefore, displays with an OLED/OS/Si structure are suitable for high-definition microdisplays. Like OS FETs formed by a low-temperature polysilicon and oxide process [10], which are used in a glass substrate process, CAAC-OS FETs have a low leakage current and thus contribute to a reduction in power consumption.

The development of monolithically stacked CAAC-OS FETs over Si FET circuits offers new possibilities for enhancing the functionality of AR and VR displays. Specifically, integrating Si FETs below the display allows for the incorporation of functional circuits other than the display driver without widening the bezel. These built-in functional circuits enhance performance and achieve multifunctionality. This study proposes a high-definition, high-luminance OLED microdisplay and presents an example of functional circuit integration, where amplifier offset compensation, which is necessary for image quality correction, is performed using a built-in central processing unit (CPU; Cortex-M0).

2. OLED/OS/Si Monolithic Structure

Figure 1 presents a cross-sectional image of the structure formed by the OS/Si stacking process. CAAC-OS FETs, formed by the CAAC-OS 130-nm process, are monolithically stacked over Si FETs and wiring formed by the Si CMOS 55-nm high-voltage (HV) process. Thus, in the OS/Si structure, a display driver and other functional circuits can be integrated in the Si layer below the pixel circuit formed in the OS layer.

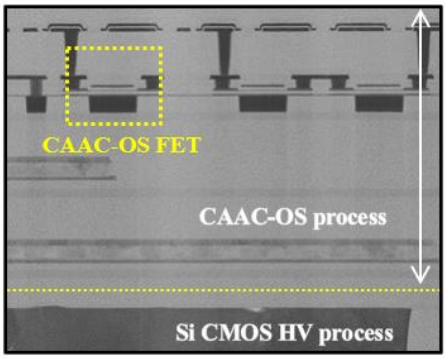

Figure 1. Cross-sectional scanning transmission electron microscopy image of the structure formed by the OS/Si monolithic stacking process.

Figure 2 presents a schematic view of the prototype display, where multiple source drivers are arranged to achieve higher definition. The Si layer incorporates not only source drivers but also scan drivers and driver controllers, eliminating the need for a pixel control circuit outside the pixel array.

To evaluate the feasibility of functionality enhancement, a CPU (Cortex-M0) is integrated into the Si layer as a functional circuit beyond the display driver. An amplifier output signal line from

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the display driver is connected to the input terminal of the analog-to-digital converter (ADC) of the CPU, enabling processing necessary for amplifier offset compensation.

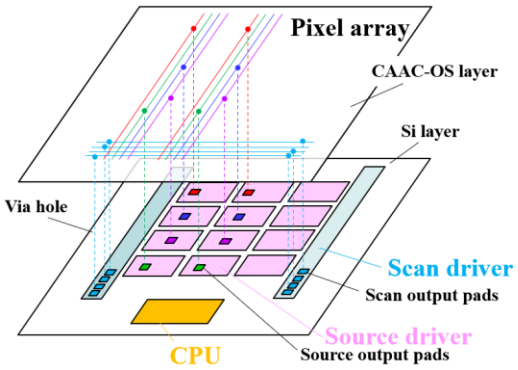

Figure 2. Schematic view of prototype display.

3. Structure of Prototype OLED/OS/Si Display

Table 1 presents the specifications of the prototype display.

Table 1. Display specifications

Screen diagonal	1.02 inch
Resolution	3600 × 3 (RGB) × 3600
Pixel size	5.07 μm × 5.07 μm
Pixel density	5009 ppi
Structure	OLED/OS/Si
Coloring method	Side-by-side with photolithography
Emission type	Top emission
Si CMOS process	55-nm HV Logic: 1.2 V, analog: 6.0 V
CAAC-OS process	130 nm
Refresh rate	90 Hz
Aperture ratio	38.9%
Source and scan drivers	Integrated

The display circuits are described below, beginning with Si circuits.

In the Si display driver below the CAAC-OS layer, two Si driver blocks with the same circuit layout are arranged point-symmetrically in a plan view (Figure 3). Thus, the two Si driver blocks are independently controlled. Each Si driver block consists of an input/output interface, a low-voltage differential signaling (LVDS) receiver (3 clock lanes, 30 data lanes), an inter-integrated circuit (I^2C) module, a controller, six source drivers, and a scan driver. The controller manages the timing of driver operations and the distribution of video data. The I^2C module adjusts the internal logic parameters to control the logic operation and signal timing of the Si driver.

The source lines connected to four adjacent pixels receive video potentials from the respective source drivers. The amplifier and the pass transistor logic (PTL) can be positioned to match a maximum four-pixel pitch, allowing for higher definition while reducing layout constraints. Two 3600-stage scan drivers, positioned on the left and right sides, generate scan signals. For gate lines requiring high-speed signal transmission, selection signals are supplied from both scan drivers. The control signal line of the pixel is connected to the output signal line of the driver in the lower layer through a via.

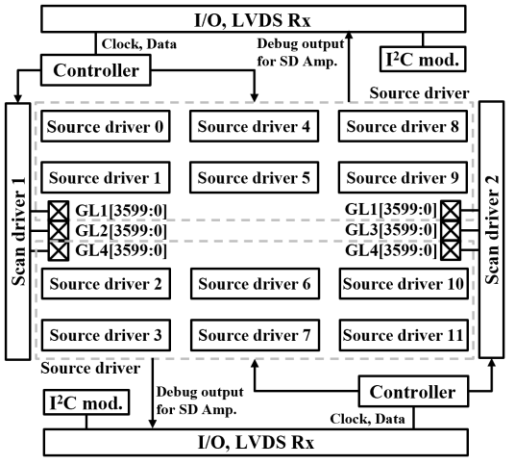

Figure 3. Circuit block diagram of Si display driver. I/O: input/output interface, LVDS Rx: low-voltage differential signaling receiver, SD: source driver, GL: gate line, SL: source line.

As illustrated in Figure 4, a CPU is integrated to perform part of the amplifier offset compensation, enabling evaluation of the feasibility of functionality expansion. In amplifier offset compensation, the source driver amplifier output is obtained, the average value of the amplifier output is calculated, and the input voltage is adjusted using the deviation from the average as compensation data. The CPU obtains the source driver amplifier output and transmits it to an external drive unit, which then employs the obtained data to generate the compensation data.

The amplifier output signal line of the source driver is connected to the input terminal of the ADC of the CPU. In addition, the amplifier output node of the source driver is connected to a debug output line through an analog switch. As a result, the output potentials of all amplifiers can be read using an I^2C parameter. The ADC converts the output potential of the amplifier into digital data, enabling the retrieval of all amplifier output data by reading the digital data.

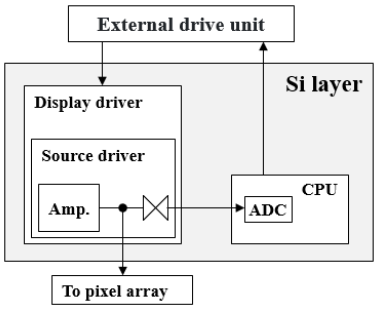

Figure 4. Circuit block diagram of the prototype display with a built-in CPU.

Next, the pixel circuit is described. Figure 5(A) presents a circuit diagram of a subpixel formed in the OS layer. A pixel, which is composed of three subpixels, has a size of 5.07 µm × 5.07 µm and thus requires small transistors. Accordingly, submicron-sized CAAC-OS FETs are employed. The threshold voltage of drive transistor M2 is compensated using a back-gate bias [11]. Figure 5(B) presents the timing chart for the pixel. The pixel circuit is controlled such that the threshold voltage is compensated, the video data are written, and a light-emitting device is turned on and then off in one frame period. The compensation data for the threshold voltage are stored in capacitor C2 on the back-gate side of drive transistor M2. To achieve a 10000-cd/m^2 display, a tandem OLED device is generally preferred for its reliability. Although a tandem OLED device requires a higher voltage than a single OLED device, this does not affect the operation of drive transistor M2, which is a CAAC-OS FET, as it exhibits a high breakdown voltage.

Light emission and non-light emission are controlled by switching transistor M5. This transistor requires a gate potential above 6 V for high-luminance light emission; however, the output signal from the scan driver, which is composed of Si FETs, is 6 V/0 V. A gate potential sufficiently high to turn on transistor M5 can be achieved by using bootstrap capacitor (C3). This pixel structure reduces the maximum voltage required for Si FETs, enabling the use of technology suitable for high-speed operation.

Figure 6 displays the characteristics of the CAAC-OS FET (*W*/*L* = 130 nm/550 nm) monolithically stacked over the Si CMOS circuit. Figure 6(A) reveals that the CAAC-OS FET exhibits normally-off characteristics and a sufficiently low off-state current that is below the lower measurement limit (1×10^{-12} A). Furthermore, Figure 6(B) demonstrates that the CAAC-OS FET exhibits favorable saturation in the range where a nanoampere-order current flows.

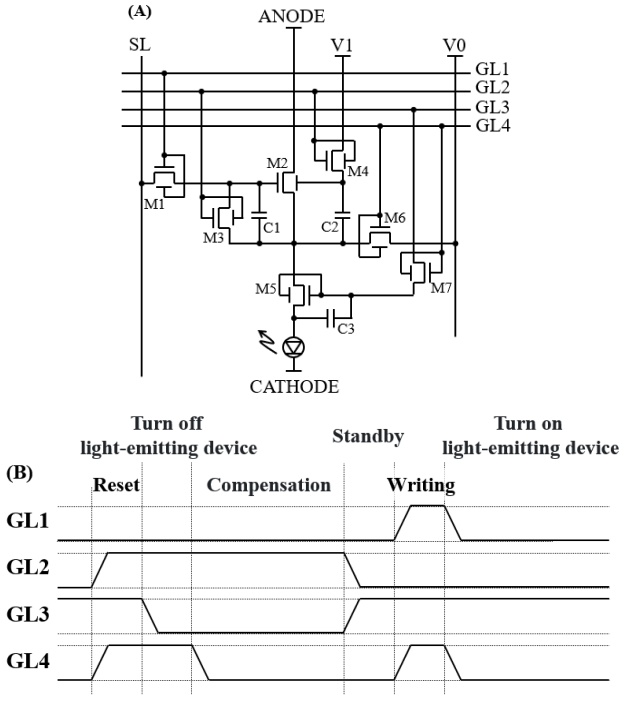

Figure 5. (A) Pixel circuit consisting of seven CAAC-OS FETs and three capacitors. (B) Timing chart.

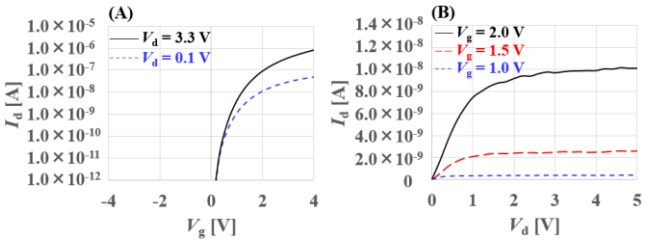

Figure 6. Characteristics of CAAC-OS FET: (A) I_d vs. V_g (V_g = V_{bg}), (B) I_d vs. V_d (V_{bg} = 0 V).

4. Measurement Results of OLED/OS/Si Display

The fabricated OLED/OS/Si display, built to the specifications presented in Table 1, exhibits a monolithically stacked structure. This includes the Si driver, formed by the Si CMOS 55-nm HV process, the OS pixel circuit, formed by the CAAC-OS 130-nm process, and the OLEDs, formed by a side-by-side coloring method with photolithography (a metal maskless lithography (MML) process [12]). The MML process increases the aperture ratio, which reduces the screen door effect. Figure 7 presents a photograph of an image displayed on the prototype display, which has a display region of 18.25 mm × 18.25 mm. It was confirmed that the 5009-ppi OLED/OS/Si display can display images at 90 Hz and achieve a luminance of up to 10000 cd/m^2.

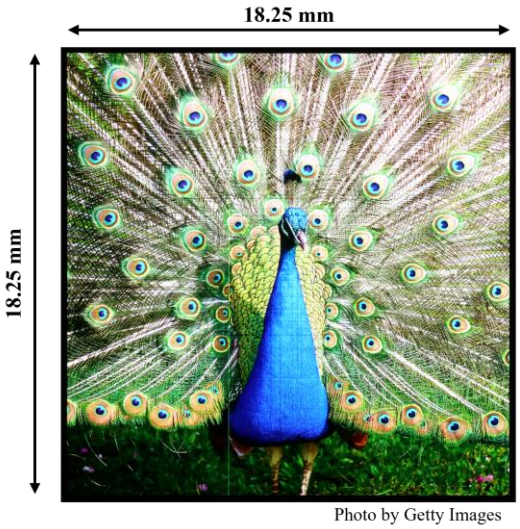

Figure 7. Photograph of image displayed on prototype display.

Next, to examine the multifunctional circuit fabricated on the same substrate as the display driver, amplifier offset compensation using the built-in CPU was verified. First, the CPU measured the amplifier output, and the external drive unit utilized these data to obtain the amplifier offset compensation data. It was investigated whether variations in amplifier output could be reduced using the compensation data. In the verification using standard deviation as an index of variation, the standard deviation was 13.68 mV before offset compensation and 3.22 mV after compensation using the CPU, decreasing by 76.5%. It was confirmed that compensation using the CPU reduces an offset variation.

The verification results for the built-in CPU in the OLED/OS/Si structure indicate that functional circuits beyond the display driver can be integrated into the Si layer and operate successfully. This result demonstrates the feasibility of enhancing the functionality of Si circuits. By placing a circuit that was previously implemented externally beneath the pixel array, it is possible to reduce the number of integrated circuits in AR and VR display devices and enable more compact housing.

Lastly, high-mobility OS was applied to the prototype display. While progress has been made in developing high-mobility OS for a glass substrate process [13], large scale integration (LSI) devices also need high-mobility OS. OS with high mobility, a low off-state leakage current [14], a high breakdown voltage, and high reliability is suitable for displays of AR and VR devices, which are required to achieve high luminance. In view of this, crystal indium oxide (crystal IO) was applied to an active layer of the OS FET of the prototype display. Figure 8 shows a displayed image. Favorable display was achieved, showing the applicability of a transistor whose active layer includes crystal IO (a crystal IO FET) to LSI devices.

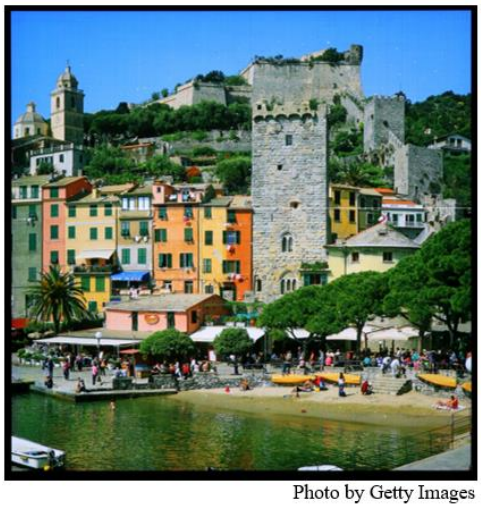

Figure 8. Photograph of image displayed on prototype display fabricated using crystal IO FETs.

5. Conclusion

A 90-Hz, 5009-ppi OLED display was fabricated using an OLED/OS/Si structure, in which the pixel array and drivers are monolithically stacked. The display achieved a luminance of 10000 cd/m^2. For functionality expansion of the Si circuit, the CPU was provided in the Si layer. It was confirmed that the amplifier offset compensation function using the CPU operated as expected, and this demonstrates the feasibility of functionality expansion. In addition, incorporating not only the CPU but also various other functional circuits into the Si layer can provide unprecedented AR and VR displays with multifunctionality, high luminance, and high definition.

6. References

[1] K. Parikh et al., “Next Generation Virtual Displays: Challenges and Opportunities,” SID Symp. Dig., 49, pp. 502-505 (2018).

[2] J. Nguyen et al., “Screen door effect reduction using mechanical shifting for virtual reality displays,” in Proc SPIE, Optical Architectures for Displays and Sensing in Augmented, Virtual, and Mixed Reality, 113100P (2020).

[3] T. Liu et al., “Full Color Organic Light Emitting Diodes on Silicon Micro-display with Ultra-high Luminescence and High Resolution,” SID Symp. Dig., 54, pp. 101-104 (2023).

[4] J. Jo et al., “High-luminance, large-size 4K OLED microdisplays for VR/MR applications,” Journal of SID, 32, pp. 371-378 (2024).

[5] H-J. Shin et al., “4670-PPI OLEDoS pixel circuit design for wide data voltage range in a 5 V 0.13 μm CMOS process,” Journal of SID, 32, pp. 165-173 (2024).

[6] S. Katsui et al., “5291 ppi Organic Light Emitting Diode Display using Field-effect Transistors Including a C-Axis Aligned Crystalline Oxide Semiconductor,” SID Symp. Dig., **50**, pp. 311-314 (2019).

[7] K. Kato et al., “5,291-ppi OLED display enabled by monolithic integration of C-axis-aligned crystalline IGZO FET and Si CMOS," Journal of SID, **30**, pp. 690-698 (2022).

[8] T. Saito et al., “Layout of 1.50-inch, 3207-ppi OLED Display with OSLSI/SiLSI Structure Capable of Division Driving Fabricated through VLSI Process with Side-by-Side patterning by Photolithography”, SID Symp., Dig., pp. 94-97 (2022).

[9] M. Kozuma et al., “OLED Microdisplay with Monolithically Integrated CAAC-OS FET and Si CMOS Achieved by Two-Dimensionally Arranged Silicon Display Drivers," IEEE Journal of the Electron Devices Society, **12**, pp. 187-194 (2024).

[10] JP patent7,554,334.

[11] M. Kaneyasu et al., “New Pixel Circuits for Controlling Threshold Voltage by Back-gate Bias Voltage using Crystalline Oxide Semiconductor FETs,” SID Symp. Dig., **46**, pp. 857-860 (2015).

[12] Y. Yamane et al., “3207-ppi, 1.50-in. OLED Microdisplay with All Pixels Formed Through RGB Side-by-Side Patterning by Photolithography”, SID Symp., Dig., pp. 1334-1337 (2023).

[13] Y. Magari et al., “High-mobility hydrogenated polycrystalline In2O3 (In2O3:H) thin-film transistors” Nature Communications 13, Article number:1078 (2022).

[14] S. Yamazaki et al., “High-performance single-crystalline In2O3 field effect transistor toward three-dimensional large-scale integration circuits,” Commun. Mater., 5, 184 (2024).