Invited paper: Power-Saving Strategies in High-Resolution 4K VR LCD Technology

Yung-Hsun Wu, Chia-Hao Tsai, Chih-Hao Chang, Yi-Hsiu Wu, Ming-Jou Tai, Jiou-Teng Lai, Zheng-Jun Shih, Yuan-Sheng Yang, Jian-Hua Luo, Tzu-Yu Kuo, Chiu-Lien Yang
Innolux Corporation, Miaoli, Taiwan

Abstract

This article explores advanced power-saving strategies for 4K high-resolution VR LCD, focusing on increasing pixel aperture ratio and reducing transmittance degradation caused by misalignment issues. To address these challenges, we discuss COA architectures and LTPO technologies with short-channel design. This approach reduces overall power consumption above 20%, creating high efficiency and performance displays suitable for next-generation VR applications.

Author Keywords

VR, MR, LCD, Display, High resolution, Sub-pixel Rendering, Mini-LED backlight, LTPO, COA, Low power consumption

1. Introduction

As Virtual Reality (VR) and Mixed Reality (MR) technologies continue to evolve, there is a growing demand for high-resolution displays[1-3]. However, the increases in resolution and pixel density result in significantly higher power consumption. This high power demand poses a particular challenge for VR devices, where portability and extended battery life are essential for optimal user experience. With the resolution of VR/MR display approaching 4K, such as Apple's Vision Pro, emerging as a critical element to enhance user immersion. INNOLUX has led the industry in developing 4K VR/MR AMLCDs with scanning backlight technology, achieving significant power savings with total power consumption of approximately 1.25W in our work. [4-5].

Recently, the request of specification demand in total power comes to 1W. To address these challenges, this study introduces a series of innovative techniques focused on enhancing panel transmittance to reduce power consumption while maintaining display quality. One of the core strategies in this work is optimizing pixel aperture by utilizing low-reflectance metal as the shielding layer(Low-Reflectance Shielding Layer, LRSL) onto array substrate, replacing traditional black matrix materials on color filter substrate(CF BM). Traditional CF BM materials due to the intrinsic characteristics of resin, face limitations in achieving fine-line patterning, which reduces the pixel aperture ratio. Additionally, CF substrate alignment with the array substrate can lead to misalignment issue, further increasing aperture losses. By employing LRSL directly on the array substrate, our approach achieves significantly finer line patterns, increasing the effective aperture area for each pixel while simultaneously eliminating the alignment issues associated with CF. This enhancement improves panel transmittance, providing a particular advantage for VR applications, where high brightness and contrast are essential to an immersive experience.

In addition, this study introduces an improved Color Filter on Array (COA) architecture. The newly developed COA structure further enhances pixel aperture, thereby improving panel transmittance. This COA technology works synergistically with the Low-Temperature Poly-silicon and Oxide (LTPO) Thin-Film Transistor (TFT) design[6-7], particularly beneficial in ultra-high-resolution VR panels. By designing and implementing short-channel TFT devices with reduced size, the occupied pixel area is minimized, which further increases the pixel aperture ratio. Together, these techniques maximize the effective transmittance of the display, allowing for reduced backlight intensity without compromising brightness or image quality, and thereby supporting lower backlight power consumption. These power-saving strategies collectively reduce the total module power consumption from 1.25W to lower than 1W.

2. Architecture and pixel design for low power consumption

2.1 Low power backplane technology

As VR display resolution reaches 4K with pixel densities exceeding 2000 ppi, balancing display quality, power efficiency, and high refresh rates has become increasingly challenging. To address these demands, INNOLUX has developed an innovative technology that integrates Low-Temperature Poly-silicon and Oxide (LTPO) backplane with Color Filter on Array (COA) for VR displays.

In Fig.1, illustrates a schematic diagram of the array substrate architecture combining LTPO and COA technologies, which realized in a 2.56" 4K LTPO and COA LCD panel.

The application of Indium Gallium Zinc Oxide (IGZO) TFT to the pixel TFT in the display area enhances high-resolution pixel aperture. The channel region of IGZO TFT were determined by self-aligned with a top-gate metal mask and the source-drain regions by ion implantation through the gate insulator. Meanwhile, employing Low-Temperature Poly-Silicon (LTPS) TFT in the non-display area, which encompasses circuits in the border region, such as H-driver and V-driver, ensures high driving capabilities, meeting the requirements for a high refresh rate.

Notably, the LTPS gate electrode also serves as both the bottom gate and the light-shielding layer for the IGZO TFT. This dual role helps to block light interference and enhance performance in the active display area. Within this area, IGZO TFT is designed with a double-gate structure, incorporating both a top gate and a bottom gate, which improves current driving capabilities to meet the specification of high refresh rate demands required for VR applications.

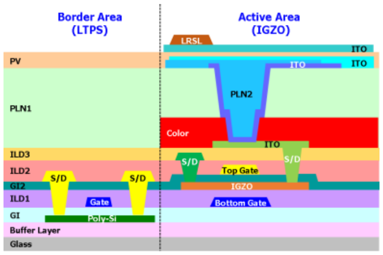


Figure 1. Schematic diagram of LTPO and COA backplane for 4K VR display

In the Active Area, the drain electrode of the IGZO TFT is used a high-transmittance ITO (indium tin oxide) electrode with a transparency exceeding 95%. Unlike traditional metal electrodes, which are opaque, the use of ITO maintains pixel aperture ratio without sacrificing transmittance, thereby enhancing the overall

ISSN 0097-996X/25/5601-197-$1.00 © 2025

display brightness and quality.

Additionally, a second planarization layer (PLN2) is added in this architecture to fill the via hole in the first planarization layer (PLN1). This multi-layer structure provides a flatter surface for the pixel ITO electrode, further improving the liquid crystal (LC) efficiency and enhancing panel transmittance.

This innovative LTPO with COA structure effectively increases the pixel aperture ratio and transmittance, significantly reducing power consumption in VR displays, making it an ideal solution for ultra-high-resolution VR applications.

2.2 Advanced design for high transmittance pixel

2.2.1 High aperture pixel design

Enhancing the pixel aperture ratio is essential in high-resolution LCDs as it directly impacts display brightness and power efficiency. INNOLUX has developed the sub-pixel rendering design and algorithm to expand the dot size to 6μm by 12μm, thereby increasing the effective aperture area. Fig.2 illustrates the layout of the pixel shielding layers, Shielding Layer 1 (SL1) and Shielding Layer 2 (SL2). SL1 is aligned along the data line and employs a low-reflectance metallic material, referred to as the Low-Reflectance Shielding Layer (LRSL). This layer functions as an opaque shield and plays a critical role in minimizing color shifts at the left/right-side viewing angles, also for mitigating ghost image concerns in VR HMDs when viewed through the pancake lens. On the other hand, SL2 is aligned parallel to the gate line, where it functions as a shield for the channel of IGZO TFT while also covering the boundary area of the COA photoresists. This design helps reduce color interference between adjacent pixels positioned above and below SL2, thus ensuring better color consistency across the display. The line width design of SL2 is carefully optimized to balance TFT dimensions with the COA photoresist process margin.

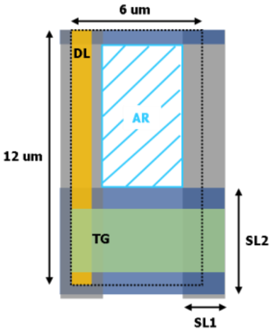


Figure 2. Shielding layer (SL1 and SL2) design in 4K pixel

To further enhance pixel aperture, we have optimized the line widths of both SL1 and SL2. SL1 was reduced to an ultra-narrow 2.0μm, achieving minimal width without compromising optical performance or inducing color shifts at oblique viewing angles. To reduce the width of SL2 is a great challenge, through the development of specialized COA photoresist materials and fine-tuned process parameters, the shielding area of COA boundary was successfully minimized to 5μm. As summarized in Table 1, these optimizations have collectively increased the pixel aperture ratio by approximately 30%, leading to a significant reduction in backlight luminance and helping for power saving.

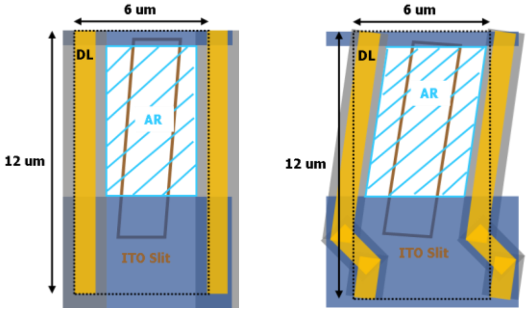
Shielding Layer Design	Old Design	New Design
SL1 Width (um)	2.2	2.0
SL2 Width (um)	6.5	5
Pixel Aperture Ratio	25.4%	33.1%

Table 1. Pixel aperture ratio with different SL1 and SL2 designs

2.2.2 Improve the LC efficiency

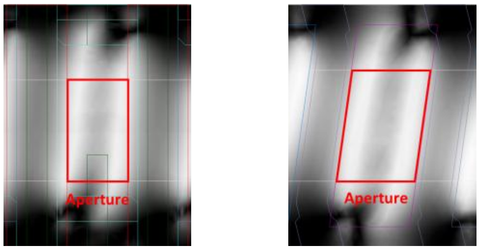
The new concept is to change the contour of pixel that designs as a form of parallelogram, instead of the old one which is in the form of rectangle. Fig.3(a) illustrates the old design, the pixel Indium Tin Oxide (ITO) slit is tilted about 5 to 10 degrees relate to SL1 or data line(DL). The SL1 pattern is parallel and overlap to DL and functions as lowing surface reflectance of DL. When we reduce the line widths of SL1 and SL2, meaning the pixel aperture area become larger, the rectangle pixel would have disadvantage in LC efficiency because of the percentage of dark area increasing in aperture regions and thereby reduce LC efficiency. The new design, parallelogram pixel shows in Fig.3 (b), SL1 parallels with ITO slit could maintain LC efficiency as high as possible even the increasing of pixel aperture.

As a result of the simulated images for LC efficiency, Fig.4 (a) and (b) respectively represent the rectangle and parallelogram pixels, the LC efficiency not only does not become smaller but also increases by 4% when we design the high aperture with the parallelogram pixel.



(a) (b)

Figure 3. The pixel design for (a) rectangle and (b) parallelogram shapes



(a) (b)

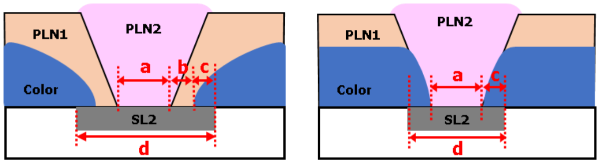
Figure 4. The images of LC efficiency simulated for (a) rectangle (b) parallelogram pixels

2.3 Color filter on array(COA) architectures

Reducing power consumption in VR head-mounted displays (HMDs) is crucial for minimizing battery weight, thereby enhancing user comfort. Reducing power consumption in display could significantly decrease the overall power demand of HMDs.

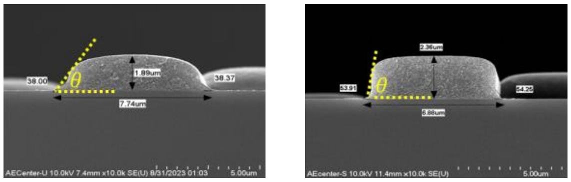
The COA backplane is a promising approach, integrating the RGB color and Black Matrix (BM) layers from the CF substrate directly onto the TFT substrate. For the application of ultra-high resolution VR displays, the COA backplane offers the advantage of addressing brightness inconsistencies between the left and right images, this issue mainly resulting from misalignment (MA) between the TFT and CF substrates during the assembly process, can be effectively mitigated with COA technology. Another significant benefit of COA technology is the increased pixel aperture ratio achieved by eliminating the need to account for MA, allowing for a narrower design of the shielding layers (SL) without compromising optical performance.

INNOLUX has developed two types of COA backplane architectures. First, we discuss the optimization of the SL2 line width. Fig.5(a) shows the old COA architecture, where the SL2 shielding design must consider several factors: the hole size of PLN1 (dimension a), the distance between PLN1 and the RGB color resists (dimension b), and the taper of RGB edge (dimension c). These determine the design of SL2 line width, which required to be at least 8μm. But considering for the pixel aperture ratio we designed it to 6.5μm finally, this would have some color shift issue in normal angle. To further enhance the performance of VR products, we introduced a new COA architecture, reducing the SL2 line width to 5μm, thus could improve panel transmittance and lower power consumption. As illustrated in Fig.5(b), the new COA architecture employs newly developed RGB materials with enhanced its chemical resistance and optimized processing parameters. This allows the capability of color-to-color spacing to align with the hole size of PLN1, effectively eliminating dimension b to zero. To address dimension c, we improved the RGB edge profile by optimizing RGB materials and processing conditions. As shown in Fig.6(a) and (b), the SEM images of the old and new color materials, the edge-profile angle(θ) of the RGB was increased to approximately around 80 degrees, resulting in a steeper profile. This adjustment minimizes dimension c, allowing for a total reduction in SL2 line width by approximately 23% and then without color shift issue.



(a) (b)

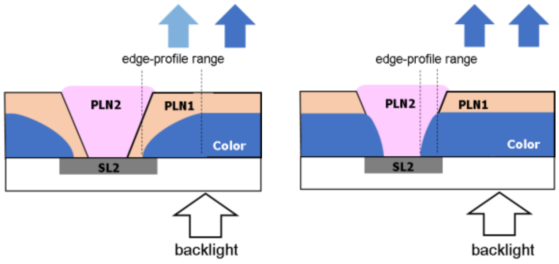
Figure 5. SL2 designs for (a) old and (b) new COA architectures



(a) (b)

Figure 6. SEM images of RGB profile for (a) old and (b) new color materials

Next, we discuss how the RGB edge profile impacts color shift issues. As shown in Fig.7(a), in the design under our old COA architecture, SL2 does not completely shield the edge profile range considering the specification of pixel aperture ratio. Because the RGB edge has a gentle slope, the thickness of the RGB photoresist there will be thinner than that of the flat area. When the LED backlight passes through the RGB photoresist, the thinner photoresist area will cause the problem of chroma uniformity comes from light penetrating the RGB to become lighter, and then resulting color shift issue. In Fig.7(b), the improved steep slope of RGB edge would get the small edge-profile range and to narrow SL2 line width to 5μm is enough for design margin which taking into account both aperture ratio and color shift issue.



(a) (b)

Figure 7. Schematic diagrams illustrating color shift mechanisms in (a) old and (b) new COA architectures

The design of SL1, as illustrated in Fig.8(a), it functions as LRSL in array glass to mitigate the transmittance variation and wild-angle color mixing for our 4K VR displays [4]. The most challenging item of reducing SL1 width is to keep the optical performance of wild-angle color mixing. In our new COA structure, we have thinned the thickness of organic layers for the purpose to design fine SL1. Fig.8(b) is the color-mixing simulation result of LRSL width versus color-mixing levels by different viewing angles. The simulation conditions are that the LRSL shifts left to DL by 0.4μm, and the viewing angles of the panel are observed from the right side with 30 and 45 degrees respectively. It shows that when the LRSL line width smaller than 1.9μm, the color-mixing level (JNCD) would out of specification in 45 degrees (red line). For considering the process variation of LRSL, we finally chose 2.0μm for the new COA structure. Overall, the new COA architecture enhances panel transmittance, increases the pixel aperture ratio, and lowers power consumption, making it ideal for ultra-high-resolution VR displays.

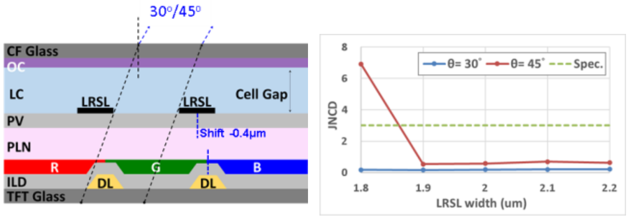


Figure 8. Color-mixing simulation of (a) layer structures and (b) results for LRSL width versus JNCD

3. LTPO short channel technology

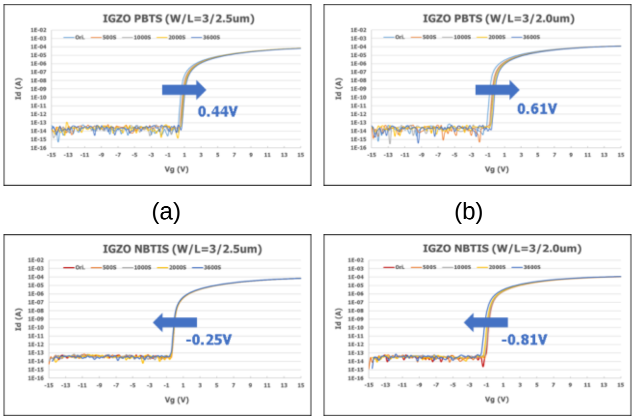
Incorporating LTPO technology has become essential in 4K VR displays for enhancing display performance while optimizing power consumption. By using IGZO TFT in the active area, compare to traditional LTPS TFT, it offers superior low-leakage characteristics, which are advantageous for high resolution applications. The lower leakage current enables to design smaller pixel TFT in the type of single channel, not like LTPS needs dual channel design to prevent leakage issue in off-state, effectively increasing the pixel aperture ratio and thereby enhancing display brightness and power efficiency.

To further reduce the power consumption of the display, we have developed the short-channel IGZO TFT devices with a minimized channel length of 2.0µm. This reduction in channel length pushes the aperture ratio optimization to its limits, allowing for maximum transmittance through each pixel. Table 2 summarizes the transfer characteristics of the IGZO TFTs that obtained from the Ids-Vgs transfer curves. The transition to a 2.0µm channel length, as opposed to the previous 2.5µm design, shows the similar levels in mobility and threshold voltage(V_{th}).

TFT W/L(µm)	3/2.5	3/2.0
Vth(V)	0.1	-0.5
Mobility($cm^2/V{\cdot}s$)	9.8	10.6
SS(V/dec)	0.1	0.1

Table 2. The characteristics of IGZO TFTs obtained from Id-Vg transfer curves

The Vth shift under Positive Bias Temperature Stress (PBTS) tested in gate voltage of +30V and thermal temperature in 60℃ with 3600-second stress time shows minimal deviation for IGZO TFT in both 2.5µm and 2.0µm channel lengths, as show in Fig.9(a) and (b) respectively. Specifically, the Vth shift for the 2.5 µm TFT is approximately 0.44V, while the 2.0µm TFT shows also slightly of 0.61V. On the other hand, the reliability testing of Negative Bias Temperature Illumination Stress (NBTIS) is more important than PBTS for IGZO n-TFT because the duty ratio of the negative is greatly higher than the positive in LCDs. The gate voltage of -30 V was applied and the temperature at 60℃ stressed for 3600 seconds, in the same time, backlight luminance was 8000 nits, irradiated from the bottom side of panel TFT. As shown in Figure 9(c) and (d), the Vth shift for the 2.5 µm TFT is -0.25V, while the 2.0µm TFT shows a slightly higher but still minor shift of -0.81V. These results demonstrate that reducing the channel length to 2.0µm, as developed by INNOLUX, does not significantly compromise device stability under prolonged usage conditions. This confirms the feasibility of implementing short-channel IGZO TFT technology in VR displays to achieve higher pixel aperture ratios and lower power consumption.



(a) (b)

(c) (d)

Figure 9. The Vth shift of PBTS as TFT channel lengths (a) 2.5µm and (b) 2.0µm, and NBTIS as (c) 2.5µm and (d) 2.0µm

4. Power-saving benefits

The 2.56” 4K VR display that integrated LTPO and COA technologies have developed by INNOLUX. The overall total power consumption measured approximately 1.25W with scanning backlight. Further, we significantly optimize the power through reduce IGZO TFT device size in pixel by short channel design and adjust COA architectures and materials for the narrow shielding layer design be available that could satisfy the optical performances. Both solutions direct the higher pixel aperture and lesser power demand in ultra-high resolution display. As illustrated in Fig.10, the total power consumption is improved below 1W by our power-saving strategies, represent an approximate 20% decrease in total power consumption.

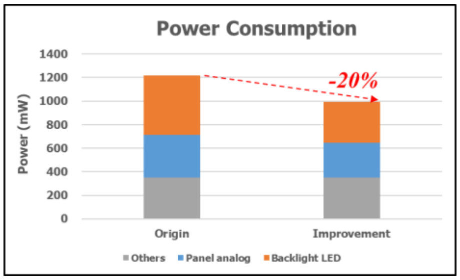


Figure10. Power consumption of 2.56” 4K VR LCDs

5. Conclusion

This study demonstrates innovative power-saving strategies for 4K VR AMLCDs, including COA and LTPO technologies. By optimizing pixel aperture and reducing misalignment issues, we achieved enhanced transmittance and minimized power consumption, reducing total module power below 1W, enabling high-performance, power-efficient VR displays.

6. References

1. Rao, L., Park, Y., Klement, A., Kang, C., Park, E., Zhuang, J., ... & Shen, S. (2023, June). 5-1: Invited Paper: Infinite Display for Meta Quest Pro. In *SID Symposium Digest of Technical Papers* (Vol. 54, No. 1, pp. 32-35).
2. Wu, Y. H., Tsai, C. H., Wu, Y. H., Cherng, Y. S., Tai, M. J., Huang, P., ... & Yang, C. L. (2023). Breaking the limits of virtual reality display resolution: the advancements of a 2117-pixels per inch 4K virtual reality liquid crystal display. *Journal of Optical Microsystems*, *3*(4), 041208-041208.
3. Wu, Y. H., Chang, C. C., Tsou, Y. S., Lo, Y. C., Tsai, C. H., Lu, C. H., ... & Chuang, F. M. (2023). Enhancing virtual reality with high-resolution light field liquid crystal display technology. *Journal of Optical Microsystems*, *3*(4), 041202-041202.
4. Wu, Y. H., Tsai, C. H. , Chang, C. H., Wu, Y. H., Cherng, Y. S., Tai, M. J., …&Yang, C. L.(2024). Toward the Challenges of 4K MR Using AMLCD. *SID Symposium Digest of Technical Papers*, vol. 55, no. 1, pp. 1262-1265
5. Wu, Y.-H., Tsai, C.-H., Wu, Y.-H., Cherng, Y.-S., Tai, M.-J., Huang, P., Yao, I.-A., & Yang, C.-L. (2023). High dynamic range 2117-ppi LCD for VR displays. *SID Symposium Digest of Technical Papers*, 54(1), 36-39.
6. Watakabe, H., Jinnai, T., Suzumura, I., Hanada, A., Onodera, R., Tada, M., Mochizuki, K., Tanaka, H., & Ito, T. (2019). Development of advanced LTPS TFT technology for low power consumption and narrow border LCDs. *SID Symposium Digest of Technical Papers*, 48(1), 541–544.
7. Chang, T. K., Lin, C. W., & Chang, S. (2019, June). 39-3: invited paper: LTPO TFT technology for AMOLEDs. In *SID Symposium Digest of technical papers* (Vol. 50, No. 1, pp. 545-548).