EM Compensation Applications and Results for Flexible Active-Matrix Organic Light-Emitting Diode Notebook Display

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Abstract

As a new NB display technology, flexible Active-Matrix Organic Light-Emitting Diode (AMOLED) display with more complex circuit system and algorithm architecture than LCD, which is facing more challenges from power consumption, screen flickering at low frequency, and screen flickering issues when switching frequency. Further expanding to Variable Refresh Rate (VRR) driving of gaming NB, as well as issues of screen latency and tearing, all pose more challenges. Aiming at the actual these problems in NB flexible AMOLED display, firstly, introduce and analyze the emitting signal. Secondly, apply it to some commonly used technical scenarios in NB display. Finally, describe and analyze some of the problems encountered in the design.

Keywords

EM compensation; flexible; NB display; active-matrix organic-light emitter diode display; variable refresh rate.

1. Introduction

Active-Matrix Organic Light-Emitting Diode (AMOLED) display have gained widespread adoption in wearable, smartphones, NB, and televisions devices due to their superior image quality and thin form factor. However, the issue of screen flickering with AMOLED display has been mentioned by many users. Flicker, an undesired variation in brightness, is often noticeable during VRR operation due to the emission characteristics of OLED pixels, which are sensitive to changes in voltage and current. This phenomenon can degrade the visual experience and contribute to eye strain. To address these issues, emission compensation techniques have been introduced to stabilize the luminance of OLED pixels under variable refresh rate. This paper explores the implementation of an emission compensation method that aims to maintain consistent brightness and color accuracy, regardless of refresh rate, by changing the number of complementary emission pulses and adjusting the duty of different emission pulses. This method reduces flicker and improves the overall user experience.

Figure 1 shows the control signal output from the Timing Controller (TCON) IC to the pixel circuit of the NB display panel. When the system changes the frequency through the longV method, the Vblank time will also change accordingly with the frequency. As the Vblank time increases, the number of lines in the Vtotal of one frame also increases. If the number of lines in the Vtotal cannot be divided by the cycle of one EM signal (1EM=75H), then as the frequency changes, there will be brightness differences in the image, resulting in flickering.

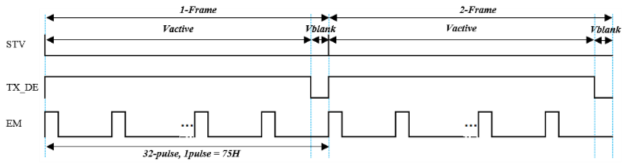

Figure 1. Output timing chart of TCON IC.

Figure 2 shows a solution that maintains the number of EM pulses and evenly distributes the increased Vblank time (as shown in region A) to the EM cycle (1EM=77H). But if this method cannot be divided by the EM pulses in a frame, the extra lines will not be evenly distributed. The general approach is to directly cut off the excess lines. This method may still cause flickering, especially during the VRR process.

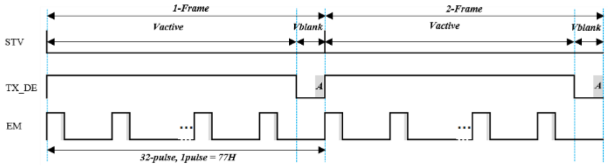

Figure 2. The increased Vblank is evenly distributed to each EM pulse.

In order to this issue, this paper proposes to fill in a complete EM signal. As shown in Figure 3, adding some line buffer is used to fill a complete EM signal (as shown in region C).

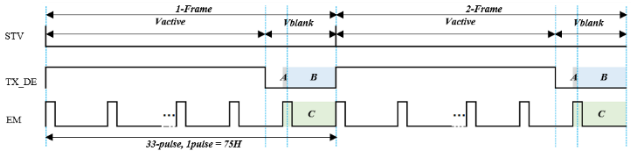

Figure 3. The increased Vblank is supplemented into a complete EM.

Figure 4 shows that when changing frequency (between 40Hz and 33.33Hz) on the system side, TCON IC's Frame Buffer System (FBS) output timing can be supplemented as an integer multiple of EM, and EM remains consistent without truncation during frequency variation.

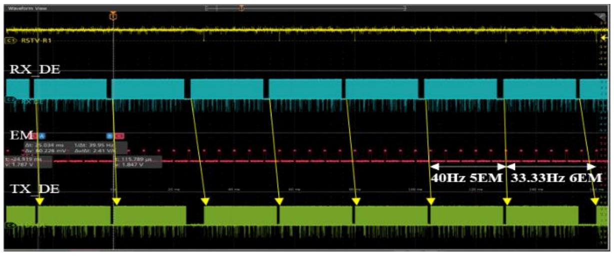

Figure 4. EM remains consistent without truncation during 40Hz and 33.33Hz frequency variation.

Table 1 shows the complete EM cycle frequency conversion. When the EM cycle is incomplete, it will be supplemented by the line buffer in TCON, which can achieve the minimum frequency conversion step of 1Hz.

Table 1. Complete EM cycle frequency conversion.

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Input Frequency (Hz)	EM pulse (quantity)	Compensation EM pulse (quantity)	Output Frequency (Hz)	Remark
120	32.00	32	120.00	
119	32.27	33	116.36	Min. 3Hz step
118	32.54	33	116.36	
..... 99	38.79	39	98.46	
98	39.18	40	96.00	Min. 2Hz step
97	39.59	40	96.00	
96	40.00	40	96.00	
..... 66	58.18	59	65.08	
65	59.08	60	64.00	Min. 1Hz step
64	60.00	60	64.00	
63	60.95	61	62.95	
..... 1	3840.00	3840	1.00	

On the other hand, combining algorithms to adjust the duty compensation of each EM, as shown in Figure 5, can also reduce flicker.

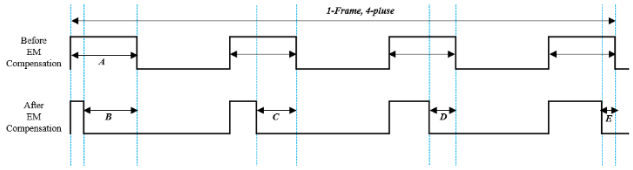


Figure 5. EM duty compensation.

This compensation method, as shown in Figure 6, aims to make the brightness of each EM pulse within one frame as consistent as possible, reducing the significant brightness difference when entering the first few EM pulses of the next frame from the last few pulses of one frame.

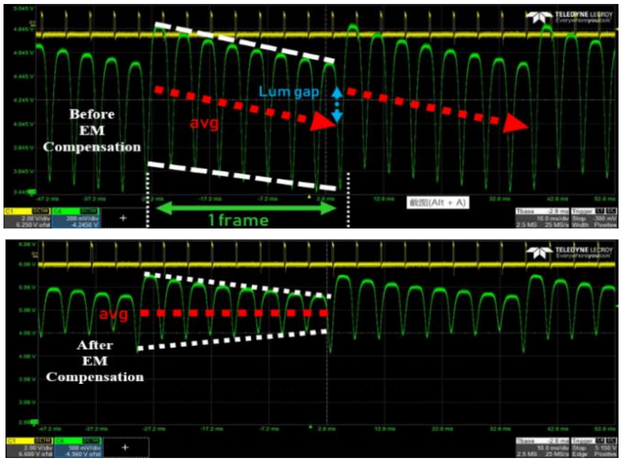


Figure 6. EM duty compensation reducing the significant brightness difference.

Based on these design methods, this paper will apply them to some commonly used technical scenarios in NB display and measure some data to verify them.

2. Application and Results

2.1 The Development Platform

The development platform consists of a Source board with 4 COPs and a Control board with TCON and FPGA IC. We used FPGA IC to embed EM compensation algorithm. We also use this platform to verify the flicker, power consumption, and VRR results of the AMOLED module. Additionally, improving the Panels deviation caused by the impact of the manufacturing process through automatic adjustment.

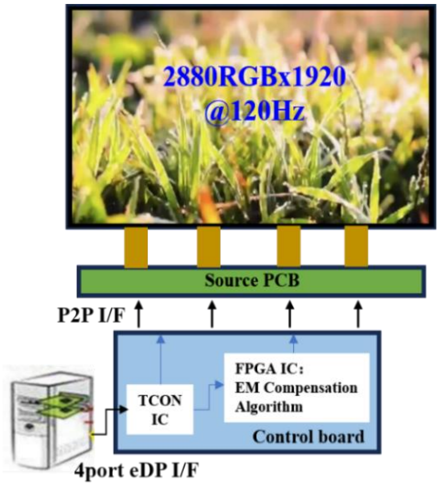


Figure 7. The development platform.

2.2 Test results applied to low frequencies

When the display operates at lower refresh rates (e.g., 10Hz for static content), flicker is more likely due to the increased time between pixel refreshes. EM compensation ensures that the pixel maintains stable brightness across these intervals, reducing flicker and brightness fluctuations. The flicker test results obtained based on EM compensation are shown in Figure 8.

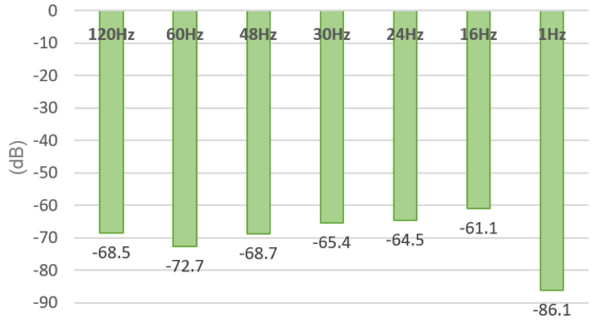


Figure 8. Flicker measurement.

In addition, the system technology of NB display can autonomously reduce the refresh rate according to different application scenarios (such as video playback, web browsing, etc.). By adjusting the refresh rate, unnecessary power consumption of the display can be reduced, thereby achieving energy conservation. As shown in Figure 9, power consumption was also tested at different refresh rates.

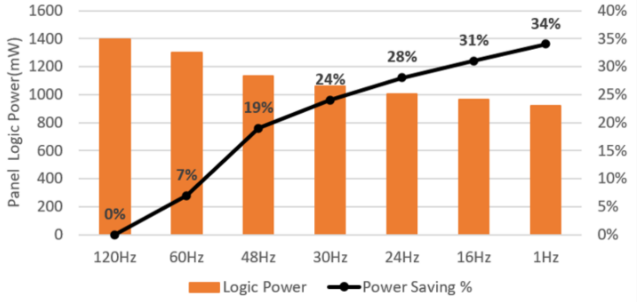


Figure 9. Power consumption measurement.

2.3 Test results applied to variable refresh rate

Next, we will extend to the validation of the gaming NB. According to this design method, the VRR gaming notebook will not experience flicker, and the flicker values tested by VESA tool are all below -60dB, as shown in Figure 10.

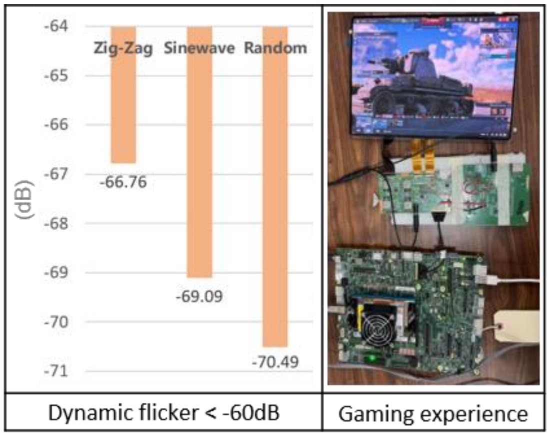
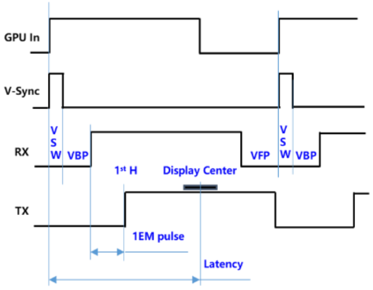


Figure 10. 120Hz ~ 1Hz VRR Flicker measurement by VESA Adaptive-Sync tool and the gaming experience.

Another important criterion for gaming NB is latency display analysis, which can eliminate screen tearing and minimize display stutter and input lag. This creates smoother and more fluid gameplay, especially in games where frame rates can fluctuate. By using Latency Display Analysis Tool (LDAT), we obtained the results shown in Table 2, and all the results meet the specifications.

Table 2. LDAT test and analysis results.

Test items		Test results	
LDAT	Display Latency@L64 -> L192 Spec : 120Hz latency < 6.67ms 60Hz latency <13.33ms	Pass	120Hz : 5.492ms 60Hz : 5.575ms
	Luminance Invariance with Max Frame and Max Frame/2 @L16 ~L255 Spec : ΔLv < 4%	Pass	120/60Hz : ΔLv < 0.7% 60/30Hz : ΔLv < 0.8%
	Static Flicker and Frame Range Test @ L128 Spec : Flicker < -45dB	Pass	-57dB ~ -70dB
	Dynamic Flicker @ L128 Spec : <-50dB	Pass	-55dB ~ -68dB
	Gamma @ L8 ~ L255 Spec : 2.2±0.2	Pass	2.318



120 Hz display latency: 5.5ms
(vsync to smallest detectable change)
Display Latency:
Average: 5.492
Min: 4.656
Median: 5.62
Median in frame times: 0.6744
Max: 6.68
Test Result: Pass

60 Hz display latency: 5.6ms
(vsync to smallest detectable change)
Display Latency:
Average: 5.575
Min: 4.71
Median: 5.546
Median in frame times: 0.3327
Max: 6.392
Test Result: Pass

Figure 10 is also used to demonstrate the gaming experience. Many competitive gamers use LDAT to minimize system latency and ensure faster response times.

2.4 Automatic EM and flicker turning system

We designed automatic EM and flicker turning system as Figure 11. In order to fast measure and find the duty value required to compensate for EM and optimize the flicker of the screen. This system consists of flicker measuring device (CA410) and program built in PC to control board for measured data collecting and analyzing.

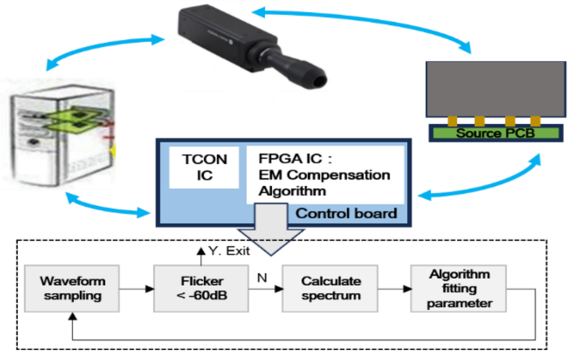


Figure 11. Automatic EM and flicker turning system.

Through this system, automatic turning can be achieved to solve the problem of panel deviation caused by process and optimize flicker to achieve specifications below -60dB. This system makes it possible to repeated automatic measurement, calculation and correction. Figure 12 shows the optimized flicker data based on our system.

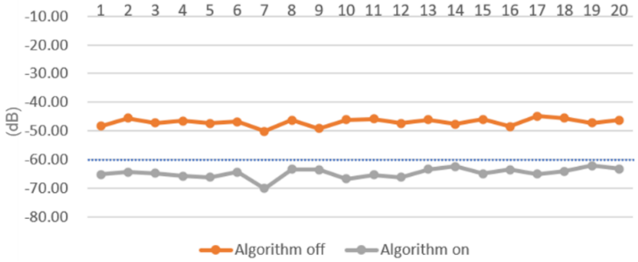


Figure 12. Optimized Flicker measurement based on automatic EM and flicker turning system.

2.5 Issue analysis

As is well known, GPU manufacturers will release the eDP1.5 platform by the end of this year, and eDP1.5 NB products will also be launched on the market starting next year. Embedded DisplayPort (eDP) version 1.5 leverages a new Panel Replay (PR) protocol for enhanced panel self-refresh capability. During self-refresh, the GPU and eDP1.5 interface enter a low state to conserve system power and extend battery life, as shown in Figure 13. The use of Panel Replay enhances display timing control making it compatible with Adaptive-Sync, simplifies panel control protocol, and enables further power savings, improving gaming and media playback performance.

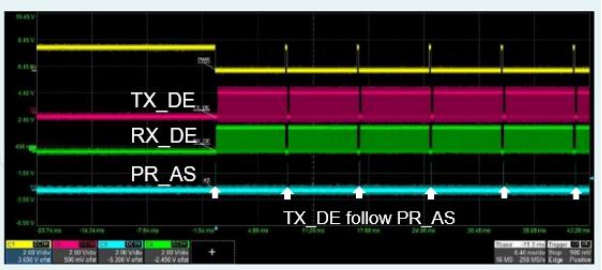


Figure 13. Display timing control with Panel Replay protocol

Our research found that during self-refresh, even if the Panel Replay does not send anything, once the GPU has updated data, we need to immediately exit of self-refresh and follow the GPU.

Otherwise there will be a lost data and screen delay phenomenon. After modifying the behavior of the timing, as shown in Figure 14, this phenomenon will no longer occur.

Figure 14. Display timing no update because Panel Replay no send anything (a) and improving the behavior of the display timing (b).

3. Conclusion

In this paper, we have developed an EM compensation algorithm that adjusts the duty of different EM pulses and fills them with integer multiples of EM to achieve flicker and brightness stability when the system changes frequency. This brings significant benefits to the power consumption of the system in low-frequency applications and can increase battery life. In variable refresh rate (VRR) environments, this reduces visual artifacts like tearing and stuttering of fast moving graphics, especially for gaming or fast content transitions. We also develop automated measurement system, fast measurement and finding the duty value require to compensate for EM and optimize the flicker of the screen, improving production yield and take time. Finally, combining eDP1.5 adds new features and protocols and integrating EM compensation algorithms, ASIC development is completed and commercialized.

4. Acknowledgements

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5. References

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