1 Hz Low-Power Consumption Liquid Crystal Display Based on Oxide Thin Film Transistors

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Abstract

Reducing power consumption of liquid crystal displays (LCDs) helps meet global energy policies worldwide. Here we introduce a series of strategies, including panel designs and materials selection, and fabricated a low-power consumption LCD with 1 Hz refresh rate, based on oxide thin film transistors (TFTs).

Author Keywords

Low-power consumption; LCDs; 1 Hz; Oxide TFTs.

1. Introduction

LCDs exhibits widespread applications range from smartphones, pads, notebooks, monitors, TVs, vehicles, to public display boards. For all these display consumer goods, low-power consumption helps meet global energy policies worldwide. Logic power consumption and backlight power consumption are two main parts of LCDs power consumption, which could be optimized significantly by reducing refresh rate and increasing transmittance. Here, low logic power consumption is mainly focused by low refresh rate driving. Under low refresh rate driving, TFTs are mostly depleted during one frame and the current leakage could be a concern. Oxide TFTs have advantage over amorphous silicon (a-Si) TFTs and low temperature poly-silicon (LTPS) TFTs [1] because of the extremely low off-current. Therefore, low refresh driving are mostly realized with oxide TFTs.

Under low refresh rate driving, the image quality should always be guaranteed. However, the optical flickers could impede the low refresh rate driving [2-4]. There are two primary contributors for low refresh rate optical flickers. The first one is the voltage-holding properties. The failure of voltage-holding properties maintenance could results in a brightness decline over time. The other one is the noticeable flexoelectric effect (FEE) of liquid crystal (LC) under electric potential because of the high transmittance, wide field-of-view, and high resolution [5-8]. The FEE of LC could bring varying brightness levels depending on the voltage polarity. To achieve low refresh rate as to 1 Hz, both voltage-holding properties and FEE must be resolved for high image quality.

Here, based on low refresh rate driving and optical flicker optimization strategy, a high image quality, low-power consumption 13.3 inch 1920*1200 notebook with 1 Hz refresh rate based on oxide TFTs is fabricated. The optical flicker level under 1 Hz is lower than -60 dB, which exhibits a high image quality. Meanwhile, the logic power consumption is reduced from 392 mW to 266 mW, when decreasing the refresh rate from 60 Hz to 1 Hz.

2. Low Refresh Rate Driving to 1 Hz

For low-power consumption strategy, reducing the refresh rate, which is linearly dependent on the logic power consumption, is one of the most effective methods. A common way to realize low refresh rate driving even to 1 Hz is holding the refresh time and increasing the V-blanking time, as shown in Figure 1. For 1 Hz display, the frame would refresh only once per second. Therefore, the pixel TFT would be charged much less frequently when compared with high refresh rate driving. The logic power consumption could be effectively reduced. However, the inevitable leakage current during the exponentially increased V-blanking time would bring brightness fluctuation. This brightness fluctuation is tightly associated with optical flicker, which is unacceptable for high quality image display. Even worse, human eyes are more sensitive to the optical flicker under low refresh rate driving. Therefore, reducing the optical flicker is critical to our high image quality, low-power consumption panels.

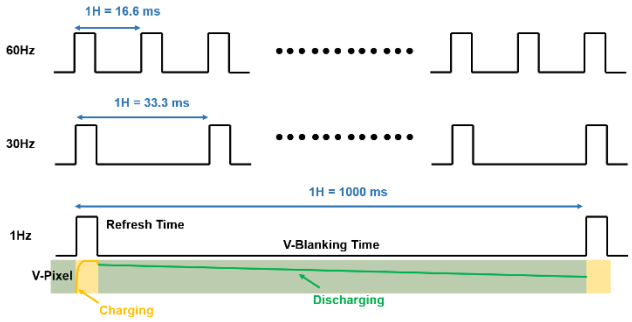

Figure 1. Scheme of clock signal and pixel TFT voltage under high and low refresh rate driving.

To evaluate the optical flicker, the JEITA method [9] is used under the gray 127 level image. Generally, the optical flicker could be expressed as:

$$Flicker_{JEITA}(dB) = (20 * log_{10} \frac{F(xHz)}{F(0Hz)} - y)(dB) \quad (1)$$

Where F(x Hz) and F(0 Hz) represent the brightness intensity amplitude at x Hz and 0 Hz (DC component) , y is human eye sensitivity factor. For 1 Hz display, y equals 0.

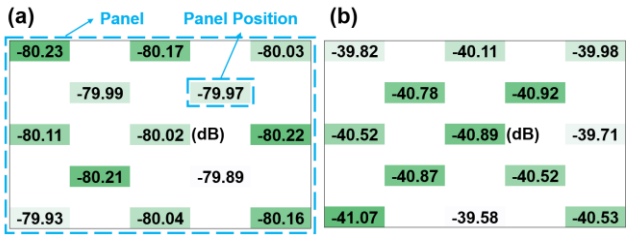

Figure 2. The gray 127 level image optical flicker under (a) 60 Hz and (b) 1 Hz before optimization.

The optical flicker level of thirteen points which are evenly distributed in the panel are measured for our panel under 60 Hz and 1 Hz, as shown in Figure 2. Under 60 Hz driving, the average optical flicker level is around -80 dB, which indicates a high quality image. However, when decrease the refresh rate to 1 Hz, the optical

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flicker level is deteriorated to around -40 dB. The optical flicker level should lower than -60 dB for high quality image under 1 Hz driving.

Optical flicker results from the brightness fluctuation between positive and negative frames. There are many factors could lead to this deterioration, including the reduction of voltage holding ratio (VHR), the LC FEE and the feed through-voltage (ΔV_p). VHR and FEE are responsible for the optical flicker level, while ΔV_p could decline the uniformity. Several optimization strategies are employed for the high quality image under 1 Hz.

3. Optical Flicker Optimization

The key of the optimization of optical flicker is minimizing the brightness fluctuation between positive and negative frame. There are three critical influences of brightness fluctuation: the brightness deterioration during one frame, the different luminous efficacy between two frames and the unequal operation voltage (V_{op}) between two frames. For the first influence factor, the leakage current between common electrode and pixel electrode is the key, which means the VHR should be maintained at a high level. For the second influence factor, the LC FEE is critical. LC with small dielectric anisotropy and large elastic constants is used for 1 Hz display. For the third influence factor, the common electrode voltage (V_{com}) shift caused by ΔV_p could lead to the unequal V_{op}. The key to avoid the unequal V_{op} is decrease ΔV_p. Actually, V_{com} could be adjust to a best value to eliminate the influence of ΔV_p. However, the best V_{com} for the whole panel would not be equal because of the process fluctuations, which means the non-uniformity of optical flicker. Therefore, decrease ΔV_p is still necessary for the optimization. All in all, VHR, LC FEE and ΔV_p are optimized for high quality image under 1 Hz display.

Voltage Holding Ratio: For 1 Hz display, the VHR reduction could be the primary factor for optical flicker. The VHR reduction is reflected from an obvious current leakage between common electrode and pixel electrode. There are two method to reduce the impact of current leakage. The first one is the direct reduction of leakage current from TFTs and other panel materials which are mainly LC and polyimide (PI). The second one is the increase of storage capacitor (C_{st}). In this case, the current leakage shows less effect on brightness during one frame.

For 1 Hz display, the V-blanking time multiply increase and the pixel TFTs are mostly depleted during one frame. Therefore, the off-current of pixel TFTs are the main source of leakage current. To minimize the off-current of TFTs, amorphous IGZO (a-IGZO) is used as the channel material. The hole-mobility of a-IGZO is extremely low because of its large effective mass of hole-carrier. Therefore, a-IGZO TFT exhibits off-current as low as to 10^{-13}A, as shown in Figure 3(a). Relatively, a-Si TFT shows an off-current of 10^{-11}A, as seen in Figure 3(b).

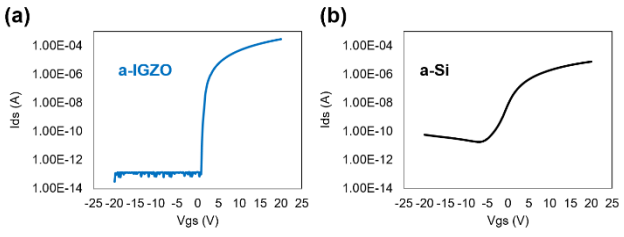

Figure 3. I_{ds}-V_{gs} curve of (a) a-IGZO and (b) a-Si TFTs.

Except for the off-current of pixel TFTs, the leakage current of panel materials, which are mainly from LC and PI, could also contribute to the VHR reduction. As shown in Figure 4(a), the selection of high-resistance LC and PI is helpful to the maintenance of VHR because of the smaller leakage current. The VHR is a relative value based on the test cell. A sealed test cell, whose scheme is shown in Figure 4(b), is used to evaluate the VHR of different kinds of LC and PI. For different kinds of LC and PI, the test cell with the same size and structure are used to obtain an accurate VHR. The high-resistance LC and PI exhibits a VHR of 99.5% at 1 Hz, while the low-resistance LC and PI only exhibits a VHR of 94.8%, as shown in Figure 4(c). Naturally, the VHR of LC and PI would increase under higher refresh rate.

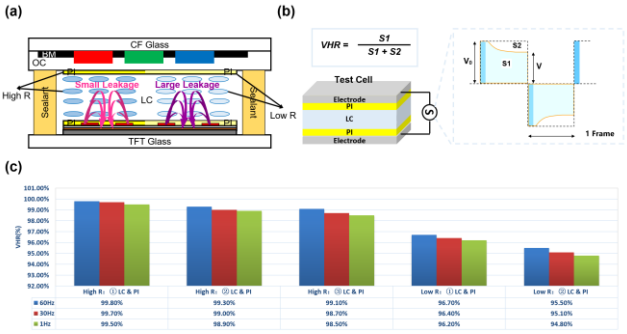

Figure 4. (a) Scheme of different leakage currents between high/low-resistance LC and PI. (b) Scheme of test cell and the calculation method of VHR. (c) VHR of five kinds of high/low-resistance LC and PI under 60 Hz/30 Hz/1 Hz.

Except for the reduction of leakage current, increase the storage capacitor could also improve the VHR maintenance ability. The storage capacitor is mainly consist of the capacitor between pixel electrode and common electrode with SiN_x as the capacitive dielectric, as shown in Figure 5(a). Usually, decrease the thickness of capacitive dielectric could increase the storage capacitor. While, the storage capacitor could still be not large enough for 1 Hz display. Therefore, a dual common electrodes structure as shown in Figure 5(b) is adapted to further increase the storage capacitor. As the C_{st} increases from 252.53 fF to 973.42 fF by decreasing the dielectric thickness and adapting dual common electrodes structure, the maximum 1 Hz flicker level under gray 127 level image is optimized from -39.58 dB to -53.44 dB, as shown in Figure 5(c).

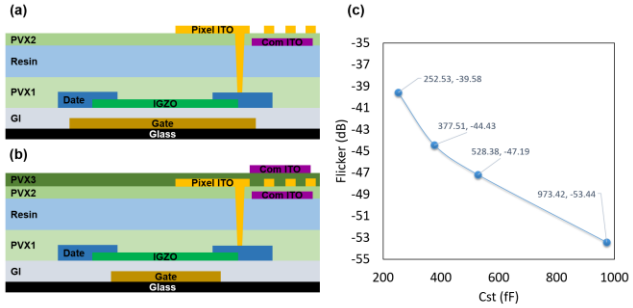

Figure 5. (a) Structure of normal back channel etch (BCE) TFT. (b) Structure of dual common electrodes BCE TFT for increase the storage capacitor. (c) The maximum 1 Hz flicker under gray 127 level image with increasing C_{st}.

Generally, adapting a-IGZO as TFT channel material and high-resistance LC and PI could effectively reduce the leakage current, and a dual common electrode TFT structure could bring a larger storage capacitor. The VHR under 1 Hz display could be maintained through these optimization strategy.

LC Flexoelectric Effect: Except for VHR reduction, LC FEE could also bring brightness fluctuation between positive and negative frames. The FFE is a phenomenon that the distortion of the LC director and the electric polarization are coupled so that the polar axis of LC is accompanied with splay and/or bend deformations. The FEE induced polarization is given by:

$$\overrightarrow{P_f} = e_{11}\vec{n}(\nabla \bullet \vec{n}) + e_{33}\vec{n}(\nabla \times \vec{n}) \times \vec{n} \quad (2)$$

Where e_{11} and e_{33} are flexoelectric coefficients, and $\vec{n}$ is the unit vector of the LC orientation. The interaction between the electric polarization and an externally applied electric field is called flexoelectric interaction. This interaction is sensitive to the polarity of the applied electric field. The electric field produced by the common and pixel electrodes is not spatially uniform, and thus flexoelectric interaction exist if the liquid crystal has non-zero flexoelectric coefficients.

In addressing the display, from the positive frame to the negative frame, the polarity of the electric field changes direction. The aligning effect of the electric field due to the flexoelectric interaction changes. Therefore, the orientation of the liquid crystal is different in the two frames. And the brightness could be different, as shown in Figure 6. In the positive frame, the minimum transmittance occurs on the top of patterned electrodes, but it shifts to the middle of electrode gaps during negative frame. This clearly confirms the dynamic transition of LC director distributions caused by the flexoelectric polarization.

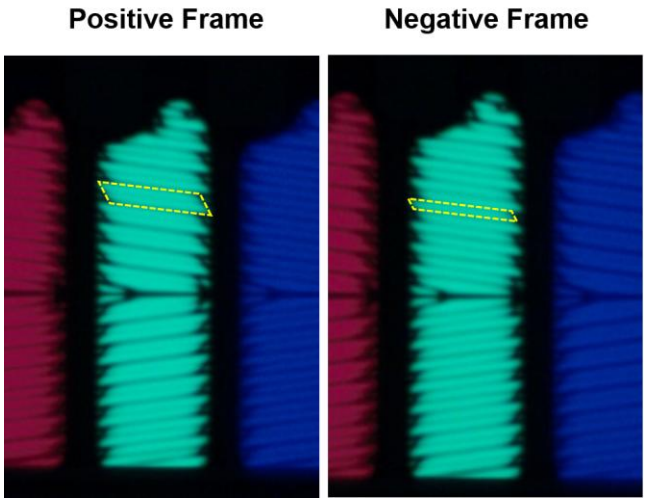

Figure 6. Brightness difference between positive and negative frames.

However, e_{11} and e_{33} are hard to be measured accurately. And FEE is strong in a system with large shape polarity and permanent dipole moment, which means there is a correlation between flexoelectric coefficients and dielectric anisotropy [10]. In an ununiformed electric field, the total Gibbs free energy (F_{total}) consists of three terms: elastic (F_e), dielectric (F_d), and flexoelectric (F_f).

$$F_e = \frac{1}{2}K_{11}[\nabla \bullet \vec{n}]^2 + \frac{1}{2}K_{22}[\vec{n} \bullet (\nabla \times \vec{n})]^2 + \frac{1}{2}K_{33}[\vec{n} \times (\nabla \bullet \vec{n})]^2 \quad (3)$$

$$F_d = -\frac{1}{2}\varepsilon_0 \Delta\varepsilon[\vec{n} \bullet \vec{E}]^2 \quad (4)$$

$$F_f = -[e_{11}\vec{n}(\nabla \bullet \vec{n}) + e_{33}\vec{n}(\nabla \times \vec{n}) \times \vec{n}] \bullet \vec{E} \quad (5)$$

$$F_{total} = F_e + F_d + F_f \quad (6)$$

Where K_{11}, K_{22}, and K_{33} are the splay, twist, and bend elastic constants, ε_0 and $\Delta\varepsilon$ are the vacuum dielectric constant and the dielectric anisotropy of parallel and vertical dielectric constant. Therefore, K_{11}, K_{33} and $\Delta\varepsilon$, which should be related to e_{11} and e_{33}, could also influence the optical flicker, which are simulated by using TechWiz LCD. To evaluated the influence on optical flicker of these factors, a relative flicker (Fli_{Rela}) is defined as $Fli_{Rela} = 2(T_{Max}-T_{Min}) / (T_{Max}+T_{Min})$, as shown in Figure 7(a). The simulation result of $|\Delta\varepsilon|$ influence is shown in Figure 7(b), which indicates a smaller $|\Delta\varepsilon|$ is beneficial to the optical flicker. As for elastic constants, larger K_{11} and K_{33}, which means hard to splay and bend, exhibit better optical flicker behavior as shown in Figure 7(c).

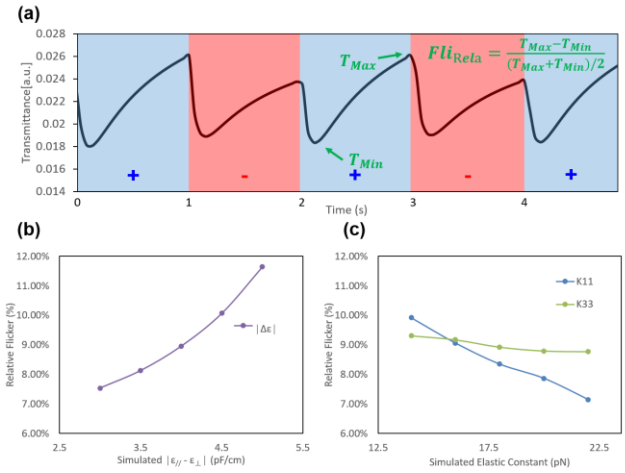

Figure 7. (a) Simulated transmittance versus time during positive and negative frames. (b) Simulated relative flicker versus the difference between parallel and vertical dielectric constant (c) Simulated relative flicker versus splay, twist, and bend elastic constants.

Generally, LC properties are strongly related to FEE. According to the simulation results, adapting LC with smaller $|\Delta\varepsilon|$ and larger K_{11} and K_{33} could effectively suppress the FEE and optimize the optical flicker. An optimized LC is used for 1 Hz display.

Feed-through Voltage: Besides the optical flicker level, the uniformity of optical flicker is also important for high quality image in the whole panel. The non-uniformity usually comes from the difference of the best V_{com} in the whole panel. In this situation, the V_{op} for positive and negative frames could be unequal in somewhere of the panel, and leads to severe optical flicker.

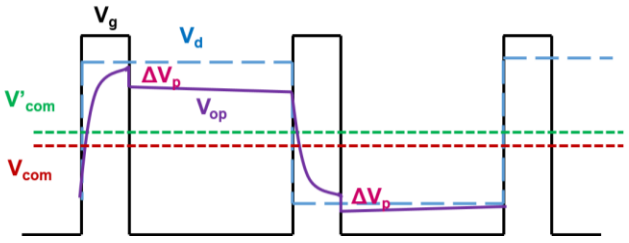

Figure 8. Feed-through voltage of the signal voltage.

To avoid a single direction deflection of LC and keep zero DC voltage, positive and negative frames are employed alternately. The absolute value of V_{op} for positive and negative frames must be equal. The ideal V_{com}, which could be marked as V'_{com}, should equal to half of the sum of V_d for positive and negative frames, as shown in Figure 8. However, a feed-through voltage, which is mainly aroused from the parasitic capacitance between gate electrode and source electrode would increase or decrease the signal voltage as gate driver off. This feed-through voltage could be expressed as:

$$\Delta V_p = \frac{C_{gs}}{C_{gs} + C_{st} + C_{lc}} (V_{gh} - V_{gl}) \quad (7)$$

Where C_{gs}, C_{st}, C_{lc}, V_{gh} and V_{gl} represent the parasitic capacitor between gate electrode and source electrode, storage capacitor, LC capacitor, high gate voltage and low gate voltage. The key to suppress ΔV_p is reducing C_{gs} and increasing C_{st}. The C_{gs} mostly come from the staggered gate electrode and source electrode for the BCE TFT as shown in Figure 5(a). A simple method to reduce the staggered area is shorten the gate electrode length, as shown in Figure 5(b). By this way, the C_{gs} could be reduced from 9.82 fF to 5.17 fF. As mentioned before, C_{st} could be increased by a dual common electrode design, also shown in Figure 5(b). Suppressing ΔV_p by decrease C_{gs} and increase C_{st} could effectively optimize the uniformity of the optical flicker in the whole panel.

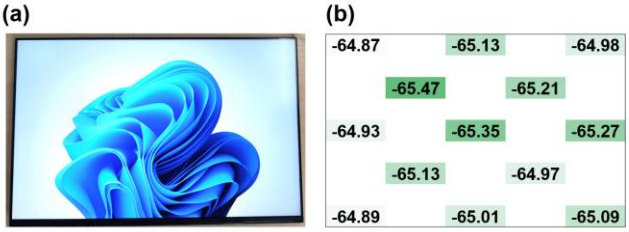

Figure 9. (a) A 13.3 inch 1920*1200 notebook with low power consumption. (b) The gray 127 level image optical flicker under 1 Hz after optimization.

After the optimization of VHR, LC FEE and ΔV_p, a low-power consumption 13.3 inch 1920*1200 notebook is fabricated, as shown in Figure 9(a). Under 1 Hz driving, the optical flicker level is lower than -60 dB, as shown in Figure 9(b), indicating a high image quality. The logic power consumption is measured under a mosaic image. It's reduced from 392 mW to 266 mW when the refresh rate decreases from 60 Hz to 1 Hz.

4. Conclusion

LCDs exhibits widespread applications which are required for low-power consumption to help meet global energy policies worldwide. Low refresh rate driving is an effective way to reduce power consumption. However, optical flicker, which could affect the image quality, must be concerned. The optical flicker level and uniformity are optimized by VHR maintenance, FEE suppression, and ΔV_p reduction. A low-power consumption 13.3 inch 1920*1200 notebook is fabricated. Under 1 Hz driving, the optical flicker level is lower than -60 dB, which indicates a high image quality, and the logic power consumption is reduced to 266 mW.

5. Acknowledgements

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6. References

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