Insulation and Planarization of Nanowire LEDs

Seth Coe-Sullivan[1,2^], Binh H. Le[2], and David Laleyan[2]
[1]NS Nanotech, Inc., Ann Arbor, Michigan, USA
[2]NS Nanotech Canada, Inc., Montréal, Canada
^: seth@nsnanotech.com
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Abstract
Nanowire-based InGaN light-emitting diodes (nanoLEDs) have progressed to being the most efficient LEDs ever made at extremely small lateral sizes in research labs, and have the added benefits of highly directional emission and extremely narrow bandwidth. However, critical challenges of insulation and planarization remain before this technology can be deployed commercially.

1. Introduction
Submicron-scale, high-efficiency, directional, multicolor narrowband light sources monolithically integrated on a single chip are required by the display technologies of tomorrow, especially the small displays required for augmented, mixed, and virtual reality (AR/MR/VR) headsets. Achieving efficient green and red light-emitting diodes (LEDs) using GaN-based technology has proven stubbornly difficult, but previous InGaN nanowire studies have shown promise to solve such critical challenges [1,2]. Nanostructured LEDs exhibit low dislocation densities and improved light extraction efficiency. And multicolored emission can be demonstrated from InGaN nanocolumn arrays integrated on a single chip. Thus, display technologies based on nano-LED pixel arrays integrated on a single chip could become the ultimate emissive light sources for next-generation AR/VR displays. However, the manufacturability of such devices has yet to be demonstrated. In this work we highlight and elucidate the critical issue of insulation of such 3D structures, a challenge somewhat unique to these vertical nanowire-based LEDs.

The efficiency of current commercial micro-LEDs decreases drastically with reducing dimensions. Current devices having lateral dimensions below 10 µm fall below 1% external quantum efficiency (EQE) Figure 1 [1, 2, 7], below the thresholds required for commercial AR applications.

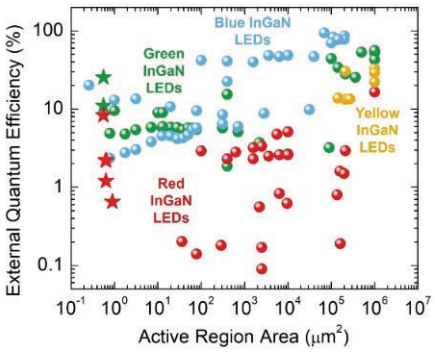

Figure 1. External quantum efficiency (EQE) for different active region areas with different emission wavelengths. The star data points mark efficiencies achieved for red and green submicron nanowire LEDs [1, 2, 7].

High nonradiative surface recombination resulting from damage induced by the plasma etching of conventional top-down MQW devices and degraded p-type contact due to plasma etching reduce their efficiency. InGaN based red micro-LEDs operating at longer wavelengths especially exhibit low internal quantum efficiency (IQE) due to a higher indium composition and the resulting extensive defect formation. These critical issues have been addressed by bottom-up growth of nanostructures eliminating the use of plasma etching of the device active region [3]. This growth method has previously resulted in nanowire-based micro-LED devices that demonstrated record EQE, marked by the red and green stars on Figure 1.

Much work has shown the building blocks of green and red-emitting InGaN devices, utilizing selective area growth, engineered photonic crystals, and in some cases core-shell designs [4, 5, 6]. All of these works rely on one or more methods of planarization of the nanowires before p-contacts can be applied to the LEDs, and this process step is of critical importance in creating high-yield nanoLEDs.

2. Results
In this work, we continue to show the building blocks of manufacturability of these unique nanowire LEDs. Previous work [7] highlighted the reliance on electron beam lithography (EBL) to make the patterns that are a requirement of the selective area growth technique, and how deep UV (DUV) lithography was emerging as an effective alternative to this approach. In this work, we focus on the need to insulate and planarize the nanowires prior to p-contact deposition, in order to make nanowire LEDs that are compatible with the scalability requirements of the display industry.

While even a single nanowire can operate as a complete LED, in most display applications the nanowire dimension (50-250nm) is smaller than the size of the desired sub-pixel size (1-10um). Hence, a sub-pixel nanowire LED contact must span many nanowires, contacting the p-GaN region of each, while being well-insulated from the rest of the nanowire structure, and underlying layers (mask layer, n-GaN, template layer). While this has been shown to work with free-standing contact materials [8] floating over the top of the nanowire array, for robust contact placement and subsequent annealing steps, the spaces between the nanowires must be filled in (insulated) to allow for physical vapor deposition (PVD) of the contact materials (ITO, Ni/Au). This planarization material must be able to withstand future process steps, and be optically transparent to the radiation of the LED, visibly transparent in the case of RGB displays.

An early solution to this problem relied on the liquid coating of polyimide materials [9]. While liquid coating techniques have the advantage of filling very high aspect ratio spaces quickly and easily, these organic materials are also limited in temperature budget, and hence contact materials cannot be annealed, or can be annealed only at lower temperatures

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resulting in increased contact resistance in these LEDs. For compatibility with this and many other downstream processes required by the display industry, a higher temperature material is required, typically an inorganic filling material.

Sputter deposition and plasma enhanced chemical vapor deposition (PECVD) are perhaps the most common means of applying conformal insulating thin films in manufacturing today, especially for high aspect ratio structures. PECVD deposited silicon nitride can indeed be used as a planarization layer for a nanowire LED. Alternatively, atomic layer deposition (ALD) can be used to deposit a variety of metal oxides, but most typically alumina (Al_2O_3). To study the differences between the planarization quality of oxides coated using these two methods, cross-sectional transmission electron microscopy (TEM) sampling was performed and the images analyzed.

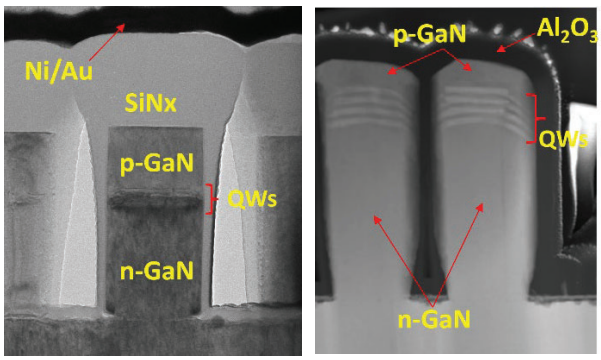

Figure 2. STEM-HAAD images of InGaN/GaN nanowires insulated by different materials and processes. Top image shows nanowire after nominal 300nm of SiNx deposition via PECVD. Bottom image shows two adjacent nanowires after nominal 60-nm Al_2O_3 deposition using atomic layer deposition (ALD) technique.

Figure 2 shows the cross-section TEM images from two different samples of nanowires as would be used in fabricating a nanowire LED. In Figure 2 (top), the planarization layer is SiN_x deposited by PECVD, while in Figure 2 (bottom) the planarization is Al_2O_3 deposited via ALD. The cross-sectional analysis shows the challenge in this planarization layer in general. Nanowires are much taller than they are wide, with a roughly 4:1 aspect ratio, but typically the spaces between the nanowires that must be filled are even narrower, with spacing that might be ~50nm wide, despite a ~700nm height. Furthermore, the nanowires are typically not perfectly straight-walled, with a wider gap at the bottom than at the top as can be seen clearly in Fig 2(bottom).

The shortcomings of deposition into this narrow gap are apparent from the cross-section (Fig 2 top). While SiN_x is deposited on all surfaces of the nanowire, the thickness of deposition at the bottom of the nanowires is much less than at the top, roughly 30nm versus the nominal deposition thickness of 300nm. This is due to the shadowing effect that the top of the nanowires provide over the high aspect ratio holes, preventing uniform deposition rates on all surfaces. The typical “mushroom top” is seen as a consequence of this effect. This very thin insulator with voids between the nanowires is a potential source of device shorting after fabrication, and during the long-term operation of the device.

In contrast, the ALD deposited alumina (Fig 2 bottom) forms a nearly perfect conformal coating on all surfaces of the nanowire, with near equal thickness on the mask layer at the base of the nanowire, on the nanowire sidewalls, and on the nanowire surface, with smooth corners and no visible gaps. This conformal insulation provides the basis for robust deposition of subsequent p-contact materials, with little means for p-contact shorting to other layers of the device.

3. Conclusions

It has been previously shown that the bottom-up growth of nanowire LEDs can be utilized to achieve the high efficiency small devices required for AR/VR headsets and other micro-displays, and that the problematic EBL step can be replaced by optical lithography at wafer scale. This work shows that in-fill and planarization, another unique requirement of nanowire LEDs, can be effectively achieved with existing industrial, scaled processes such as ALD. While much work will be required to scale this technology and transfer it into production, another of the main bottlenecks has herein been addressed.

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