Research on Key Technologies for Large Transparent MiniLED Display Devices

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Abstract

Conventional display technologies face significant challenges in achieving large-area transparent displays. For instance, while liquid crystal display (LCD) technology is well-established, its ability to attain high transparency is limited by the relatively thick film layers required for its operation. In contrast, Mini LED transparent displays, a promising emerging solution, leverage the advantages of Mini LED technology—such as high brightness, high contrast, and low power consumption—offering substantial potential for diverse market applications. Our aim is to develop a large-scale, modular transparent display using glass-based Mini LED technology combined with a compact integrated micro circuit (IC) driver solution. This product will be strategically positioned within the high-end commercial sector, particularly for large window glass displays, serving as an innovative medium for product presentation while providing consumers with an exceptional transparent visual experience.

Author Keywords

Mini LED direct display; Transparent display; Splicing display; Electroplating thick copper process.

1. Introduction

Mini LED display technology has evolved from LED lighting technology, driven by the ongoing miniaturization of LEDs initially designed for illumination. This advancement has enabled the integration of LEDs into the display industry. As a self-emissive display technology, Mini LED stands in contrast to traditional LCD technology. Compared to conventional LCDs, Mini LED displays offer significant advantages, including superior contrast ratios, higher luminous efficiency, and lower energy consumption. These characteristics underscore the considerable potential of Mini LED technology in the future of display applications.

The application of Mini LED technology in the display field is primarily concentrated in two main areas. The first is its use as a backlighting solution, where Mini LEDs replace conventional LED backlight modules in traditional LCD displays. This integration enables localized dimming, allowing for more precise control of light emission. When combined with LCD technology, Mini LED backlighting significantly enhances contrast ratios, improving black levels and overall image quality in comparison to traditional LED-lit LCD panels. Currently, most high-end television models on the market employ Mini LED backlighting technology, utilizing partitioned dimming to achieve superior display quality. Another key application of Mini LED technology is direct display; however, due to challenges such as the high yield rates required for successful technology transfer, direct Mini LED displays remain largely in the research and development phase. This paper proposes a glass-based Mini LED display solution, combined with a Mini IC driving scheme, to develop a large-scale, modular transparent display. The product is envisioned as a high-end commercial showcase, designed to function as an innovative display medium for businesses and retailers.

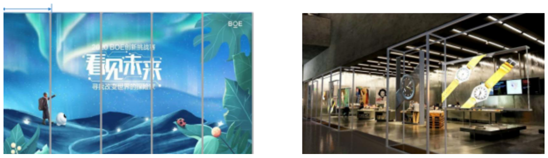

Figure 1. Product form simulation image

2. The design of display device

2.1 The optical simulation of Transparent display

Realize the automated optimal design function of multi membrane structures through gradient descent algorithm. The transparent film layer is composed of multiple layers of inorganic film layers overlapping each other. Due to the reflection between the interfaces of each film layer, adjusting the thickness of the film layer can make the phase difference between each interface meet half the wavelength, thus achieving the effect of interference cancellation transmission enhancement to increase transmittance; Adjust the thickness of each layer of SIN to increase transmittance based on the demand for transparent display. After software optimization, the maximum transmittance can reach 84.15%, but the project requires a transmittance of over 95% in the transparent area. Therefore, this paper chooses the solution of completely removing the transparent film layer, and only retaining the Glass transmittance can achieve 99%.

Table 1. Tr optimization of membrane structure

Layer	Ref-300/nm	Ref-200/nm	Split1/nm	Only Glass
OC2	2200	2200	2200	-
PVX3	180	180	180	-
PVX2	20	20	20	-
PVX2	80	80	100	-
OC1	9000	9000	9000	-
PVX1	150	150	237	-
Buf	300	200	200	-
BP simulation Tr	84.15%	82.35%	**83.44%** **(1.32%↑)**	> 99%

2.2 Transparent display pixel design

In pursuit of optimizing overall transmittance, a large-area hollow pixel architecture is employed. Excluding the metal routing and driver integrated circuit regions, the entire pixel area is engineered to be optically transparent. The RGB Mini LED array is strategically positioned above the ground (GND) metal layer, ensuring it does not occlude the transparent regions, thus preserving the light transmission pathway. This design yields an aperture ratio of 85%, thereby substantially enhancing optical transmittance and significantly improving the display's overall performance.

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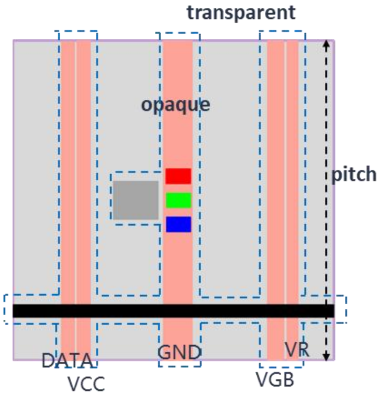


Figure 2. Transparent display pixel design

The following is the formula for calculating transmittance

$$T = \frac{S_{transparent}}{S_{pixel}} \times 99\%$$
$$= \left(1 - \frac{90 + 110 + 1300 + 60 + 155 + 50}{2834} - \frac{233 \times 275}{2834 \times 2834}\right) \times 99\%$$
$$= 84\%$$

3. Results and Discussion

3.1 Main process route design

To maximize the transmittance of the product, this paper outlines several critical design considerations in the process route. First, the transparent region of the pixel is configured with a hollow structure, where the organic and non-polar film layers are removed. This design ensures that the transmittance of the transparent area is primarily determined by the glass substrate. In the non-transparent regions, particular focus is placed on the metal traces. These long metal traces are plated with thick copper (greater than 7 μm in thickness), which not only satisfies the resistance requirements for cross-screen driving but also minimizes the width of the copper traces, thereby optimizing the overall transmittance of the product.

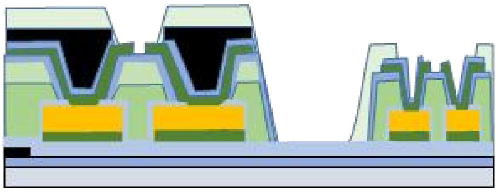


Figure 3. Cross sectional view of transparent display backplate

3.2Design to prevent metal routing

Due to the first copper (Cu) wiring layer exceeding a thickness of 7 μm, the likelihood of residual film layers after the deposition of this layer is substantially increased. The presence of residual organic layers can impair the transparency of the transparent regions, while residual metal routing layers may introduce a risk of short circuits within the circuit. To address these challenges in organic layer stacking, this study employs a misalignment strategy for the organic layers. In contrast to the conventional alignment design, the staggered arrangement reduces the vertical height discrepancy between adjacent segments, thereby minimizing the potential for residual material and mitigating the associated risks.

The specific design implementation is illustrated in the following figure.

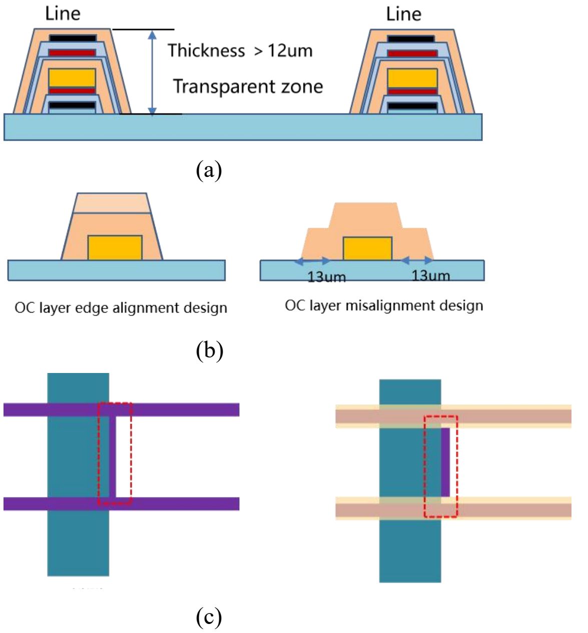


Figure4. (a) Schematic diagram of high section problems caused by thick copper wiring.(b)OC layer external expansion design section diagram.(c) Schematic diagram of OC layer external expansion design plan.

3.3 Glass warping issue

In order to reduce driving resistance, a Cu electroplating process with a thickness range of 7 to 10 μm was employed. However, the electroplating of a thick copper layer across the entire substrate surface can induce substantial warping, thereby increasing the risk of substrate fragmentation during subsequent processing. To mitigate this risk, a 0.7T thick glass substrate was selected to provide enhanced resistance to stress-induced deformation. Furthermore, a reverse stress compensation strategy was implemented, which involved the deposition of a reverse compressive stress layer (1500Å SiNx) to counterbalance the mechanical stress generated during the electroplating process. Warpage was quantitatively assessed using a plug gauge, and it was found that the electroplated substrate exhibited warpage of less than 2 mm, confirming that the substrate maintained adequate flatness and mechanical stability, ensuring its suitability for further processing.

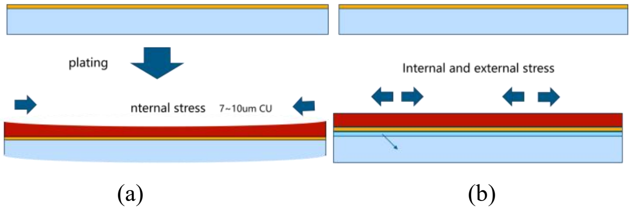


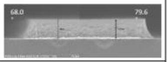
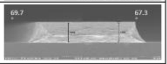
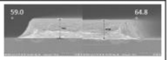
Figure5. Experimental diagram of substrate warping (a) Do not create a schematic diagram of reverse stress film layer,(b)Schematic diagram of reverse stress film layer production.

3.4 Electroplating thick copper process

A comprehensive evaluation of various etching protocols for electroplated copper thicknesses was conducted, leading to the conclusion that efficient etching of thick Cu can be reliably achieved within the thickness range of 7-12 μm. The etching duration was found to be adaptable within a range of 1000 to 1500 seconds, depending on the specific Cu thickness to be processed. Scanning electron microscopy (SEM) imaging reveals that the angular variation in the profiles of Cu traces, within the 7-12 μm thickness range, fluctuates between 60° and 80°, indicative of stable and reproducible etching characteristics.

Further assessments, utilizing optical microscopy, were performed on both the AA area (effective display area) and the Fanout region, which exhibits denser wiring patterns, to evaluate potential issues such as Cu trace breakage and residual material. The findings confirm that the optimized etching parameters result in high-quality, well-defined Cu traces, within the 7-12 μm thickness range, without notable defects or residue. This suggests that the established etching conditions are robust and suitable for producing precise Cu structures in advanced display applications.

Table 2. Verification of Cu etching process with different thicknesses

	THK/um	Etch time	DICD	FICD	CD Bias	Taper	SEM Check
1	7.83	1000s	167.8	142.9	24.9	73.8°	
2	8.45	1000s	166.2	145.2	21.0	58.4°	
3	11.8	1500s	167.8	134.7	33.1	68.5°	
4	12.1	1500s	167.2	127.6	39.6	61.9°	

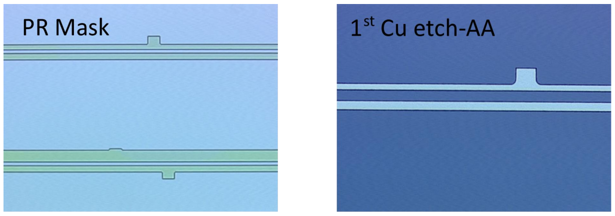


Figure 6. Display area and Fanout Cu post etching microscope photos

This study investigates the issue of organic layer residue caused by the use of high-thickness copper traces and further examines the residual organic film layer resulting from significant step differences in the copper traces. The results, as illustrated in Figure 7, show that when the exposure dose exceeds 200 mJ, residual organic material accumulates at the edges of the copper traces. In contrast, when the exposure dose is below 100 mJ, the problem of organic layer residue is effectively mitigated. The analysis primarily focuses on the negative photoresist employed in this process, with a proximity exposure system used for the exposure. At higher exposure doses, strong diffraction effects during exposure lead to residual photoresist at the step differences in the metal lines.

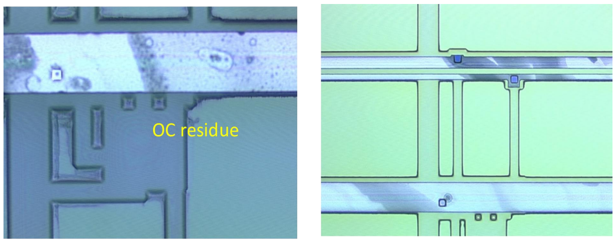


Figure 7. Microscopic photo of residual organic layer caused by high step difference

The second copper metal layer serves two primary functions: it establishes electrical connections between the first metal layer through openings in the organic layer, and it acts as a bonding pad for Mini LEDs and Micro ICs. Given the relatively short wiring distances, sputtering technology is employed to meet the resistance specifications of the design. To prevent oxidation of the metal pad layer, a Cu/CuNi stacked structure with a thickness of 9000/500Å is utilized. Additionally, the study explores the effects of various process parameters on copper residue and peeling. In particular, due to the residual copper traces at regions of high step differences in the organic layer (OC), an OC layer expansion design is introduced to address potential short-circuiting issues caused by copper residue. The experimental results also characterize the critical dimension (CD) bias in exposure, correlating it with different design line widths.

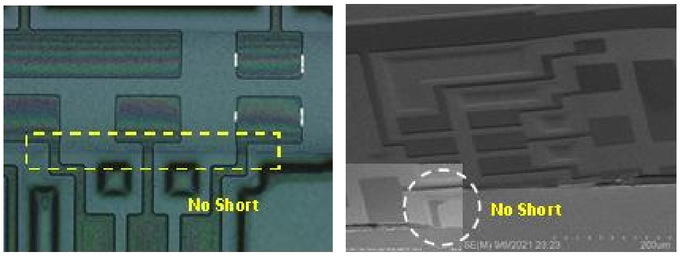


Figure 8. Cu residue and Peeling test microscope and SEM photos at the high level difference of metal wire routing

We studied the effect of coating organic layer OC thickness on copper wire widths with different designs. From the experimental results, it can be seen that the thickness of the organic layer formed across different width lines varies. For example, the VR Line metal Cu has a line width of 30um and an OC thickness of only 0.93um, while the GND Line has a line width of 190um and an OC thickness of 3.8um is formed on it. The reason for the analysis is that when the width of the lower layer wiring is insufficient, the organic adhesive is more likely to overflow during the post drying curing process, resulting in a decrease in thickness.

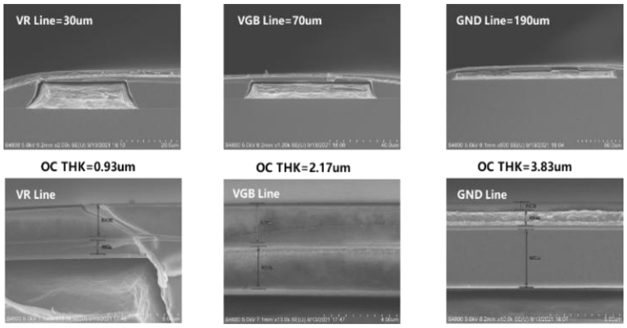


Figure 9. Thickness of photoresist on metal wiring with different designs

4. Conclusion

Through our efforts, we have finally achieved the illumination of transparent display samples, and the transmittance of the product can reach 84%. The following are actual photos taken after lighting, as shown on the display screen.

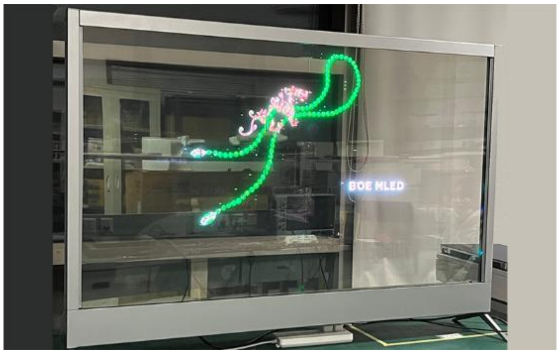


Figure 10. 65 inch demo

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