MicroLED in Series on a Single Chip for Display Performance Enhancement

Hugues Lebrun, Mickaël Mairy, Pierre Tchoulfian, Yoann Malier, Thomas Lacave, Ivan-Christophe Robin, Xavier Hugon, Philippe Gilet, Eric Butaud, Jerome Napiarela

Aledia, Champagnier, France

Abstract:

In the competition between OLED and microLED for direct view displays, the former has significantly improved the display performance by using Tandem OLED (TO) with TFT backplanes. The latter has to offer the same solution to the display manufacturers. The purpose of this paper is to demonstrate that the nanowires technology of Aledia can provide ultra small chips with several LEDs in series at no cost, both in single LED efficiency and on an economic point of view.

Keywords:

MicroLED displays; tandem structures; LED in series

1. Tandem OLED

WOLED or QDOLED TV or the latest version of high-end tablets with OLED displays are using TO to reduce the power consumption and to reduce the current density by increasing the operating voltage of the OLED stack. TO are made of a stack of OLED devices that are deposited on top of each other's as shown in Figure 1 for a WOLED display. In such a structure, the efficiency of the device in cd/A is strongly increased, therefore, the current density per layer for the same brightness is reduced which helps to improve the reliability of the product.

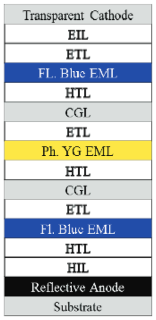

Figure 1. Three stack-WOLED for top emission from [1]

2. Impact of TO on power consumption

The other consequence of tandem architecture is to distribute power consumption in the driving TFT (Figure 2) over several devices instead of one. Table 1 shows the impact on power consumption of having 1 or 2 or 3 LEDs in series with the driving TFT in a pixel element. It is a well-known architecture in LCD backlighting units that helps to save a significant amount of power.

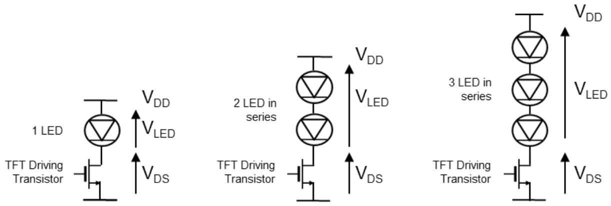

Figure 2: 1, 2 and 3 MicroLED in series with the driving TFT

Reducing the current with LED in series, is also beneficial in reducing the IR drops across the panel, thus reducing the constraint on metals resistivity in the power grids of the array.

VF (V)	VDS=1V	VDS=2V	VDS=3V
3	100%	100%	100%
6	88%	80%	75%
9	83%	73%	67%

Table 1: Relative power consumption of LED in series with the driving TFT at pixel level (VF: LEDs forward voltage, VDS: drain to source voltage of the driving TFT)

The objective of having several microLEDs in series is different from TO's one, that is, either to reduce the current density in the stack to improve the reliability of the OLED device or to increase the brightness at the same current density without any loss on reliability. In the MicroLED case, the primary purpose of having microLED in series per subpixel is not to reduce the current density which has a little impact on the reliability, but, regardless of the current density, to reduce significantly the power consumption in the display panel

3. MicroLED in series at pixel level

TO is equivalent to having microLEDs in series on the same chip. With 2D microLEDs, it can be achieved by on-chip splitting a microLED into two smaller ones with on-chip serial interconnection, to be, then, transferred on the TFT backplane like any microLED chip or by stacking the layers of the 2 LEDs on top of each other's.

Having 2D LEDs in series next to each other's, in the same chip size, would lead to an even smaller area per individual microLEDs, thus reducing their efficiency. Since saving on cost requires reducing the chip dimension continuously, having 2D LED in series on the same chip would lead to lower and lower efficiencies. Thus, the gain expected on power consumption is difficult to achieve and the solution leads to a dead end when the chip dimensions are further shrunk.

Stacking 2 LEDs on top of each other has 2 obvious drawbacks. First the processing time for epitaxy is multiplied at least by a factor of 1.5 to 2, leading to both a significant increase in the cost of the LED and to a reduction of the manufacturing capacity leading to further CAPEX to provide enough quantity for the display market (which is already a challenge today). Second, as described in [5], a tunnel junction (TJ) contact is needed between the nGaN of the bottom LED and the pGaN of the top LED of the stack. The TJ induces an increase of the forward voltage of the stack which partly compensates for the improvement on driving voltage described in section 2. TJ complexifies the epitaxial process. The increased thickness requires optimizing the strain management during the epitaxy of tandem LEDs. This is especially challenging for large-area substrates, where the increased wafer bow can drastically reduce the yield of subsequent processes. Realizing tunnel junctions (TJs) using metal organic chemical vapor deposition (MOCVD) is difficult due to delays in Mg incorporation and its memory effect [2, 3], which hinder the formation of a sharp interface between the Mg-doped and Si-doped layers. Additionally, the top n-GaN layer prevents hydrogen out-diffusion from the surface, making it hard to fully activate the p-GaN layer [4, 5]. The Mg memory effect can also poison the quantum well (QW) of the upper LED structure, impacting its internal quantum efficiency (IQE) and, consequently, the wall-plug efficiency (WPE).

Aledia's unique 3D nanowire technology demonstrated in [6] that each wire with 1µm diameter at a pitch of 5µm, is a microLED on its own with uniform performance. The core of the wire is the cathode while the shell is the anode. On a chip of 15x30µm^2, there are up to 18 wires as shown, for example, in Figure 3. On such a chip, it is possible to have from 2 sets of 9 wires in series up to 9 sets of 2 wires in series while keeping wires redundancy. It means that when one wire is dead in a pair of 2 wires in parallel, light can still be emitted and current can still be flowing in the remaining 3D device. With such a solution, the ability to have microLEDs in series is only limited by the number of wires. One can easily figures out that the ultimate chip dimension, at no loss in efficiency, is a chip of 5x10µm^2 with only 2 wires. There is niether epitaxy process changes nor processing time impact since the single nanowire structure is not modified, and therefore neither an impact on cost nor an impact on manufacturing capacity or CAPEX.

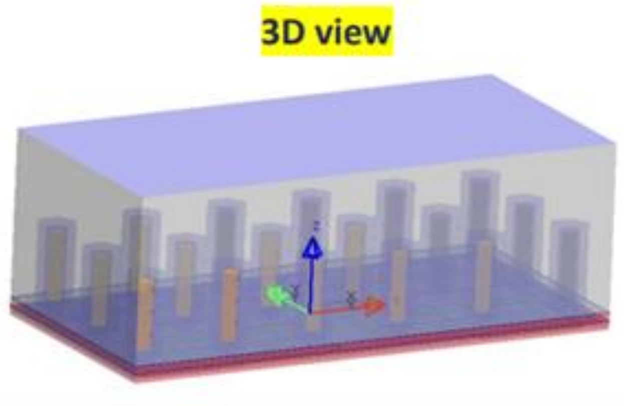

Figure 3: Aledia's 15x30µm^2 chip with 18 nanowires

4. MicroLED architecture

As shown in Figure 4, GaN nanowires are grown on a silicon wafer at a pitch of 5µm. Aledia is adding a transparent conducting oxide (TCO) on the front side or emitting side, an encapsulation layer and layers which are needed for the laser release of the device to the CoC1 (1st chip on carrier). The front side TCO is connected to the back side layers. Up to 2 metal layers and associated vias are then added on the backside of the chip to connect the wires together to build the high voltage architecture. The design rules are the submicron ones of the 200mm CMOS on silicon with 248 nm photolithography solutions.

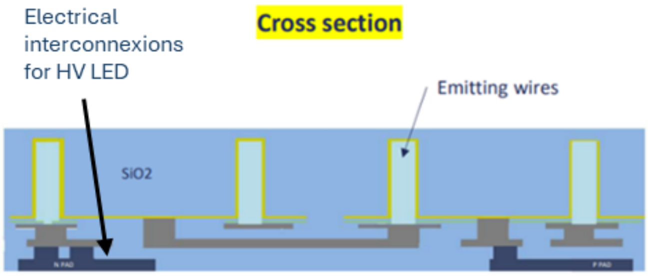

Figure 4: Cross section of the nanowires in series (not in scale)

5. Chip size, wires and redundancy

Aledia demonstrated in [6] that the nanowire technology enables the manufacturing of a single LED chip of 3.5x3.5µm^2 with one wire of 1µm and top-bottom contacts. Based on this solution and considering the ability to process the wiring on the back side of the LED, it is possible to consider chips made of an even number of wires as candidates for high voltage chips or chips with LED in series.

Table 2 is a relation between the number of wires per chip, the size of chip, the capability to have the LED in series, the redundancy built in the chip associated to the quantity of wires in parallel, depending on the architecture and the typical contact pad size and spacing as an indication (when pads are only on one side), although it should not be considered as a limitation, since as describe in [6], it is possible to implement a top/bottom contact structure. Figure 5a and 5b explains how wires are interconnected (electrical schematics) on an 18 wires chip to achieve either of 2 LED of 9 wires in series or 3 LED of 6 wires in series. With 2 LEDs in series on this chip, each LED has a redundancy of 9 nanowires. Thus, the probability of having a chip not emitting the light is very small. The more LED in series, the less efficient the redundancy. There is a trade-off between the reduction of the power consumption by having more and more LED in series, the high voltage capability of the TFT backplane to operate the LEDs at high voltage and the redundancy which is needed to achieve a very high yield.

The power supply to the LED array (VCC) can be calculated as the number of LED in series in each pixel time 3V plus VDS. For Example, with an 18 wires chip, with 9 LEDs or 2 wires in series and a VDS of 3V, VCC should be bigger than 30V (IR drops not included).

Quantity of wires	Chip size (µm^2)	LED in Series	Redun-dancy	Contact pads rule (µm)
2	3.5x8.5	2	None	2.5
4	8.5x8.5	2 4	2 None	3
6	8.5x13.5	2 3 6	3 2 None	4
8	8.5x18.5	2 4 8	4 2 8	5.5
12	13.5x18.5	2, 3, 4, 6, 12	6, 4, 3, 2, None	6
18	13.5x28.5	2 to 18	9 to None	9

Table 2: Chip design opportunities based on the nanowire solution of Aledia

Aledia's unique nanowire solution is paving the way to further reductions of the chip size without any loss in efficiency, depending on the integration capabilities on TFT of the display industry while offering significant improvement on power efficiency. At short term, the 15x30µm² chip with 18 wires is the solution which matches the design rules of the TFT.

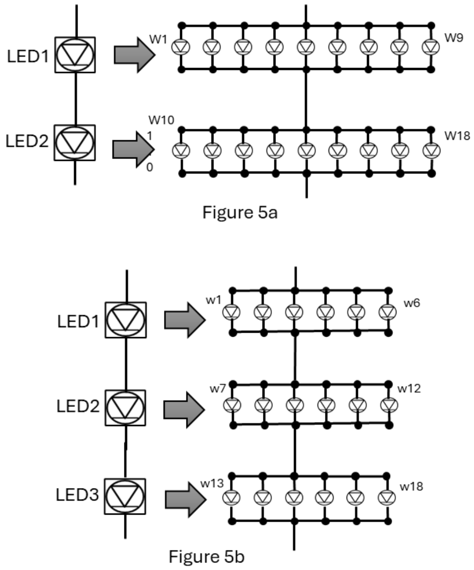

Figure 5a

Figure 5b

Figure 5 a&b: Wires connections on an 18 wires chip to achieve a 2 (Figure 5a) or 3 (Figure 5b) LEDs in series with redundancy (Wn stands for the wire number)

6. Process flow

Figure 6 shows the process flow up to the manufacturing of the CoC1 standard of the microLED transfer on TFT.

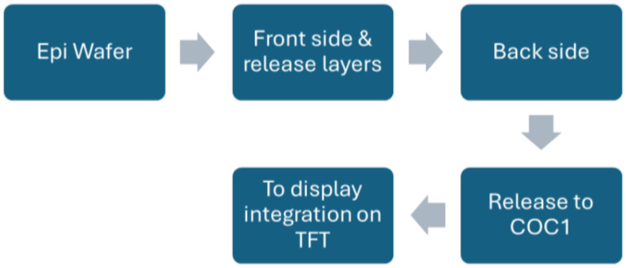

Figure 6: Process flow for nanowires in series at Aledia

At 1st, GaN wires are grown on silicon wafers by epitaxy as described in [6]. Wires are 1µm in diameter with a 5µm height.

During the front side operation, the transparent conductive oxide (yellow layer in Figure 4) is deposited on the anodes and structured. One should notice that the TCO reaches the floor of the chip which is almost the surface of the growth wafer. Then, the wires are coated with a passivation and encapsulation layers. The latter becomes the main bulk material of the LED. Final operation of the front side is the coating of the laser release materials and other materials that are needed for the transfer on a handler to enable the back side process.

At the back side process, metal layers and vias are added for the interconnexion of the anodes and cathodes of the LEDs, the mirror and the contact pads. Finally, a photolithographic step defines the trenches between the chips down to the handler. Chips are ready for the transfer to a CoC1 using a laser release solution.

7. High voltage chip performance

The latest results on the efficiency of the blue nanowires of Aledia are presented in Figure 7 a&b from paper [7]

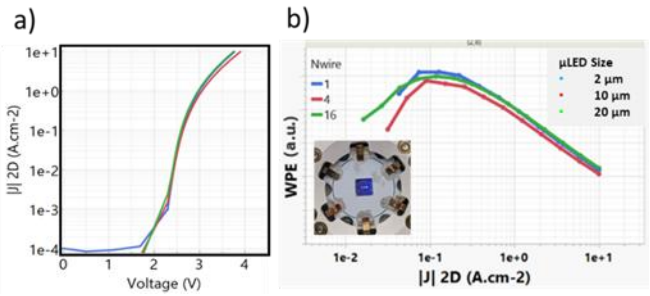

Figure 7 a&b: J(V) and EQE as a function of current density for different quantities of nanowires i.e. chip sizes.

Figures 7a&b show that, thanks to nanowire configuration, the efficiency of the LED does not change with the quantity of wires per chip, thus validating the longer-term road map that leads to smaller and smaller chips, matching the very strong expectation on cost reduction of the display industry.

As a result of this unique characteristic in the field of microLED, it is possible to compute the efficiency of high voltage µLED in cd/A to estimate the efficiency of a display panel as shown in Figure 8.

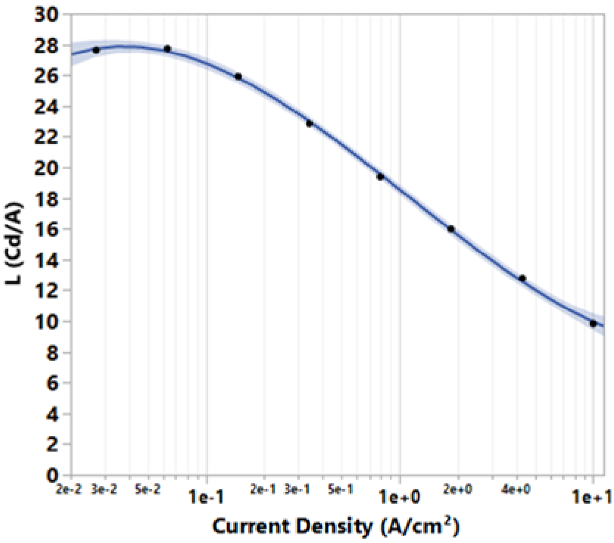

Figure 8: Brightness efficiency for 2 blue LEDs in series at 465nm.

8. Color conversion (chip level or panel level)

Color conversion is achieved at panel level after the transfer of the microLED to the TFT substrate by printing or on a remote glass or any other solution. The efficiency of the display depends on the efficiency of the coupling of the color conversion layers to the LED.

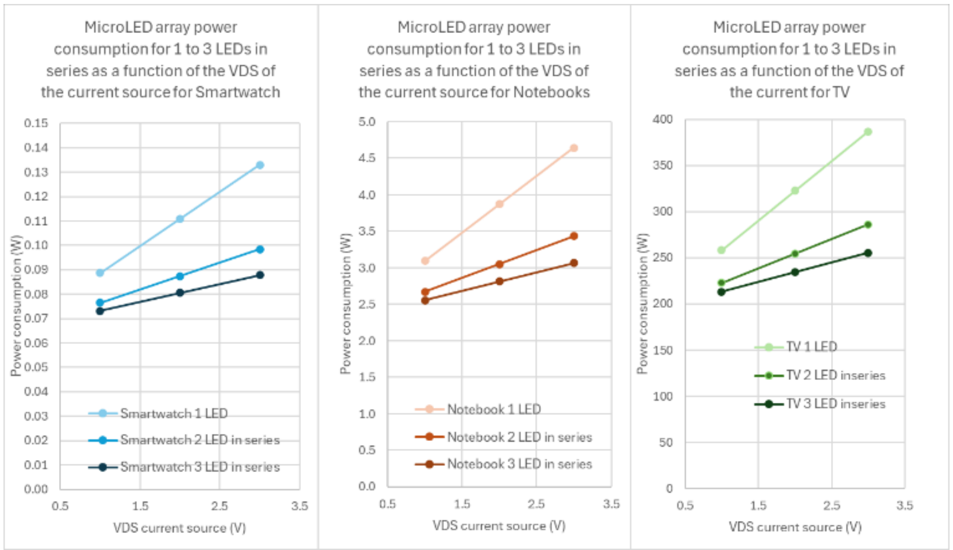

Figure 9: Power consumption for different TFT VDS on displays for Smartwatch, Notebooks or TV for 1 to 3 microLEDs in series per subpixel

Expected efficiency of 30x15µm² chip with an efficient color conversion are 35cd/A for red and 200cd/A for green with two blue LED in series

9. Impact on display power consumption

In Figure 9, the power consumption of the LED array, including the current source, is estimated for different voltage drops across the TFT used as a pixel current source (driving TFT) and for different display applications.

From one microLED per pixel to 2 microLEDs per pixel, the improvement in power consumption is in the range of 15% to 30% depending on the VDS of the current source, as expected. But from 2 devices per pixel to 3 devices per pixel, the gain decreases to 4% to 11%. The first step of having 2 microLEDs in series per pixel is already leading to significant improvement, not even considering the losses by IR drop in the power supplies along the array.

10. Conclusion

Aledia's unique high efficiency, high voltage microLED solution based on nanowires connected in series can be shrunk to the ultimate chip size that the TFT technology is able to handle today and in the coming years, while keeping performances at the same level and offering on chip redundancy. It is paving the way to the mass production of microLED displays.

References

[1] Young Kwan Jung &al, "3 Stacked Top Emitting White OLED for High Resolution OLED TV", SID Digest, vol47, issue1, P707-710, May 2016

[2] Y. Ohba, A. Hatano, "A study on strong memory effects for Mg doping in GaN metalorganic chemical vapor deposition", J. of Crys. Growth Volume 145, Issues 1–4, 2 December 1994, Pages 214-218.

[3] M. Bakhtiary-Noodeh, T. Detchprohm, R. D. Dupuis "Magnesium doping profile control in p-GaN layers grown by metalorganic chemical vapor deposition", J. of Crys. Growth Volume 602, 15 January 2023, 126962.

[4] Y. Kuwano, M. Kaga, T. Morita, K. Yamashita, K. Yagi, M. Iwaya, T. Takeuchi, S. Kamiyama, and I. Akasaki, "Lateral hydrogen diffusion at p-GaN layers in nitride-based light emitting diodes with tunnel junctions", Jpn. J. Appl. Phys. 52(8S), 08JK12 (2013).

[5] David Hwang1 & al, "Micro-light-emitting diodes with III–nitride tunnel junction contacts grown by metalorganic chemical vapor deposition", Appl. Phys. Express 11, 012102 (2018)

[6] I. C. Robin & al. "1µm Nanowire Based MicroLED Chips For Efficient and High Performance Smart Watch Displays", Proceedings of SID 2024 51.2 (2024).

[7] Ph. GILET & al CS Mantech , "Mass transfer of Efficient <5µm MicroLED Chips For Efficient and High Performance SmartWatch Displays