An Embedded DisplayPort 8.1Gbps RX PHY by Digital CDR with High ESD Capabilities at 12nm

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Abstract

A 12nm FinFET digital CDR for 8.1Gbps display interfaces is proposed, featuring a digital loop filter with >900% frequency range increment. It achieves low power (1.65pJ/bit) and compact size (23% of analog CDR). The design ensures robust ESD protection, passing HBM 8000V, MM 800V, CDM 1200V, and IEC Level 4.

Author Keywords

DisplayPort; Clock and Data Recovery (CDR); ESD; FinFET

1. Introduction

The increasing resolution and refresh rates in modern gaming monitors, notebooks, and automotive display systems have significantly elevated the data bandwidth requirements between the application processor (AP) and the timing controller (TCON) or TCON Embedded Driver (TED), with data rates reaching up to 8.1 Gbps per lane. To meet the rigorous demands of high-speed interfaces and complex image processing, integrated circuit (IC) technology has advanced to the 12nm FinFET process. From a device-level perspective, FinFET technology offers several advantages, including reduced power consumption, enhanced performance, and a smaller chip footprint, rendering it highly suitable for high-speed data transmission applications.

However, despite these benefits, two primary challenges persist in FinFET-based designs: increased design complexity and heightened susceptibility to electrostatic discharge (ESD). The stringent layout rules and design rule checks (DRC) mandated by FinFET processes complicate analog design optimization, as fully custom layouts are required, thereby lengthening the design cycle. Moreover, the thin gate oxide and metal layers inherent to FinFET devices exacerbate their vulnerability to ESD stress, raising significant reliability concerns for high-speed panel manufacturers, especially in scenarios where only minimal capacitance can be introduced by ESD protection devices.

To address these challenges, this paper presents a novel digital clock and data recovery (CDR) architecture that offers an alternative to traditional analog-based solutions. The proposed digital CDR architecture significantly reduces reliance on analog components, thereby mitigating design complexity and shortening the design cycle [1]. By transitioning from analog to digital circuitry, the proposed solution achieves low power consumption of 1.65 pJ/bit and a die size reduction to 23% of its analog counterpart. Furthermore, a novel digital loop filter is incorporated, which broadens the limited frequency acquisition range typically associated with conventional phase detectors, resulting in a measured frequency capture range increase exceeding 900%. Additionally, an advanced ESD protection strategy is introduced to enhance the design's robustness against ESD stress, ensuring reliable performance in high-speed interface applications.

2. Proposed Digital CDR

The conventional analog clock-data recovery (CDR) circuit, shown in Fig. 1(a), employs a non-linear phase detector (PD) for multi-GHz operation. To reduce the PD's operating frequency, a half-rate architecture is often adopted, wherein the PD's clock rate is only half of the incoming data rate. However, this non-linear PD typically provides only phase lead or lag information without precisely quantifying the phase error, thereby limiting the frequency capture range of the CDR loop. To overcome this limitation, a separate frequency tracking loop is commonly utilized. Initially, the voltage-controlled oscillator (VCO) frequency is tuned to approximate half of the incoming data frequency using a phase-locked loop (PLL) with an external reference source, such as a crystal or a less-accurate oscillator. Once the VCO frequency converges sufficiently, control transitions to the phase tracking loop, allowing the PD to drive the charge pump. The VCO continuously adjusts its frequency and phase based on the detected phase difference between the input data and the recovered clock. An RC loop filter is employed to suppress charge pump noise and ensure loop stability.

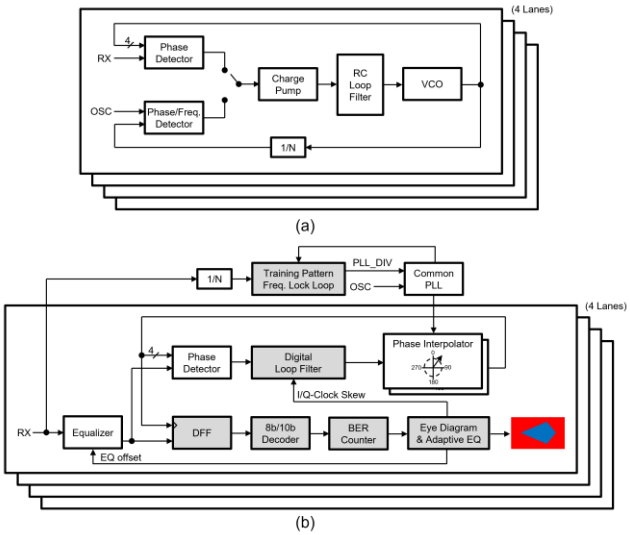

Figure 1. The traditional analog CDR block diagram (a), and the proposed digital CDR block diagram (b), in which all modules in grey color were implemented by the standard digital auto-place-and-route design flow.

While this analog CDR design achieves wide loop bandwidth and is well-suited for multi-GHz applications, it presents several design challenges. A robust analog CDR implementation requires precise current matching in the charge pump and carefully tuned resistor and capacitor values in the RC loop filter. Additionally, the VCO is highly sensitive to power supply fluctuations and substrate noise, requiring meticulous layout design and strict fabrication process control. These complexities are further exacerbated in high-speed applications, such as embedded DisplayPort, where multiple lanes are required. The presence of multiple lanes introduces crosstalk, which further degrades the

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performance of analog CDRs. Moreover, the large silicon area required by the RC loop filter and inherent process, voltage, and temperature (PVT) variations pose additional challenges. As process nodes continue to scale down, analog circuits do not scale proportionally in terms of die size or supply voltage, necessitating alternative approaches.

Digital clock-data recovery circuits offer a compelling alternative by leveraging fully digital components for CDR functionality. These designs typically oversample the incoming data and utilize digital circuitry to extract phase and frequency information, providing greater robustness against noise and PVT variations [2][3]. However, oversampling-based designs impose inherent limitations, confining conventional digital CDRs to low-to-medium-speed applications.

The proposed digital CDR, depicted in Fig. 1(b), addresses these limitations, and supports multi-GHz data rates comparable to analog CDRs. This design employs the same half-rate PD as in analog CDRs, eliminating the need for a higher clock rate required by oversampling techniques. To overcome the challenges inherent in analog designs, the charge pump, RC loop filter, and VCO are replaced by a digital loop filter and a digitally controlled phase interpolator. The proposed architecture leverages an existing common PLL that provides a four-phase clock, which feeds the phase interpolator circuit. The digital loop filter controls the phase interpolator's output clock phase based on the detected phase difference, enabling precise phase tracking. This digitally controlled phase interpolator generates a recovered clock that accurately tracks the incoming data.

Unlike other digital CDR solutions that require fully custom layouts for high-speed digital circuits, the proposed design retains the half-rate architecture. All modules highlighted with a gray background in Fig. 1(b) are implemented using a standard digital auto-place-and-route design flow, ensuring scalability and design efficiency. Due to the inherent capability of digital circuits to execute complex operations with minimal power consumption and reduced chip area, several additional digital modules have been incorporated to further enhance the overall system performance.

Most serial link protocols incorporate a training sequence during which the transceiver transmits a clock-like pattern, allowing the receiver to estimate the data rate of subsequent transmissions. A novel digital frequency-lock loop (FLL) has been introduced in the proposed design to utilize this training pattern for frequency calibration. The FLL uses the PLL clock to count a divided version of the incoming data. When the counter value exceeds a predefined target, the PLL feedback divider value is decreased to reduce the PLL clock speed. Conversely, if the counter value is below the target, the PLL feedback divider value is increased to speed up the PLL clock. This adaptive mechanism enables the FLL to adjust the PLL clock speed to within 1% of the incoming data rate, by setting the target counter value greater than 256.

In addition to CDR functionality, the proposed design integrates a channel decoder and a bit-error ratio (BER) counter to facilitate real-time link quality analysis. Another digital module is introduced to perform eye diagram analysis and adaptive equalization tuning, providing an efficient mechanism for link quality assessment and optimization. This comprehensive digital solution not only enhances link reliability but also ensures compatibility with modern high-speed interface standards.

Digital Loop Filter: As previously discussed, the bang-bang phase detector (PD) inherently suffers from a limited frequency capture range. In conventional analog CDR designs, this limitation is typically addressed by incorporating an additional frequency tracking loop. In contrast, our proposed digital CDR design introduces a novel digital loop filter that addresses this issue without increasing the sampling clock rate. The block diagram of the proposed digital loop filter is shown in Fig. 2. This digital loop filter features three key modules that distinguish it from conventional designs: (1) a biased voter, (2) a frequency hopper, and (3) an I/Q clock skew module.

The phase error output from the phase detector is processed through two distinct paths: a proportional path and an integral path. In the integral path, prior to the gain stage, a biased voter is introduced. This module converts the phase error into a binary output (+1 or −1). The voter employs two threshold values, THP and THN, which determine its transfer function, as illustrated in Fig. 2. When THP is set higher than THN, assuming a uniform phase error distribution, the voter output tends to have more negative values than positive ones, resulting in a gradual frequency drift in the phase interpolator output. This controlled drift, combined with the initial frequency setting provided by the frequency hopper, enables the digital loop filter to extend the frequency capture range of the bang-bang PD, thereby enhancing the overall CDR performance.

Additionally, the I/Q clock skew module at the output of the digital loop filter introduces a phase offset between the in-phase (I) clock signals at 0° and 180°, and the quadrature (Q) clock signals at 90° and 270°. This intentional skew facilitates on-line eye diagram monitoring and adaptive equalization tuning functionality, which will be elaborated upon in subsequent sections.

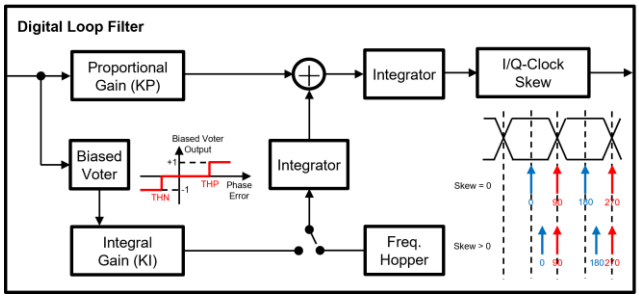

Figure 2. Block diagram of the proposed digital loop filter, which increases the frequency acquisition range without higher sampling rate and incorporates on-line eye diagram monitoring and adaptive equalization tuning.

Eye Diagram and Adaptive Equalization Circuit: In many high-speed serial link applications, link quality analysis heavily depends on the use of expensive instruments, such as ultra-high-sample-rate oscilloscopes, to reconstruct the eye diagram of the received data. However, even with such equipment, significant challenges remain. Due to the multi-GHz operating speed of modern high-speed interfaces, it is extremely difficult to access internal signals within the chip. Accurate measurement of these high-speed signals typically requires specialized low-capacitance active probes, further complicating the process. To address these challenges, our digital CDR incorporates an embedded eye diagram monitor, eliminating the need for costly external instruments. The proposed eye diagram monitor is shown in Fig. 1(b) as part of the overall digital CDR architecture.

The embedded eye diagram monitor is enabled by adding an additional stage to the digital loop filter after the phase gain integrator. This stage introduces a phase offset to the integrator

outputs, thereby generating intentional delays in the phase interpolator's output clocks. When different offsets are applied to the I-clock (0°, 180°) and Q-clock (90°, 270°), the relative phase between the I/Q clocks deviates from the ideal 90°, as illustrated in Fig. 2. The bang-bang phase detector operates by positioning the Q-clock close to the data transition edges once the CDR loop has settled, while the I-clock is used to latch the recovered data. As the I-clock moves away from the center of the data eye, incorrect data latching may occur, resulting in bit errors. By monitoring the bit error ratio (BER), which is also implemented as an integral part of our design, the eye width can be accurately estimated.

For eye height measurement, we leverage the existing offset cancellation circuit within the continuous-time linear equalizer (CTLE). By adjusting the CTLE offset voltage, the slicing level in the phase detector is effectively shifted. As the slicing level approaches the eye-opening height, an increase in the BER indicates the internal eye height. The proposed design includes a fully autonomous eye diagram monitoring circuit that performs a two-dimensional sweep across both I/Q clock skew and CTLE offset while the digital CDR remains in normal operation. Upon completion of the sweep, the resulting eye diagram is stored in on-chip memory and can be retrieved for link quality analysis.

In addition to its eye diagram monitoring capability, the embedded circuit also supports adaptive CTLE tuning. For a given link condition, the circuit performs a sweep across different CTLE settings while simultaneously monitoring eye width and eye height. Once the sweep is complete, the optimal CTLE setting corresponding to the maximum eye width or eye height is selected, significantly reducing firmware development effort and improving overall system robustness.

ESD Protection Scheme: The ESD floorplan is arranged such as to place Power/Ground Pads (VDD08/VSS08) between signal pads (RXP/RXN) to minimize impedance from pin to power/ground. The target specification is to maintain under 0.1 ohm for each path. P-diodes and N-diodes are implemented to provide ESD protection for the RX pin.

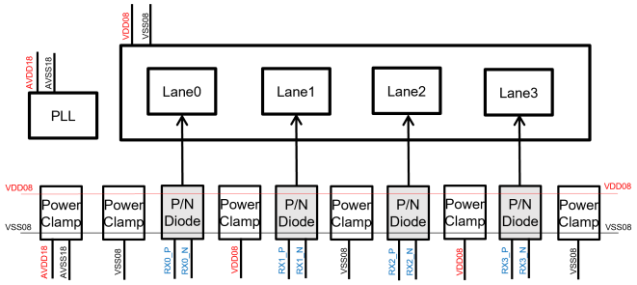

Figure 3. Floorplan of ESD protection circuit

The ESD discharge path from pin to power/ground is highly sensitive to uniformity. To prevent damage, current density must remain below IT2 as defined by foundry specifications; exceeding this threshold may result in damage to metal or via structures [4].

To address this, we propose using specialized power via placement to uniformly distribute ESD charge. The ESD current path from A to B is to allow max discharge capability.

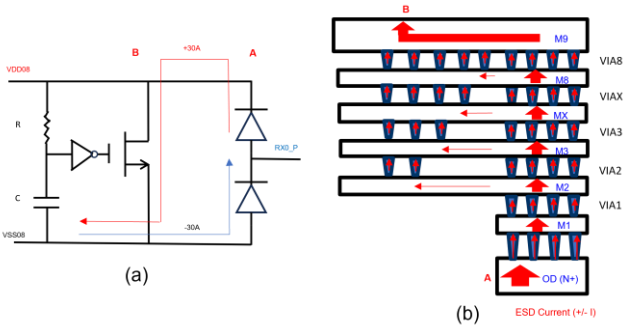

Figure 4. The ESD discharge current path

Per foundry Transmission Line Pulse (TLP) data, the Diode Junction Perimeter (PJ) size is proportional to Second Breakdown Trigger Current (IT2) current. If we choose PJ=200um, the max IT2 is 3A. To pass IEC 61000-4-2 ESD level 4 criteria, the P/D diode PJ need to be enlarged to 2000um. This kind of diode area will enlarge input capacitance and can't be accepted for 8.1Gbps speed. By adopting new power via placement technology and carefully arranged Power / Ground PADs , we can use only half of PJ (1000um) to meet IEC 61000-4-2 ESD level 4 criteria [5] and keep RX 8.1Gbps at LQFP package.

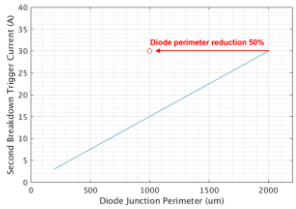

Figure 5. ESD capability (IT2) vs diode junction perimeter (PJ)

3. Experimental Results

The proposed digital CDR was fabricated in TSMC 12nm FinFET process. The die photo and mask layout are presented in Fig. 6. The area of the digital CDR measures 170 µm × 139 µm. Operating at a data rate of 8.1 Gbps, the digital CDR demonstrates power consumption of 13.38 mW. Fig. 7 provides a comparison between the proposed digital CDR and conventional analog CDRs implemented in various process nodes. The proposed digital CDR achieves a significant area reduction of 77% and a power reduction of 37%, underscoring the benefits of transitioning from analog to digital design.

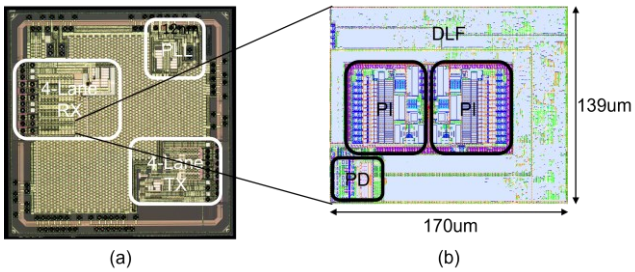

Figure 6. Die photo of the prototype chip (a) and the enlarged mask view with annotated sub-module (b)

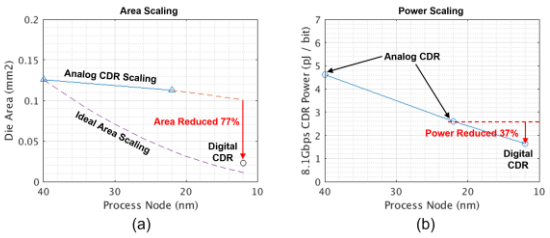

Figure 7. Comparison of analog CDR and digital CDR in area (a) and power consumption (b)

The frequency acquisition range of the proposed digital CDR is illustrated in Fig. 8. When the biased voter module is disabled, the CDR locks within ±1% of the incoming data frequency. Upon enabling the biased voter, the negative offset frequency range increases by over 900%, a substantial improvement in frequency capture capability. This expansion in the frequency acquisition range is constrained by the operating limits of the phase interpolator rather than the phase detector itself, further validating the effectiveness of the proposed digital loop filter in enhancing frequency acquisition performance.

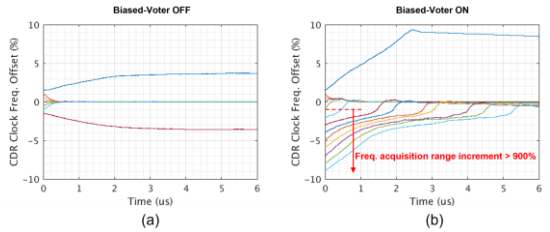

Figure 8. Frequency acquisition range comparison of the proposed digital CDR when biased voter is OFF (a) and ON (b)

The measured eye diagram of the recovered data is shown in Fig. 9. The eye width is approximately 713 mUI, indicating robust data recovery performance. Fig. 10(a) presents the measured jitter tolerance of the digital CDR, confirming its ability to maintain stable operation under varying jitter conditions. Fig. 10(b) depicts the results obtained from the embedded eye diagram monitor, revealing an eye width of 0.49 UI, which closely aligns with the measured jitter tolerance at a jitter frequency of 10 MHz.

The prototype chip was validated by operation as a repeater in a 4K 144 Hz monitor setup. The digital CDR successfully handled a total data rate of 32.4 Gbps when connected to a PC VGA card, underscoring its suitability for high-speed, high-resolution display applications.

4. Conclusion

This work presents a digital clock-data recovery (CDR) architecture with a novel digital loop filter and integrated high-reliability electrostatic discharge (ESD) protection. Key contributions include:

- A new digital CDR design is introduced, featuring over 900% increase in frequency acquisition range without raising the sampling rate.
- The digital CDR achieves significant area and power savings, occupying only 23% of the area of conventional analog CDRs and achieving energy efficiency of 1.65 pJ/bit while providing consistent multi-lane performance.
- A high-reliability ESD protection scheme optimized for the 12nm FinFET process is proposed, passing Human Body Model (HBM) tests at 8000 V, Machine Model (MM) tests at 800 V, Charged Device Model (CDM) tests at 1200 V, and IEC 61000-4-2 ESD Level 4.
- A prototype IC integrating receiver and transmitter PHYs was fabricated using the TSMC 12nm FinFET process. It was demonstrated as a repeater in a 4K 144 Hz monitor setup interfacing with a PC VGA card, achieving a total data rate of 32.4 Gbps.

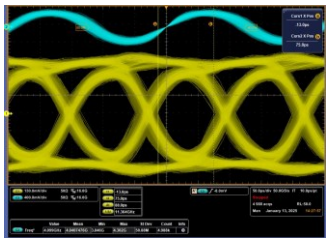

Figure 9. Recovered clock and data eye diagram at 8.1 Gbps

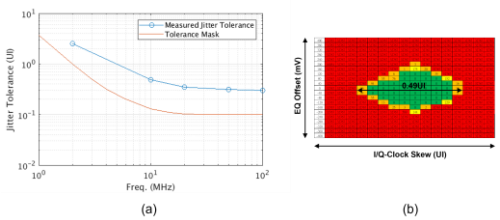

Figure 10. Measured jitter tolerance of the prototype chip (a) and the result of on-line eye diagram (b)

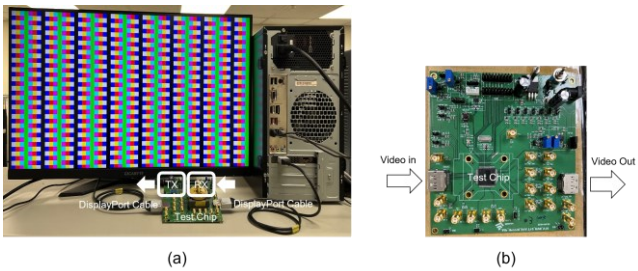

Figure 8. The demonstration system

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