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0.26-in. LED Microdisplay Using Pixel Level Cu-Cu Connections of Transferred GaN/Si and CMOS Backplane Wafer

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Abstract

We developed an integration process for LED microdisplays and present the first demonstration of a blue-color active-matrix LED microdisplay fabricated with this process. This process consists of Cu-Cu hybridization to connect heterogeneous materials; a die-to-silicon transferred GaN/Si wafer and a CMOS backplane wafer, followed by LED mesas and on-chip lenses fabrication. We report the key features and results of this process, and present a prototype of 0.26-inch, 5644-ppi LED microdisplay.

Author Keywords

microLED; microdisplay; active matrix; Cu-Cu hybridization; augmented reality

1. Introduction

Applications of augmented reality (AR) technology in various fields are being studied. As the volume of their markets expands rapidly, the development of AR glasses and their key components, including optical combiners and microdisplays, has gained significant attention. Among the various types of combiners, diffraction-based waveguides offer advantages owing to their properties such as lightweight, compact form factor, and large eye-box, compared with free-space combiners [1,2]. However, diffraction-based waveguides typically suffer from low optical efficiency of less than 2% [3]. Therefore, microdisplays for AR applications must provide a high luminance exceeding 1 million cd/m^2 to ensure sufficient visibility of images in outdoor environments. Furthermore, the small in-coupler optics used for waveguides require compact panel sizes and precise angular control of emitted light [2].

Inorganic LEDs possess attractive properties such as high brightness, energy efficiency and long lifetime. Hence, LEDs have been widely utilized for decades in applications ranging from general lighting and traffic signals to backlights for LCDs. In terms of display applications, a scalable display system using microLEDs as pixels had been commercialized [4]. Among microdisplays including OLED, LCoS, DLP and LBS, a microLED-based microdisplay (referred to as LED microdisplay) is considered the most promising device for meeting the stringent requirements for AR applications [5,6]. As an LED microdisplay is an emissive device, it has a small form-factor. Moreover, it features exceptionally high luminance and a long lifetime, which are not achieved by other emissive microdisplays such as OLED [5]. Foundational research on LED microdisplays has been reported [7,8], and recent efforts have focused on their development for commercial mass production [9].

One of the primary manufacturing challenges in realizing LED microdisplays for AR applications is the development of a process that enables pixel-level connections at a fine pitch. An LED microdisplay consists of a microLED array and a Si backplane connected at pixel level. Therefore, achieving a fine pixel pitch requires pixel-level bonding technology of heterogeneous materials with high accuracy and yield. Although chip-level flip-chip bonding has been used as an existing technology [7,10,11], it is considered impractical for achieving pixel pitches below 10 μm, owing to constraints in alignment accuracy and yield [12,13].

Wafer-level bonding is regarded as a promising approach to achieve further reductions in pixel pitch. A contact pitch of less than 1 μm has been demonstrated using wafer-level Cu-Cu hybridization [14]. However, bonding a III-V compound semiconductor wafer to a Si wafer arises a manufacturing challenge due to differences in wafer sizes. Currently, the available size of III-V wafers for LEDs is smaller than that of Si CMOS backplane wafers, limiting the use of Si CMOS production tools and facilities. Additionally, this discrepancy in wafer sizes leads to increased costs because of the presence of a certain amount of unused area on the Si backplane wafer [12].

To address this challenge, we employed a die-to-silicon process to transfer GaN chips onto a support Si wafer with the same diameter as the CMOS wafer. This GaN reconstitution process enables novel Cu-Cu hybridization regardless of the original size of the GaN on Si wafer, followed by the fabrication of microLED mesas and OCLs in the Si CMOS facilities.

This study presents the key features of this process flow and reports the electrical and optical characteristics of the microLED array with OCLs. Using this technology, we have developed the prototype of a 0.26-inch, 1080 × 960-pixels, 5644-ppi, which corresponds to 4.5-μm pixel pitch, LED microdisplay as shown in Figs. 1 and 2. This is the first demonstration of a blue mono-color active-matrix LED microdisplay fabricated with this process methodology.

Figure 1. Photograph of the 0.26-inch, 1080 × 960-pixles, 5644-ppi LED microdisplay

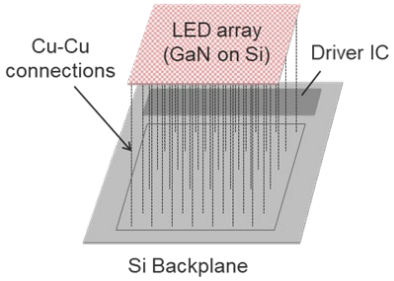

Figure 2. Schematic of the prototype

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2. Integration Process for LED Microdisplays

Figure 3 shows a schematic of the integration process for the LED microdisplay developed in this study. We had originally developed this integration process for a back-illuminated InGaAs image sensor with an InGaAs/InP die-to-silicon wafer and Cu-Cu bonding and achieved the first global mass production [15]. In such integration of III-V and Si materials, we generally struggle with many challenges such as mechanical stress, peeling, and damage caused by differences in the thermal expansion coefficients of III-V and Si materials.

For microLED applications, these challenges have been overcome by leveraging our III-V die-to-silicon technology, in which epitaxial GaN on Si wafers are diced into chips and transferred to a larger-diameter Si support wafer. The III-V die-to-silicon process solves inconsistency caused by the difference of GaN and Si wafer sizes and enables a larger-diameter CMOS image sensor wafer process with production-capable tools and facilities including leading-edge Cu-Cu hybridization. Furthermore, known good die screening has been successfully performed before transferring the diced GaN chips.

Back-end-of-line patterns are fabricated on the GaN chip areas of the GaN/Si heterogeneous wafer. After Cu pads are formed, the GaN/Si heterogeneous wafer is hybridized to the backplane using Cu-Cu bonding which connects each GaN mesa to a pixel circuit in the backplane. Following hybridization, the support wafer is removed to expose the GaN epitaxial layer to pattern the LED mesa array and OCL on top of each mesa. Figure 4 shows cumulative plots of the contact resistance for 100,000 Cu-Cu chain test element groups (TEGs). Functional electrical connections with resistance less than 2 Ω per unit in 100,000 connections were verified across all dies on the wafer (out of 24 measured points for each of the TEGs), demonstrating a 100% yield of Cu-Cu connections with pitches of 3.8 µm and 4.5 µm between the transferred GaN/Si wafer and the CMOS backplane wafer with multiple metal layers. The measured resistance is sufficiently small to suppress the voltage drop for pixel currents typically ranging from a few hundred nA to several µA. Figures 5 and 6 respectively show SEM images of the device cross-section after mesa and OCL formation. The finely tapered mesa structure, with a feature size of 1.2 µm, and the OCL structure were successfully patterned, enabling high LEE.

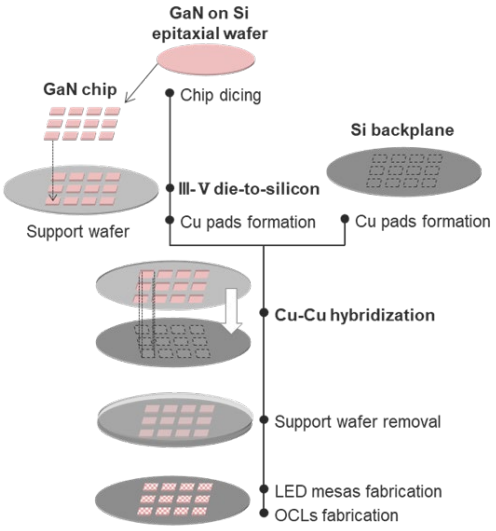

Figure 3. Process architecture of LED Microdisplays

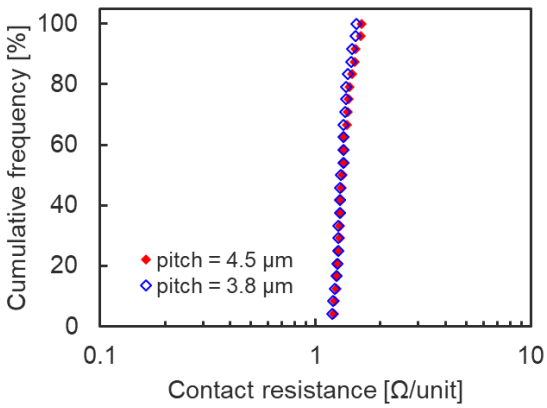

Figure 4. Cumulative plots of Cu-Cu contact chain resistance, with each module having 100k connections

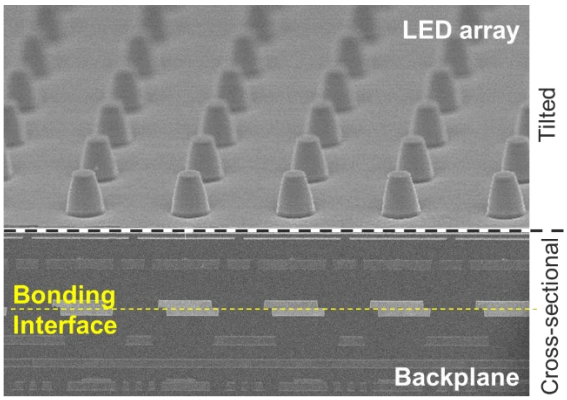

Figure 5. SEM images of the LED mesa array (Tilted view) and the bonding interface (Cross-sectional)

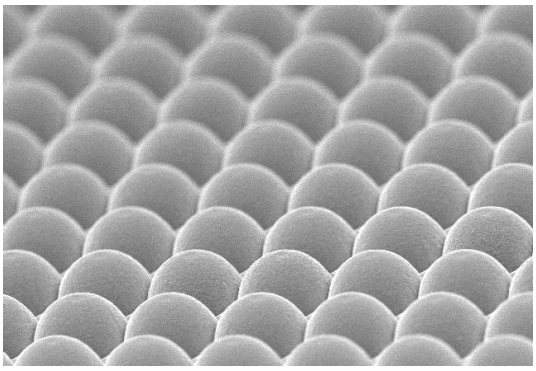

Figure 6. SEM image of the OCLs

3. Performance of the MicroLED Array with OCL

Figure 7(a) illustrates a schematic cross-sectional view of the microLED structure investigated in this study. Each LED mesa is connected to a pixel circuit in the backplane via Cu-Cu hybridization, and an OCL is formed on the top of each mesa. Figure 7(b) is a three-dimensional finite-difference time-domain (3D-FDTD) optical simulation of LEE dependency within an emission angle of ±12° in the normal direction on the ratio of the lens diameter to the mesa diameter. The results indicate that an increase in the ratio leads to a higher LEE. Due to a limited coupling angle of an AR optics, only narrow-angle components of the top-emitting light are coupled into the AR optics. Consequently, controlling light distribution through the OCL is important for enhancing the overall efficiency of the AR optical system. The light source positioned at the focal point of a OCL is collimated in the normal direction. Therefore, a smaller LED mesa diameter leads to a narrower light distribution pattern.

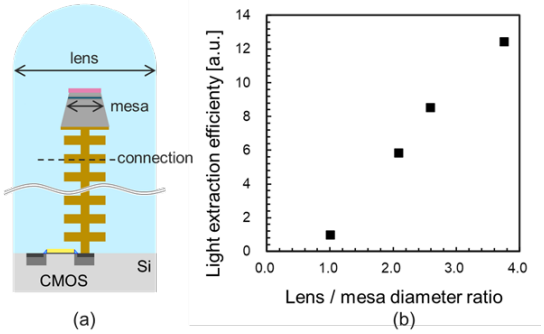

Figure 7.(a) Schematic cross-section of microLED **(b)** LEE dependency within the emission angle of ±12° in the normal direction (3D-FDTD simulation)

Figure 8(a) shows the far-field pattern (FFP) of the LED array with a 1.2-μm mesa diameter and a 4.5-μm pitch. The half-width at half-maximum of the FFP was 14°, indicating a narrow light collection angle. Figure 8(b) shows the light collection efficiency from 0° to a specific angle. Since the light distribution characteristics without OCL are approximately Lambertian light distribution, a collection factor is defined as the ratio of the collection efficiency to that of Lambertian light distribution. With the OCL, the collection factor was enhanced to 6.6 times at ±12°, 5.8 times at ±15°, and 4.2 times at ±20°.

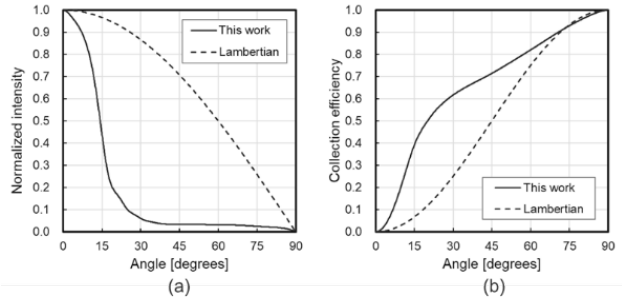

Figure 8.(a) Measured FFP of the LED array with1.2-μm diameter and 4.5-μm pixel pitch **(b)** Collection efficiency calculated from the FFP

Figure 9 shows the external quantum efficiency (EQE) of the prototyped device with a 1.2-μm mesa diameter and a 4.5-μm pixel pitch. The maximum EQE value of 1.06% was achieved at ±12° with a current density of 16 A/cm^2.

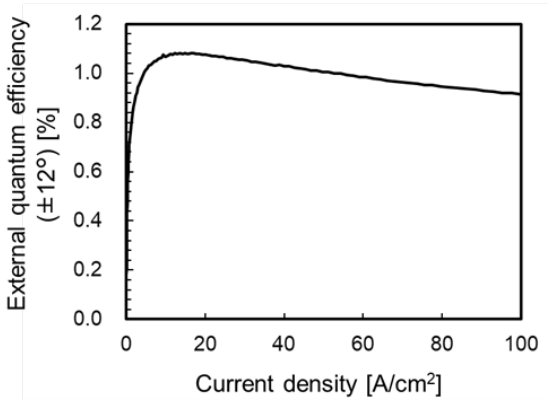

Figure 9. Measured EQE of the LED array with 1.2-μm mesa diameter and 4.5-μm pixel pitch

A small form factor is vital for AR glass applications, necessitating a reduction in the pixel pitch of microLEDs. To maintain a high LEE at narrower pixel pitches, further reduction of the mesa diameter becomes critical. Our process, being fully compatible with Si CMOS facilities, is anticipated to enable further reduction of the mesa diameter, thereby ensuring the maintenance of high LEE even for microLEDs with narrower pixel pitches.

4. Prototype of the LED Microdisplay

We have developed a prototype of the LED microdisplay, which is the first demonstration of a blue mono-color active-matrix LED microdisplay fabricated through the process which is described in previous sections. The prototype features 0.26-inch display with a resolution of 1080×960 and a pixel density of 5644-ppi, which corresponds to 4.5-μm pixel pitch.

After completing the wafer process, the wafer is diced into individual chips, and a driver IC chip is mounted onto each chip. The block diagram and the specifications of this panel are shown in Fig. 10 and Table. 1, respectively. All circuit and system blocks required for the LED microdisplay are integrated into the pixel and driver IC chips. The pixel chip comprises pixel circuits and a vertical scan driver, whereas the driver IC chip comprises a MIPI interface, a timing controller (T-CON), RAM and a horizontal scan driver.

Pixel-level uniformity compensation (referred to as Demura), along with current-driving pixel circuits, is implemented in the backplane to eliminate electrical and optical variations of GaN on Si LED mesas. After the panel fabrication, pixel-level luminance measurement was conducted for each panel module, and the compensation data was subsequently stored in the module.

The 1.2-μm diameter LED mesa array with OCLs reached 400,000 cd/m^2 at 100×100-pixel pattern, corresponding to a blue component of over 1 million cd/m^2 in white. The contrast ratio exceeded 1,000,000:1. As discussed in the previous section, Cu-Cu chain TEGs (shown in Fig. 4) demonstrated sufficiently low resistance and a high yield of heterogeneous connections. Moreover, the successful operation of the prototype verified the formation of more than 1 million (1080 × 960) connections in the pixel area, which is an order of magnitude necessary for fabricating high-resolution LED microdisplays.

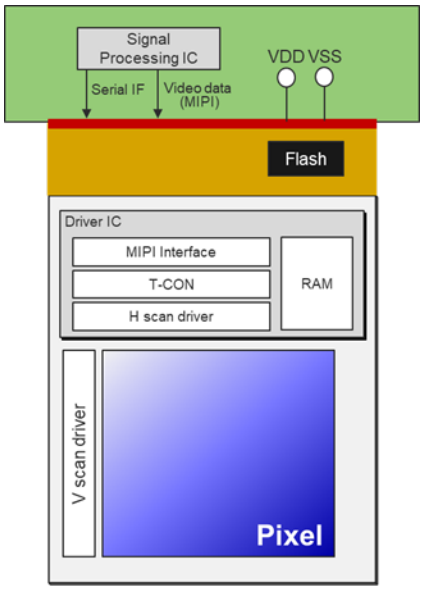

Figure 10. Block diagram of the driving circuit

Table 1. Specification of the LED Microdisplay prototype

	Specification
Screen diagonal	0.26-inch
Resolution	1080 × 960
Pixel Pitch	4.5μm
Frame Rate	120Hz
Signal Interface	MIPI
Color	Blue
Luminance	400,000 cd/m^2 (100 × 100-pixel)
Contrast Ratio	>1,000,000:1
Function	Demura Temperature compensation

5. Conclusions

We have established a process for fabricating an LED microdisplay toward AR applications, using Cu-Cu hybridization of a die-to-silicon transferred GaN/Si wafer and a Si CMOS backplane wafer, followed by the formation of LED mesas and OCLs. The prototype is the first demonstration of a blue mono-color active-matrix LED microdisplay fabricated with this process methodology. The pixel-level heterogeneous connections by the Cu-Cu hybridization demonstrated a high yield and finely tapered LED mesas with OCLs exhibited a 4.2-fold enhancement in light extraction efficiency. A prototype of a 0.26-inch 5644-ppi LED microdisplay exhibited a high luminance of 400,000 cd/m^2 and improved local uniformity. These experimental results confirmed the validity of our approach, and the established integration process enables further development toward fabrication of LED microdisplays with fine pixel pitches, high luminance, and high efficiency for AR applications.

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