A Multi-Drop High-Speed Link with Foveated Up-Scaler to Reduce Wires and Data Bandwidth in LED-on-Silicon-Backplane for AR Glasses

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Abstract

This paper presents a multi-drop high-speed link of micro LED-on-Silicon (LEDoS) display with foveated upscaling for AR glasses. By utilizing multi-drop connection of MIPI C-PHY, number of wires between host processor and LEDoS display module could be reduced from 36 to 6 wires with 1 trio per each left and right eye for data transmission. In order to maximize sampling timing margin, self-calibrated sampling phase is proposed regardless of jitter induced by multi-drop channel. Additionally, foveated upscaling technique is proposed to reduce total data bandwidth, and as a result, a 1.5Gsps MIPI C-PHY single trio can be used to transmit 3.5Gbps for AR glasses application. A silicon backplane is fabricated in a 28nm CMOS process and verified up to 2.0Gsps per trio in the MIPI C-PHY on multi-drop channel.

Author Keywords

LEDoS; Multi-drop receiver; Foveated rendering; micro display; AR;VR;MR;XR.

1. Introduction

Recently, there has been a significant interest in augmented reality (AR) glasses that leverage generative AI technology. Specifically, micro-displays are one of the key technologies that are suitable for the thin and ultra-lightweight form factors of glasses. The requirements for micro-displays include higher resolution with smaller display sizes, small pixel pitches, and compact high-speed interfaces for small form factors in AR systems [1-2]. A minimum number of wire connections are required between the host processor and display module while supporting higher data bandwidth.

In this paper, a self-calibrated multi-drop receiver is proposed with foveated upscaling function to effectively reduce data bandwidth. The self-calibration technique optimizes the sampling clock phase in the multi-drop channel. Furthermore, the data in the foveated area are transmitted without compression, while the other data are transmitted with downscaling and compression, thereby achieving a lower data rate on multi-drop channel.

2. Host Interface for AR backplane

2.1. Host Interface of Backplane for AR backplane

Figure 1 shows a typical example of a conventional MIPI DSI D-PHY connection between a single host processor and multiple displays for each color on both eyes of AR glasses. Essentially, MIPI D-PHY requires a minimum of 4 wires per single lane, including differential data and clock signals. As shown in the figure, a single host processor manages both eyes of the display, while three RGB chips for each eye have individual MIPI D-PHY 2.5Gbps links with two lanes, comprising four data and two clock wires. Consequently, at least 36 traces must pass through a confined space like the temple of glasses, necessitating a larger area for traces, PCBs, connectors, and flexible cables. Nonetheless, numerous wires and extensive PCB sizes are impractical within AR glasses due to considerations regarding form factor and weight.

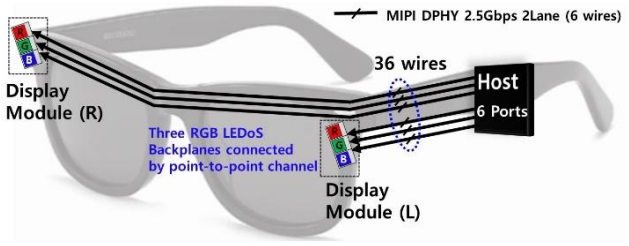
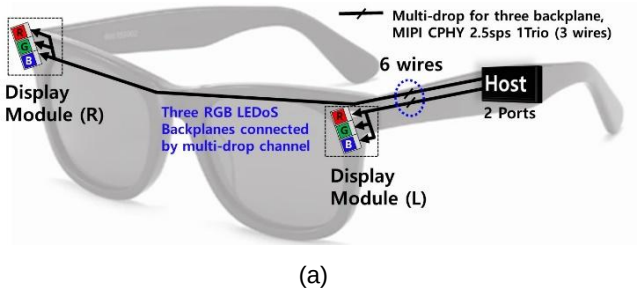


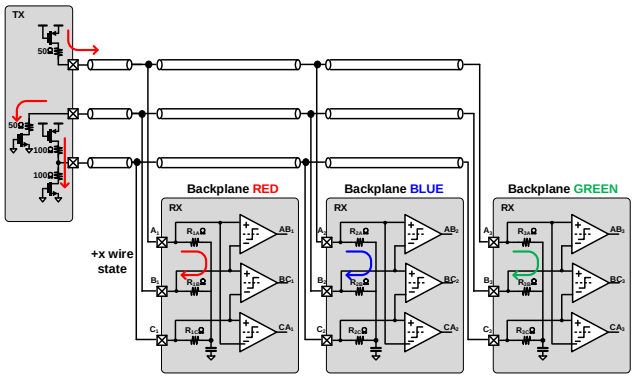
Figure 1. Configuration of RGB 3-chip micro-display system for AR Glasses

In order to simplify the connection, multi-drop channel is proposed instead of point-to-point, thereby further reducing the number of traces and display module size in the next section.

2.2. Multi-drop link with auto calibration



(a)



(b)

Figure 2. The proposed multi-drop link of AR system, and (b) channel connection of single Tx with three RXs.

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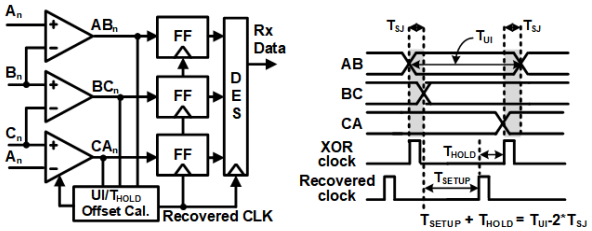
Figure 2 shows the proposed multi-drop channel and connection of single Tx port and three Rx ports of RGB color backplanes. As shown in Figure 2 (a), one trio of C-PHY from host are connected via multi-drop channel, and therefore total number of wires reduced by 83%, from 36 to 6 wires utilizing 2.5Gsps per trio. Termination resistors for each backplane are activated concurrently during high-speed transmission, enabling each backplane to receive and extract each RGB pixel data at the appropriate timing, as shown in Figure 2(b). Consequently, the host can transmit video streams to three color modules simultaneously without modifying the protocol of single monolithic RGB module.

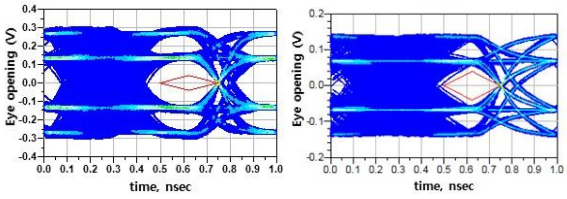
Proposed C-PHY receiver is presented in Figure 3. Conventional timing diagram of XOR clock and recovered clock are shown in point-to-point channel [3]. Derived from the last toggle, the XOR clock is delayed to establish the phase that effectively samples all AB, BC, and CA data, as shown by the recovered clock.



(a) (b)

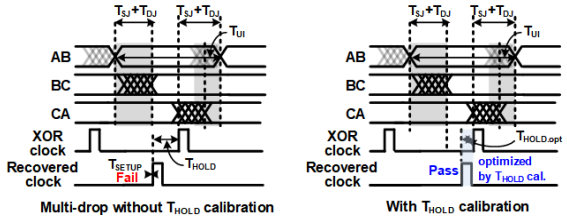
Figure 3. (a) Block diagram of C-PHY receiver, and (b) clock timing for setup and hold time of Sampler

However, a multi-drop channel induces additional jitter generated from impedance mismatches on stubs as shown in figure 4. Due to the reduction of the timing budget in a multi-drop channel, it becomes challenging to identify the optimal sampling phase due to process, supply voltage, and temperature variations, as described in figure 5(a). Therefore, T_{HOLD} calibration is proposed to find the optimum position on-the-fly in figure 5(b). By searching for the optimal delay of the recovered clock from the XOR clock, sufficient hold time margin can be achieved.



(a) (b)

Figure 4. Triggered Eye diagram of (a) point-to-point and (b) multi-drop channel at 2Gsps



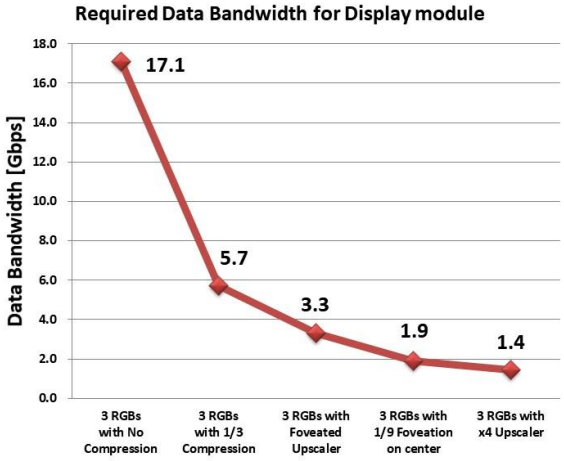
(a) (b)

Figure 5. Recovered clock timing diagram (a) before and (b) after proposed T_{HOLD} calibration in multi-drop channel

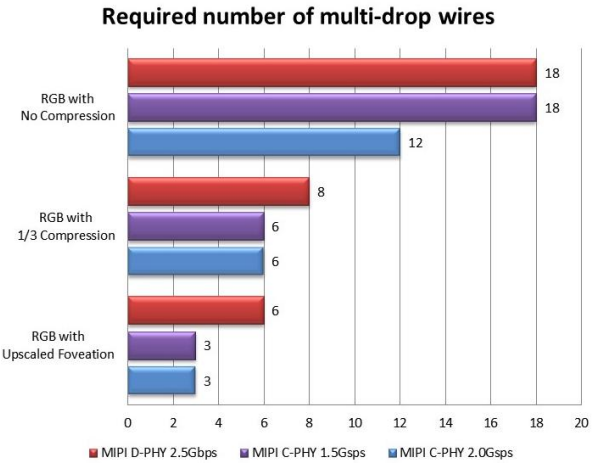
Nevertheless, since reflective jitter from a multi-drop channel cannot be eliminated, it is necessary to decrease the data rate further by reducing the data bandwidth with the assistance of foveation, scaling, and compression. Also reducing power consumption can be achieved simultaneously as described in the next section.

2.3. Foveated Upscaling with Compression

In order to save power consumption of image processing in GPU and application processor, foveation technique has been widely used in AR/VR application [4-6]. In this paper, combination of foveation and upscaling with compression technique is proposed. In figure 6, it is assumed that resolution is 1500x1200 with 8bits per each color. The refresh rate is set to 120 Hz, while assuming that data writing to memory-in-pixel is completed within 33% of a single frame time to allocate emission time for the micro-LED during the remaining time. The data bandwidth without compression reaches up to 17.1 Gbps, which decreases to 3.3 Gbps when the high-resolution area (HA) is set to 1/9 of the full frame, and the low-resolution area (LA) is set to 1/4 downscaled with 1/3 compression. Therefore, data rate of MIPI C-PHY can be reduced to 1.5Gsps(=3.42Gbps) with single trio (3 wires)



(a)



(b)

Figure 6. (a) Required bandwidth and (b) number of multi-drop wires in 1500x1200, 24bit colors and 360Hz burst write mode for 120Hz refresh rate

When comparing eye diagram of MIPI C-PHY data rate of 2.5Gsps, 1.25Gsps and 1.5Gsps shows better performance of eye opening in multi-drop channel as shown in figure 7.

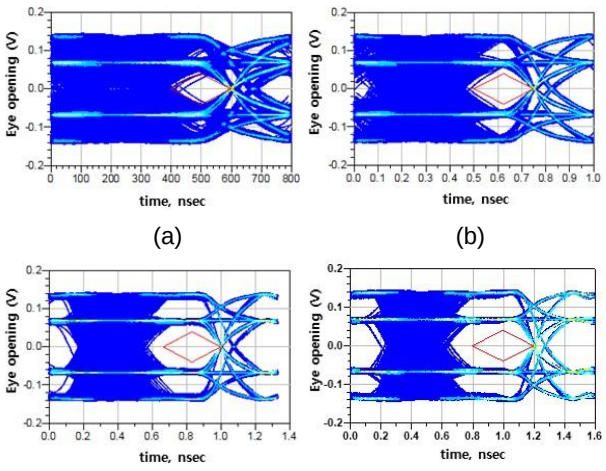
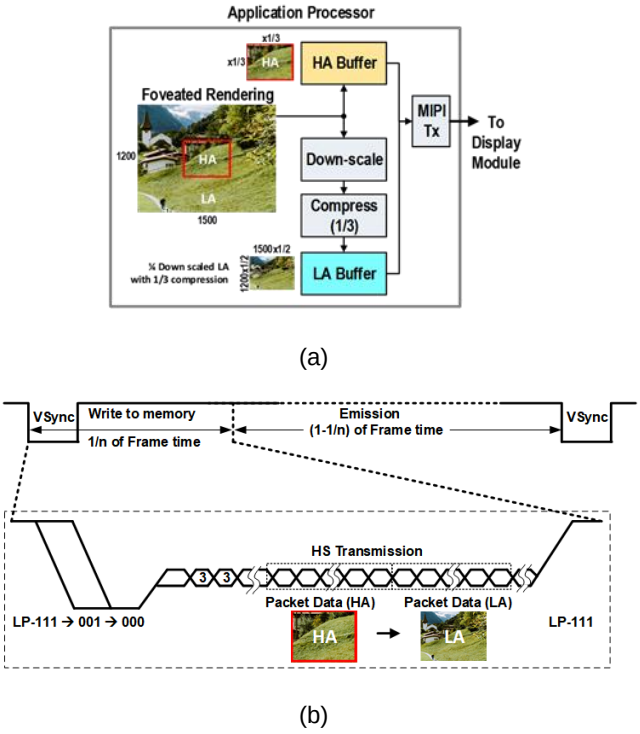


Figure 7. Triggered Eye diagram of (a) 2.5Gsps, (b) 2.0Gsps, (c) 1.5Gsps, (d) 1.25Gsps in multi-drop channel

Figure 8 illustrates the proposed data bandwidth reduction technique that employs foveation and upscaling with compression. In the application processor side, the full frame image is divided into two parts: the high-resolution area (HA) at the focused region and the low-resolution area (LA) in the other region. The video data of the HA are transmitted to the display module first, followed by the LA data, which are downscaled and compressed as described in Figure 6(a) and (b).



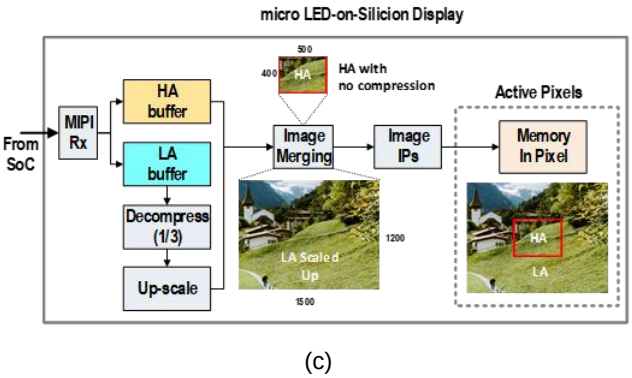


Figure 8. Foveated upscaling with compression technique

In figure 8(c), the LEDoS backplane receives the HA and LA data sequentially, and merges them after decompressing and upscaling the LA data. Once the image processing on image IPs, such as LED characteristics and IR drop compensation, are completed, the video image is sent and stored in the memory pixel, preparing for the emission of the micro-LED. Ultimately, data transmission can be achieved using a single trio of C-PHY in a multi-drop channel, while the focused area does not experience any visual loss.

3. Measurement Results

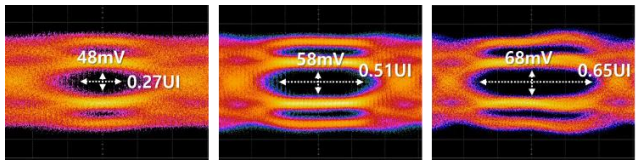
The proposed backplane was fabricated in a 28nm CMOS process technology, and tested with a multi-drop channel connecting three backplane modules as summarized in table 1 and figure 9.

Table 1. Summary of the proposed LEDOS backplane

Technology	28nm CMOS process
Supply voltage	1.0V / 1.8V for MIPI Interface
High-speed Interface	MIPI C-PHY max 2.5Gsps receiver, 1-trio MIPI D-PHY max 2.5Gbps receiver, 4-lanes
Display Info.	1500 x 1200, 24bit color, 120Hz
Test environment	3 drops, 5.9mm/12.1mm/12.1mm on each drop

Figure 9. (a) Test environment for multi-drop channel of LEDoS backplane, (b) blue color display module, (c) measured eye-diagram of MIPI C-PHY at 2.5Gsps/trio, and (d) 1.5Gsps/trio on multi-drop module

As shown in the measurement result of figure 10, measured Rx eye opening at 2.5Gsps was only 48mV and 0.27UI, and it was enhanced by 68mV and 0.65UI, 41% and 240% for each vertical and horizontal eye opening at 1.5Gsps. Consequently, three LEDoS backplanes was successfully operated with sufficient eye opening margin up to 2.0Gsps on multi-drop channel configuration.



(a) (b) (c)

Figure 10. Measured eye-diagram of MIPI C-PHY at (a) 2.5Gsps/trio, (b) 2.0Gsps/trio, and (c) 1.5Gsps/trio on multi-drop module

4. Conclusion

In this paper, a multi-drop MIPI C-PHY link driving method for LEDoS modules was proposed. By introducing a hold time auto-calibration technique of C-PHY and foveated upscaling techniques, three backplane modules could communicate with a single host via multi-drop channel with sufficient eye margin. The number of wires and C-PHY data rate were optimized to 6 wires, representing an 83% reduction from 36 wires, and 50% of the data bandwidth was saved. By combining the proposed foveated up-scaler with high compression techniques and eye tracking functions along with partial updates, further data bandwidth reduction and power consumption savings can be achieved effectively.

5. References

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