Enabling Next-Generation Metal-Oxide Backplane Technology by Atomic Layer Deposition

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Abstract

Plasma Enhanced Atomic Layer Deposition (PEALD) dielectrics was developed for metal oxide thin-film transistors. The improvement on Vth uniformity, SS tunability, and stability were previously inaccessible by conventional PECVD dielectrics. Our PEALD provides uniform and high-quality films with accurate control of precursor/plasma and fast purge architecture, which is scalable up to Gen8 size.

Author Keywords

PEALD; high-k; large SS; high mobility metal oxide

1. Introduction

Thin-film transistors (TFTs) made with metal oxide (MOx) semiconductors, such as amorphous-InGaZnO (IGZO), often show lower leakage current, better panel uniformity, and lower manufacturing cost compared to TFTs made with low temperature polycrystalline Si (LTPS) [1] [2]. Therefore, LTPS combined with metal oxide (LTPO) has been developed to take advantage of high mobility and large subthreshold slope (SS) from LTPS as scan driver (GIP) and pixel driving (DR) TFTs, and low leakage from MOx as pixel switching (SW) TFTs for high-end active-matrix organic light emitting diode (AMOLED) display panel. Further cost reduction of AMOLED panel may be possible if GIP, DR, and SW TFTs are all manufactured with MOx materials. This requires the MOx to exhibit high mobility when used as GIP and SW TFTs, and large SS and good stability when used as DR TFTs.

However, these requirements are considerable challenging to existing MOx materials: 1). For GIP and SW TFTs, large amount of oxygen vacancy (V_o) resulting from physical vapor deposition (PVD) sputtering leads to narrow process window and uncontrollable threshold voltage (V_{th}) especially for high mobility metal oxide (HMOx) materials [2] [3]. TFTs with different channel length (Ch-L) also suffer from different V_{th} due to V_o diffusion along the channel direction [4] [5]. 2). For DR TFTs, high mobility usually leads to fast turn-on and thus small SS, leading to poor OLED grey color controllability.

In this paper, we introduce an equipment solution to resolve these issues. We developed thin SiOx layers deposited by our plasma enhanced atomic layer deposition (PEALD) system as interfacial gate insulator (IGI). The TFTs with PEALD IGI show more controllable V_{th}, and improved V_{th} uniformity at different Ch-L compared to TFTs with only plasma enhanced chemical vapor deposition (PECVD) GI. In addition, we developed bottom layer GI (BGI) stacks composed of high-k materials deposited by our PEALD system. The TFTs with high-k BGI exhibit considerably larger SS and better device stability compared to TFTs with conventional SiNx and SiOx BGI layers. The results demonstrated that our PEALD system created new possibilities to enable next generation MOx back-plane technology for AMOLED display.

2. Experimental Section

Hardware configuration: The PEALD system used for this work is a showerhead type system for 1500mm×1850 mm G6 size glass, where proprietary showerhead and lid design were applied for uniform gas distribution and high efficiency gas purging. Liquid precursors from canister are vaporized and delivered to process chamber through precursor delivery system (PDS). The showerhead, lid, and PDS guarantee a uniform precursor delivery over large area without particle or thermal decomposition.

Film thickness measurement: The thickness map was generated by 96 points thickness measurement using ellipsometer (JA Woollam, M-2000) with large area translational stage provided by KMAC on G6 size glass.

TFT fabrication: A 150nm thick molybdenum (Mo) is coated and patterned as the bottom-gate (BG). Then, 100nm SiNx and 300 nm SiOx are deposited, which serve as the BGI. After that, metal oxide active layer(s) are deposited using magnetron sputtering with the New Aristo™ 1400L. The active layers are composed of either 30nm IGZO single layer, or 15nm IGZO + 5nm HMOx (metal oxide material with mobility higher than IGZO) dual layer to form the semiconducting channel layers of the IGZO TFT, or the HMOx TFT, respectively. After channel layer patterning with oxalic acid, gate insulator (GI) layers are deposited. The GI layers are composed of a thin PEALD deposited interfacial GI (IGI) layer, followed by PECVD deposited bulk GI layer to form a total GI thickness of 150nm. For reference TFT, the 150nm GI layer is deposited using PECVD only. A Ti/Mo (30nm/250nm) metal was deposited by sputtering and patterned as the top gate (TG). GI layer not covered by TG are then patterned by plasma dry etching, and the exposed IGZO area are treated with He plasma to form n+ contact region. Interlayer dielectrics (ILD) of SiOx/SiNx (400nm/100nm) was coated using PECVD and via holes are patterned. Finally, 30nm/250nm thick Ti/Mo layer is coated and patterned to form source and drain electrodes to finish the TFT fabrication. The sizes of all TFTs presented in this manuscript have a channel width of 4μm, and channel lengths are varied.

Device characterization: The electrical properties were measured by Keysight B1500A. For TFT transfer characteristics (I_d-V_g curve), the TG voltage is applied from -20V to +20V at room temperature with BG connected to source. The stress voltage is applied to the TG during positive bias temperature stress (PBTS, V_g= +30V, 70°C) for 1 hour with BG connected to source. V_{th} was extracted from $V_g@I_d=W/L\times1E\text{-}8A$, where W and L are the width and length of the measured TFTs. SS was extracted from the equation $SS=(1/3)\times[(V_g@I_d=1E\text{-}8A)-(V_g@I_d=1E\text{-}11A)]$. Note here that in this definition, SS is not normalized to device sizes. TFTs with longer channel length leads to larger SS when their have the same channel width.

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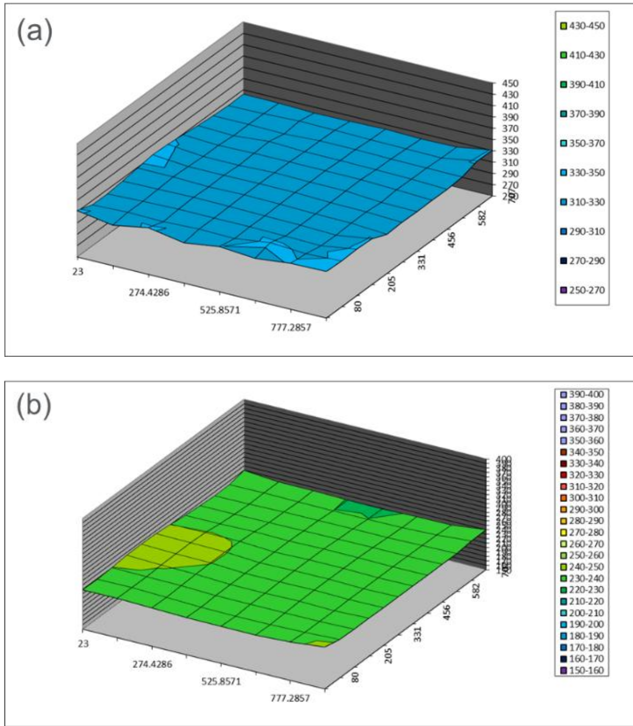

Figure 1. Film thickness maps of (a) SiO_x, and (b) TiOx deposited by G6 PEALD

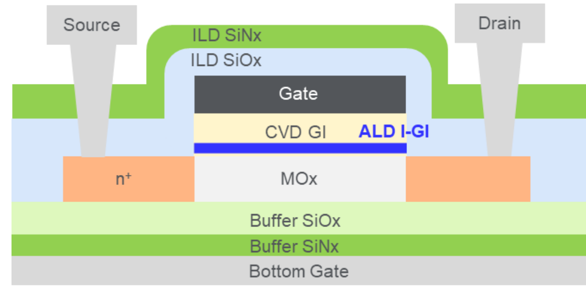

Figure 2. Schematic of a dual-gate coplanar TFT

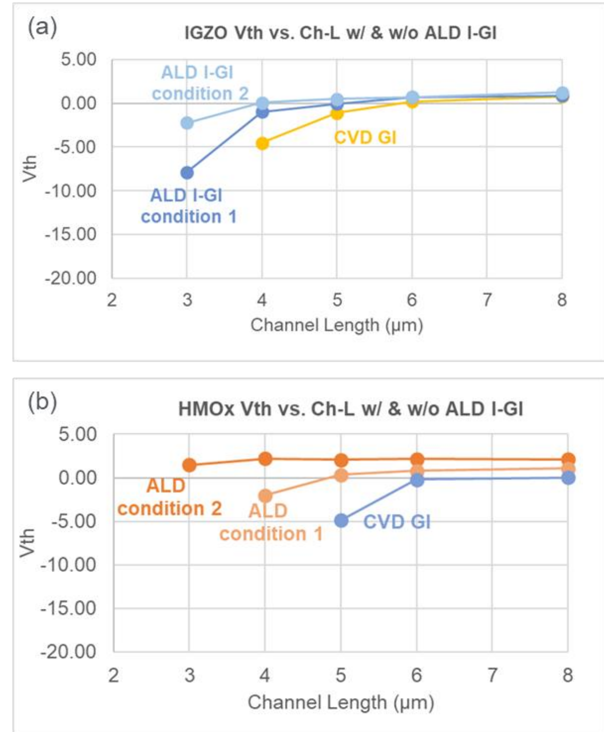

Figure 3. Vth vs. Ch-L of (a) IGZO and (b) HMOx TFTs w/ and w/o PEALD IGI layer

3. Results and Discussion

Single film characterization: Film thickness uniformity on large platform is critical to practical display application. Figure 1 shows the thickness maps of SiOx and high-k TiOx layer deposited by our PEALD system. Both of layers show non-uniformity of <3% on Gen 6 glass panel. Table 1 (a) provides more details about PEALD deposited SiOx films at 250C and 350C deposition temperature using di-isopropylaminosilane (DIPAS) precursor. The deposition rates, which may vary depending on growth per cycle (GPC) and cycle period, are generally greater than 25Å/min for stable layer-by-layer deposition at both temperatures. The in-film H contents measured by SIMS are 2.5% and 1.8%, respectively. In comparison, SiOx films deposited by PECVD systems are usually in the range of 4%~5%. Table 1 (b) shows the PEALD deposited TiOx film properties. The k-values are between 15 to 30 depending on deposition conditions.

Table 1: Summary of film property of (a) SiOx, and (b) TiOx deposited by G6 PEALD

(a)

Depo. Temp.	RI	Non-Unif. %	H Contents	Stress (Mpa)	Break-down (MV/cm)
250C	1.46	<3%	2.5%	~ -300	>12
350C			1.8%	~ -200	

(b)

Depo. Temp.	RI	Non-Unif. %	k-value	Stress (Mpa)	Break-down (MV/cm)
200C	2.30	<3%	15~30	~ -300	>3

IGZO and HMOx TFTs with PEALD IGI: Schematic of a dual-gate (DG) coplanar TFT device is shown in Figure 2. The fabrication details are described in Experimental Section. As shown in Figure 3 (a), IGZO TFTs with PECVD GI present V_{th}>0V at L≥6µm, while V_{th} shifts negatively at L=5µm. It further degrades to -4.5V at L=4µm and becomes conductive when L≤3µm (not shown). With PEALD SiOx IGI while keep all the other integration processes the same, the IGZO TFTs shows an improved V_{th} uniformity of >0V from L=4µm to 8µm. This improvement is possibly attributed to effective V_o passivation at IGZO/IGI interface by PEALD IGI deposition [6] that reduces the V_o relocation from n+ to channel region [5]. Simulations using the proprietary TCAD solution Ginestra™ [7] modeling platform confirm a reduction of shallow defects level for TFTs with PEALD IGI layer.

Figure 3 (b) shows the V_{th} vs. Ch-L plot of HMOx TFTs. Without PEALD IGI, HMOx TFTs have positive V_{th} when L≥6µm, and become conductive when L≤4µm (not shown). With PEALD IGI, V_{th} is controllable from 0V to 2V for L≥5µm with different IGI deposition conditions, and is possible to remain positive at L≥3µm. The wider range of V_{th} positions observed in HMOx TFTs is possibly due to larger amount of V_o in HMOx than that in IGZO, leading to different degree of V_o passivation by IGI. The

results also indicate that the integration optimization for HMOx TFTs is more challenging than IGZO TFTs and requires further study.

From the above results, IGI deposited by our PEALD system exhibits effective V_{th} control and V_{th} uniformity improvement. TFTs with different Ch-L show comparable V_{th}, indicating a reduced material sensitivity and an extend process window of integration. This improvement is particularly beneficial for GIP and SW TFTs as short channel lengths are required for high-current and high-speed operation.

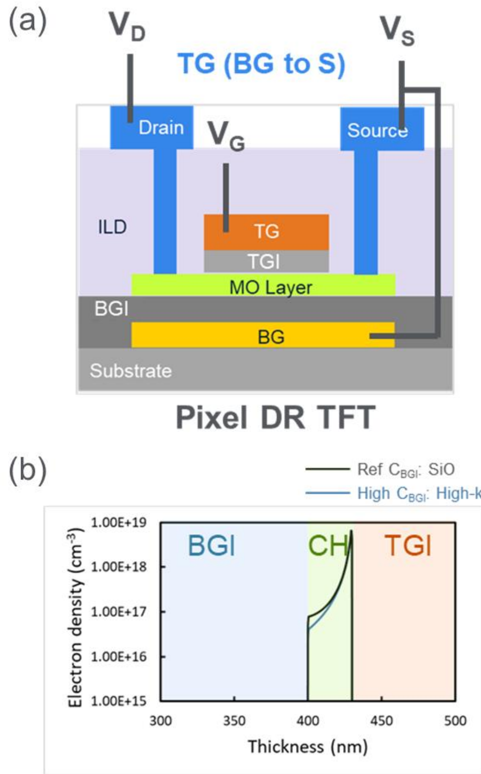

Figure 4. (a) TG operation scheme in a DG TFT (b) Simulated electron density in the MOx channel layer

IGZO TFTs with PEALD high-k BGI: Figure 4 (a) shows the TG operation scheme of a dual-gate TFT when used as a DR TFT with BG connected to source. Figure 4 (b) shows the simulated electron density in the channel layer under V_g=15V gate bias by Ginestra™ modeling platform with two different types of BGI stacks. When the BGI is composed of high-k materials, the electron density near the IGZO bottom interface is lower compared to that when the BGI is composed of SiOx at the same BGI thickness. This difference is due to the higher BGI capacitance formed between channel layer and BG by replacing SiOx with high-k materials, and thus, the electric potential at BG (grounded) has stronger impact to decrease the electron density in the channel.

Higher BGI capacitance can also be achieved by using thinner BGI thickness. As shown in Figure 5, when the SiOx BGI thickness decreases from 300nm to 10nm, higher BGI capacitance (not shown) and larger SS (+100%) is observed for IGZO and HMOx TFTs by Ginestra™ simulation. However, BGI thickness of <50nm may not be practical due to poor step

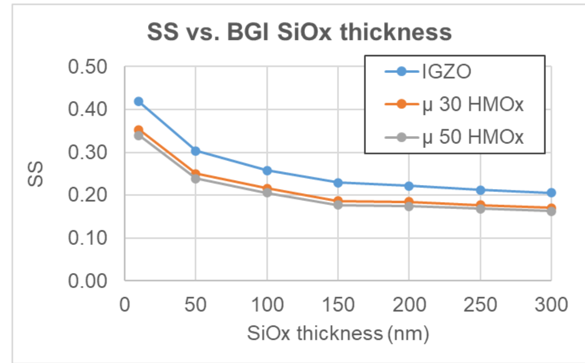

Figure 5. Simulated SS vs. BGI SiOx thickness of MOx TFTs with different field effect mobility

coverage over large area on the patterned BG metal. Alternatively, when high-k materials are employed as BGI dielectrics, the BGI thickness can be increased effectively by $k_{high\text{-}k}/k_{SiOx}$ times, while having the same BGI capacitance as thin SiOx. This makes it possible for HMOx TFTs to achieve a reasonably large SS to work as DR TFTs and keep sufficient BGI thickness for good step coverage.

Figure 6 (a) shows the schematics of two types of BGI stacks. One is SiOx BGI composed of SiNx/SiOx with thickness of 100nm/200nm, another is High-k BGI composed of SiNx/High-k/SiOx with thickness of 100nm/160nm/40nm. These two BGI stacks are applied to IGZO TFTs shown in Figure 2. Devices are fabricated with high-k materials deposited by our PEALD system, and SiOx and SiNx layers deposited by PECVD system. As shown in Figure 6 (b), TFTs with High-k BGI exhibit considerably larger SS than those with SiOx BGI. In addition, better device stability is observed with TFTs that employ high-k BGI possibly due to less electrons density in the channel during PBTS measurement as seen in Figure 4(b).

Owing to the adoption of high-k BGI deposited by our PEALD, electron density in the channel layer is effectively decreased, while enlarged SS and improved device stability under PBTS are achieved. These improvements provide new optimization directions for dielectric layer stacks in DR TFTs, as large SS and good stability are critical for stable OLED grey color control.

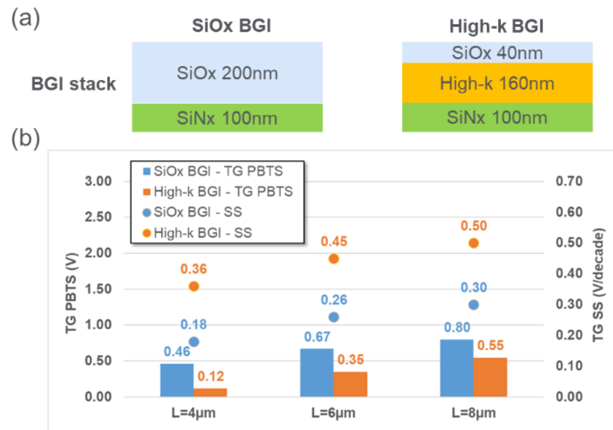

Figure 6. (a) Schematics of SiOx BGI and High-k BGI stacks, and (b) the corresponding TG PBTS & SS of IGZO TFTs

4. Conclusion

In this work, both SiOx and high-k materials (TiOx) are developed on our G6 PEALD platform and exhibit excellent film uniformity. We demonstrated that PEALD SiOx, when served as the IGI layer in IGZO and HMOx TFTs, improved the V_{th} controllability and uniformity for devices with different Ch-L. High-k materials deposited by PEALD effectively enlarged the SS and device stability when employed in the BGI stack. These results demonstrated that dielectric layers deposited by PEALD system have great potentials to play critical roles for GIP, SW, and DR TFTs, and enable next-generation MOx backplane technology.

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5. References

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