# State-of-the-Art Gas Separation Function in Dynamic New Aristo TWIN PVD System Proven with IGZTO-IGZO Dual-Layer Thin-Film Transistor

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## Abstract

***This work presents the new hardware design to enable multilayer PVD coating in the dynamic PVD system New Aristo™ TWIN. Its performance is validated by PVD film uniformity, as well as IGZTO/IGZO dual layer top-gate thin film transistor performance. By comparing the metal oxide film uniformity and the device properties, we conclude that the actual gas separation has reached comparable performance as the simulated perfect gas separated coating condition.***

## Author Keywords

Gas separation, metal oxide, multilayer coating, high throughput, film uniformity, dynamic PVD system, IGZTO, IGZO, rotary target.

## 1. Introduction

For metal oxide materials as active layer in a thin-film transistor (TFT), IGZO-like materials are under development to aim for device mobility > 30, and even higher. Active layer with multilayers of IGZO-like metal oxide has shown wide bandwidth for exploration towards good device performance [2-6]. To have better positive-bias temperature stress (PBTS) and negative-bias temperature illumination stress (NBTIS) performance, it has been shown that a capping layer is beneficial [7]. We have studied that capping layers either at bottom or on top can be used to improve both PBTS and NBTIS. Often such a multilayer structure requires different gas environments for each metal oxide layer [2-5]. The layers need to be either coated separately, that is, in two chambers that are separated by lock valves (as in a static PVD system) or by very long distance in a dynamic PVD system to ensure gas mixing is limited.

However, with our state-of-the-art gas separation module, it is possible to do continuous mass production in our dynamic PVD (physical vapor-phase deposition) system without the need to increase tool footprint drastically. The following sections will demonstrate the performance of the gas separation function with not only film thickness and uPCR maps, but also TFT performance.

In this work, we use amorphous IGZO and IGZTO (a-IGZO and a-IGZTO in short) as the TFT active layer materials to validate device performance.

## 2. Experimental setup

***Test stand hardware configuration:*** The test stand in Tainan Display Lab (TDL) is modified from a New Aristo™ VR system into a TWIN-like system, separating side A from side B completely, as shown in Figure 1. The VR chamber belongs to side A and the lock valve between chamber T2A and VR is always open during process. The experiment was executed in side A. The gas separation hardware is installed on two chamber doors of P2A, separating the gas environment of T1A, P1A and P2A from T2A and VR. Whether the gas separation module works well or still allows some gas crosstalk that will impact film property is of interest in this report. Design detail of the gas separation module will not be disclosed due to IP protection.

***Film property measurement:*** The thickness (THK) map is generated by measuring film transmittance and reflectance at 441 positions on the 1400 × 1500 mm size substrate, and then with thickness fitting model provided by SENTECH Instruments GmbH, film thickness on each measurement position is obtained. uPCR (abbreviated as microwave photoconductivity response; also known as uPCD, abbreviation for microwave photoconductivity decay) [8-9] is measured by Semilab FPT-10 Metrology Station (Semilab Semiconductor Physics Laboratory Co. Ltd.) compatible up to Gen 10.5 (2940 × 3370 mm) size. For uPCR maps in this work, 400 points were measured on the 1400 ×1500 mm substrate.

***Device fabrication:*** Schematic of a-IGZTO/a-IGZO dual-gate (DG) coplanar TFT device is shown in Figure 2. A patterned 150 nm thick molybdenum (Mo) is coated as a bottom-gate (BG). Then, 300 nm SiOx & 100 nm SiNx are deposited, which serve as the BG insulator (BGI). After that, dual metal oxide active layer of a-IGZTO (In:Ga:Zn:Sn = 4:1:4:1) and a-IGZO (In:Ga:Zn = 1:1:1) are deposited using magnetron sputtering with the New Aristo™ 1400L test stand. A Ti/Mo (30 nm/250 nm) metal was deposited by sputtering as a top-gate. A patterned interlayer of SiOx/SiNx (400 nm/100nm) was coated with PECVD. Finally, 250 nm thick Mo layer is coated as source and drain electrodes. After final patterning, the DG TFT device is fabricated.

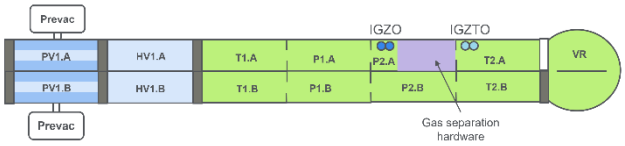


**Figure 1.** Target arrangement and hardware configuration in the New Aristo™ 1400L test stand.

***Device measurement:*** The electrical properties were measured by Keysight B1500A (POMME TECHNOLOGIES., LTD). For initial transfer characteristics ($I_d$-$V_g$ curve), the TG sweep is from -20V to +20V and measured of TG driving TFT at room temperature (RT). The stress voltage is the potential applied to the TG during PBTS (Vg= +30V, 70ºC) & NBTIS (Vg= -30V, 70ºC, under 2000 nits illumination) for 1 hour.

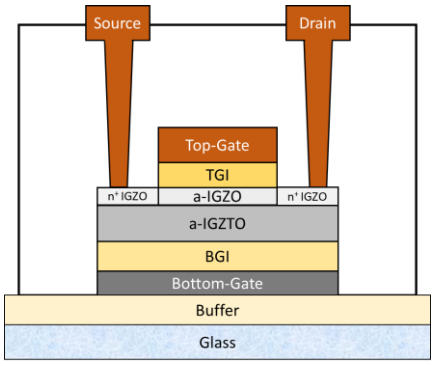


**Figure 2.** Schematic of a-IGZTO/a-IGZO DG coplanar TFT device.


*ISSN 0097-996X/25/5601-0019-$1.00 © 2025*

## 3. Leak rate measurement

To have a quantitative evaluation on the gas separation effectiveness, we use the equation as follow:

$$Leak\ ratio = \frac{P_{other\ side} - P_{0,other\ side}}{P_{flow\ in} - P_{0,flow\ in}} \times 100\% \quad (1)$$

Firstly, base pressure is measured with BPG (base pressure gauge, Inficon BPG400) for both sides of the gas separation module to get $P_{0,flow\ in}$ and $P_{0,other\ side}$. Then, we gradually flow in Ar in one side of the gas separation, from 200 sccm increasing to 900 sccm. This corresponds to an increase of pressure from 0.182 Pa to 0.846 Pa. Each step of gas inlet increase is 100 sccm and pressure on the other side of the gas separation module will be measured using CDG gauge (Inficon CDG 045D) after 2 minutes to ensure chamber pressure is stable. At this point, the leak ratio from one side to the "no-gas-side" is defined by equation (1), as shown in the upper half of Figure 3.

Then, the same is done with flowing Ar from the previously "no-gas-side" to define the gas leak ratio for the opposite direction, as indicated by the lower half of Figure 3. The gas separation performance of the tool is defined by the leak ratio average of the two directions. One can also judge from the leak ratio, if there is asymmetric gas leak preferring one certain direction than the other. This indicates there is uneven pumping efficiency by asymmetric shielding or pump configuration. The leak ratio performance at the TDL New Aristo™ 1400L system, is measured < 5% for both directions.

However, the leak rate measured under such condition is rather far from actual production situation. In production, both sides of the gas separation module will be filled with process gas, and hence the pressure difference would be much smaller, allowing less gas crosstalk than in the leak ratio test. Therefore, it is necessary to demonstrate the impact on metal oxide film, comparing "perfect gas separation" ("perfect GS") and "actual gas separation" ("actual GS"). It will be demonstrated in the next section.

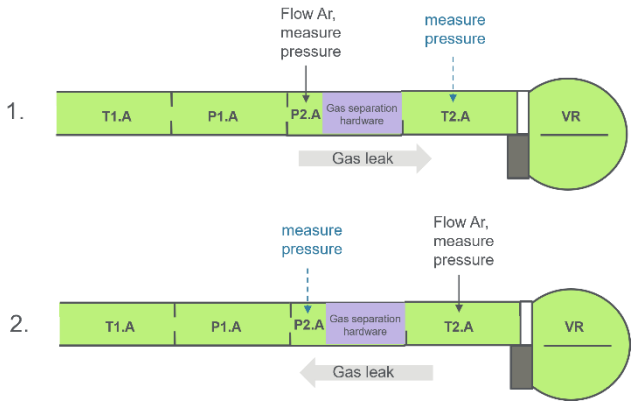


**Figure 3.** Schematic to show leak ratio measurement. Side B and load lock chambers are removed for simplicity.

## 4. Metal oxide film property comparison

In this section, a-IGZTO/a-IGZO dual layer metal oxide is used to verify the performance of the gas separation module. As shown in Figure 1, IGZTO and IGZO is deposited in T2A and P2A chambers, respectively. From internal study, the best coating conditions for IGZTO and IGZO are both at 0.5Pa but 80% $O_2$ and 40% $O_2$, respectively. The need for different $O_2$ concentration during process allows us to evaluate the performance of the gas separation. We have the "actual GS" case, and the "perfect GS" case to make the comparison.

For the "actual GS" case, VR and T2A chambers are filled with 0.5 Pa, 80% $O_2$, while T1A, P1A, and P2A chambers with 0.5 Pa, 40% $O_2$. The deposition of IGZTO and IGZO is done continuously, without having the substrate returning to HV1A chamber.

For the "perfect GS" case, both IGZTO and IGZO layers are deposited while the entire PVD system is filled with the designed gas conditions, i.e., 0.5 Pa 80% $O_2$ and 0.5 Pa 40% $O_2$, respectively. First, the bottom IGZTO layer is coated in 0.5 Pa 80% $O_2$ atmosphere, and the substrate returns to HV1A chamber. After that, the gas condition of the whole PVD system is changed to 0.5 Pa 40% $O_2$, and then the IGZO top layer is deposited. In this way, we can guarantee that no gas crosstalk is possible, hence, a simulated "perfect GS".

Figure 3 shows that both cases produce as-deposited (not annealed) film with comparable uPCR sum amplitude. The gray areas in the uPCR maps in Figure 3 are the positions on the mother substrates where the TFT wafers are attached, whose data will be discussed in the next section.

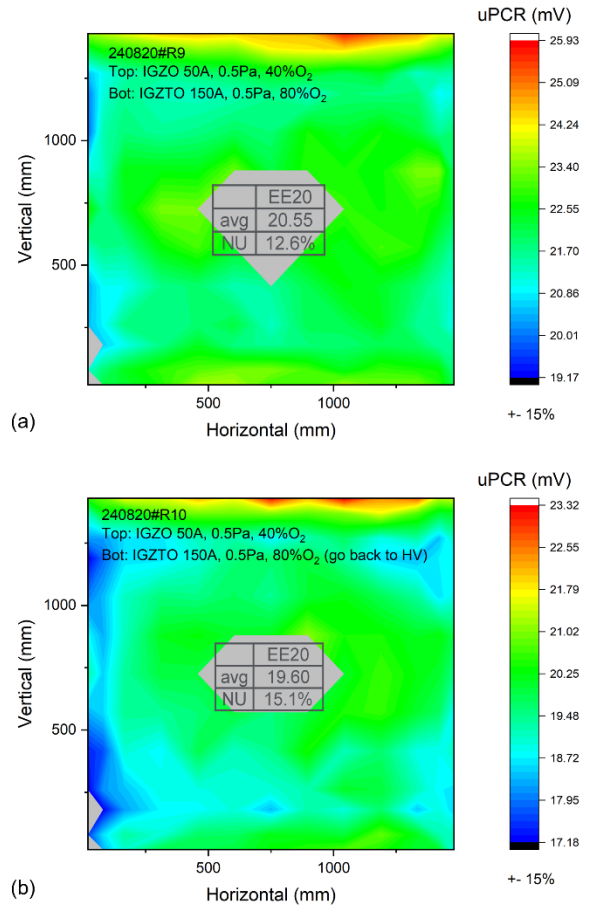


**Figure 3.** uPCR maps of as-deposited IGZTO/IGZO dual layer stack on glass with comparison of (a) "actual GS" and (b) simulated "perfect GS".

## 5. IGZTO/IGZO TFT performance validation

To validate electrical properties of a-IGZTO/IGZO dual layer metal oxide, IGZTO/IGZO TFTs with DG structure were fabricated and transfer characteristics ($I_d$-$V_g$ curves) were measured.

Figure 6(a) exhibits the threshold voltage ($V_{th}$) position change along channel length from 8 µm down to 3 µm with channel width= 4 um. One can see that the $V_{th}$ tendency of the two cases is comparable, that is, the two cases show same process window. Further optimization is possible to shift overall $V_{th}$ position more positive and allow larger process window.

Figure 6(b) and Figure 6(c) showcase very similar device properties for the two cases: at $V_{ds}$= 1 V, $V_{th}$ is -2.94 V for "actual GS" and -1.88 V for "perfect GS". The deviation is within our device integration variation. For device mobility and sub-threshold slope (S.S.), the deviation is 1.8 $cm^2/V*s$ and 0.02, which are acceptable differences given the benefits mentioned in the introduction section. Please note that the integration has not been optimized yet, and we see many tuning knobs for further improvement.

Figure 7 shows TG driving TFT device stability by applying PBTS at 70°C for 1h with +30 V as stress voltage and NBTIS at 70°C for 1h of -30 V as stress voltage under 2000 nits illumination. Measured TFTs show PBTS of 2.56 V and 2.59 V for "actual GS" and "perfect GS", respectively. And NBTIS is -0.68 V and -0.95 V, respectively. Both PBTS and NBTIS data show that the stress results between two conditions are similar.

All device properties are summarized in Table 1. The data listed proves the "actual gas separation" provides comparable device performance as "perfect gas separation".

**Table 1.** Overview for device performance comparison between "actual GS" and "perfect GS".

| | $V_{th}$ (V) | Mobility ($cm^2/V*s$) | S.S. | PBTS (V) | NBTIS (V) |
|---|---|---|---|---|---|
| Actual GS | -2.94 | 26.7 | 0.19 | 2.56 | -0.68 |
| Perfect GS | -1.88 | 28.5 | 0.21 | 2.59 | -0.95 |

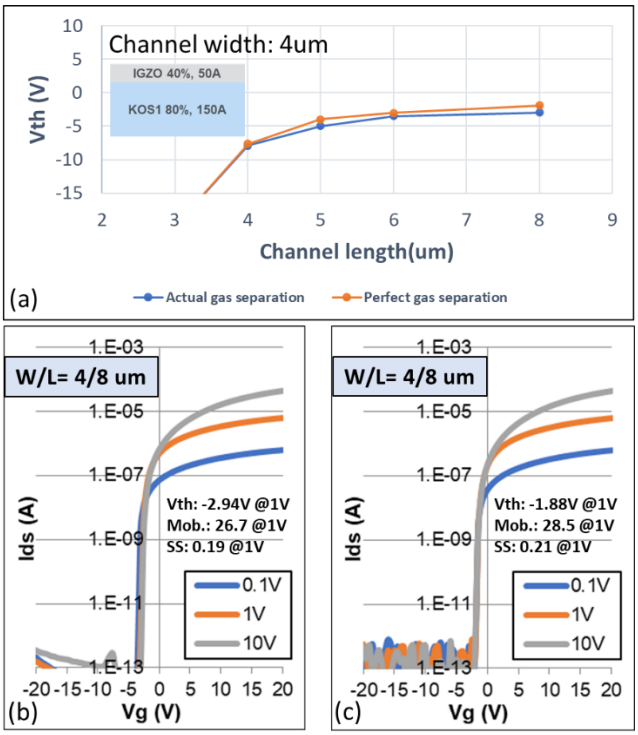


**Figure 6.** Transfer characteristics of TG driving TFT. (a) $V_{th}$ position at width= 4 um of different channel length 3 to 8 um, (b) $I_dV_g$ curve of real GS device and (c) $I_dV_g$ curve of perfect GS device.

## 6. Conclusion

This work demonstrates the performance of the state-of-the-art gas separation module developed by Applied Materials ®, which enables continuous multilayer deposition with more than one process gas conditions within the New Aristo™ TWIN PVD system. With uPCR maps, it is shown that PVD film property is the same for the actual process compared to the perfect gas separated case. Device performance is also shown to be the same for short channel tendency, PBTS and NBTIS, only with marginal difference in $V_{th}$ and mobility. With this result, we can confidently promote our tool to the market and expect the higher flexibility for PVD deposition can contribute to innovation for next generation display products.

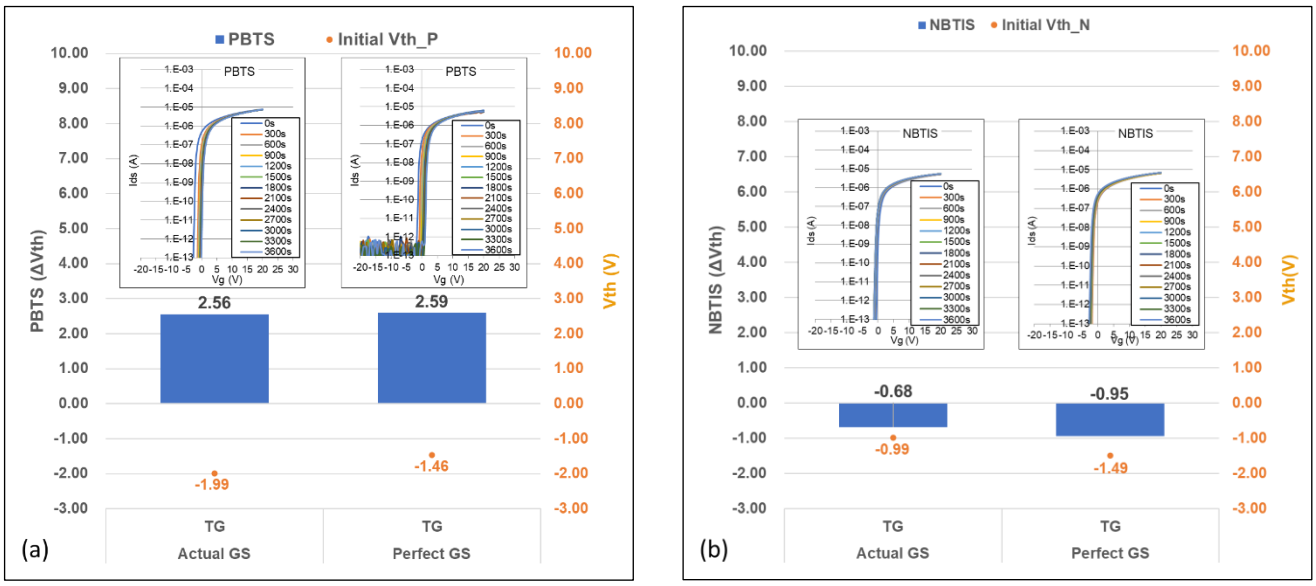


**Figure 7.** Transfer characteristics under TG (a) PBTS and (b) NBTIS.

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