A Study on Less Mask Process of Metal Insulator Metal Storage Cap Doping

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Abstract

In this work, the storage cap was formed by doping poly Si under the gate insulator in the contact hole process without using the storage cap doping mask. Using SIMS analysis, it was confirmed that boron was injected into Poly Si by passing through the gate metal, and by measuring the CV curve of Poly Si-GI-Gate Cap, it succeeded in securing flat MIM characteristics.

In addition using Half-tone process, the problem of circuit short Poly Si, Poly Si-GI short that may occur, and the scan signal RC delay problem caused by the thinning of the gate line have been solved. Process architecture with high process capability were used instead of difficult and low yields, and It was constructed without side effects that could not be applied to the products.

Author Keywords

Storage cap doping, Half-tone process

Introduction

Advantages of AMOLED Display, such as response speed, color reproducibility, and panel thickness are already well known. However, in terms of manufacturing cost, it is still less competitive than LCD display. In particular, the recent AMOLED display trend has changed from primium to entry-level. In the current situation where selling price is feared to be lower than cost,reducing manufacturing cost has become the most important development goal. In this study, we focus on reducing the LTPS mask, which has the largest reduction in manufacturing cost in AMOLED, and propose a method that goes from the existing top emission 8 mask to 7 mask. There have been various attempts to reduce masks in the past [3], but there have been problems such as reduced aperture ratio, increased power consumption, cross-talk, and deterioration in image quality. In this study, these disadvantages were overcome. Process with high process capability were used instead of process with difficult and low yields, and PA was successfully constructed without side effects that are not applicable to products.

In this study, cost reduction and process tact time were reduced by developing a process architecture for a 7-mask front-emitting smartphone. Poly Si under the GI Cap was also doped in the contact hole process without using a cap doping mask. Through SIMS analysis, it was confirmed that boron passing through the gate metal was injected into Poly Si. By measuring the CV curve of Poly Si-GI-Gate Cap, we succeeded in securing flat MIM characteristics. In addition, the Poly Si short circuit, Poly Si-Gate short problem that can occur in the new PA, and the scan signal RC delay problem caused by the thinning of the gate wiring have been solved. Figure 1 is the LTPS process architecture. A new 7 mask PA structure was completed by combining the role of the storage cap mask and the contact mask of the conventional PA structure.

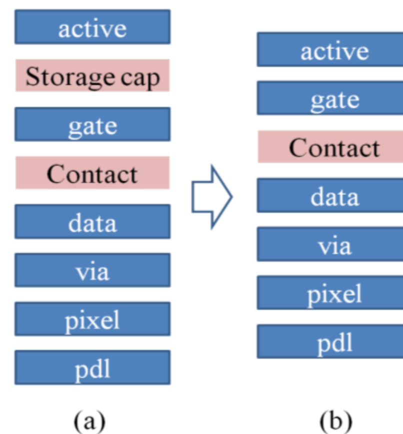

Figure1 AMOLED Back plane 7Mask PA

Experiments and Results

Figure 2 is the process flow chart. After Buffer/a-si CVD batch deposition, ELA crystallization/GI deposition was carried out, and gate metal Moly was deposited at 1500Å and then patterned. As shown in Figure 2(a), P+ doping was performed and ILD was deposited to form the source drain structure of the TFT. After that, Photo-resist was used to form a thin layer of PR on the top of the cap inlet using the half tone PR method as shown in Figure 2(b). As shown in Fig. 2(c), the ILD on the top of the cap is removed by 1st dry etching and the PR at the cap inlet is ashed (Fig. 2(d)) Then, as shown in Figure 2(e), 2nd dry etching was performed to expose Poly Si in the TFT's source drain area. The subsequent process is the cap doping process (Fig. 2(f)). Since the ILD on the upper part of the cap was opened, the poly Si under the GI was converted into P+ Poly Si by passing through the gate metal during doping.

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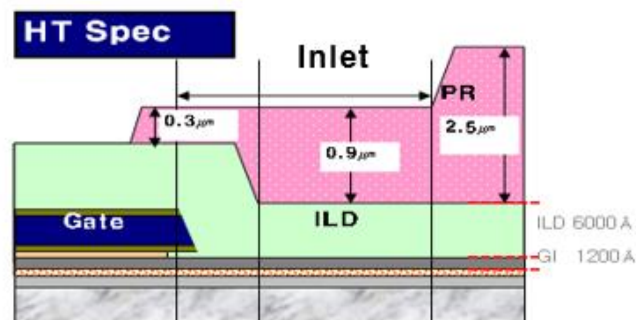
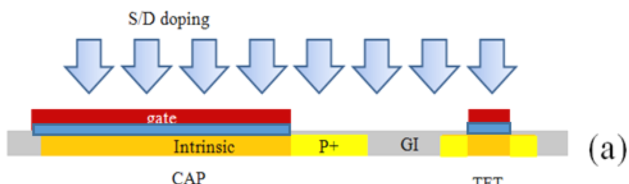
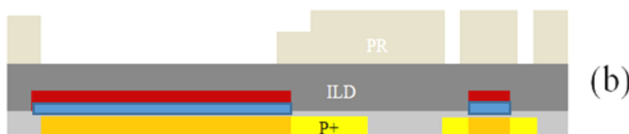
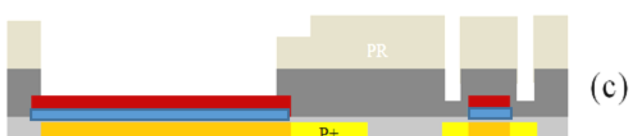
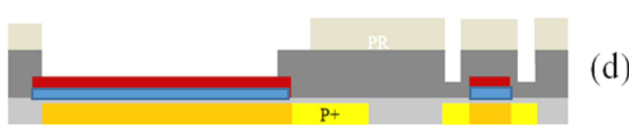
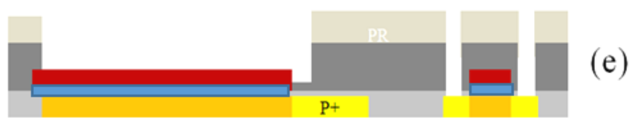












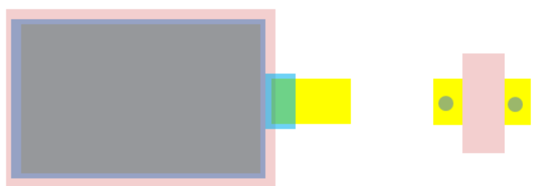


Figure 2 (a) P+ doping (b) Contact H.T (c)1st etching (d) ashing (e) 2nd etching (f) St.Cap doping

Figure 3 is a SIMS analysis image showing the boron concentration of the poly Si area after doping with 60KV impalantor in the cap using gate metal Moly 1.5K. It was confirmed that boron was detected in Poly Si through the gate metal.

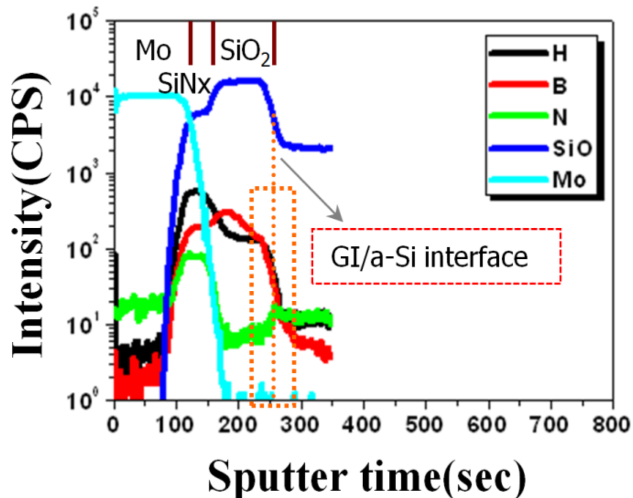
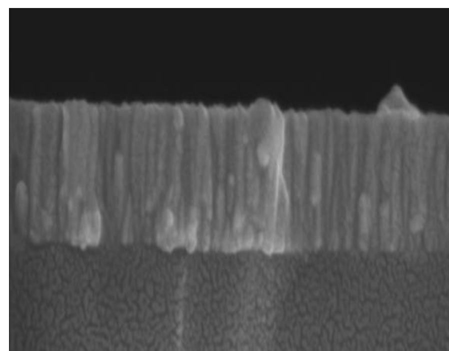
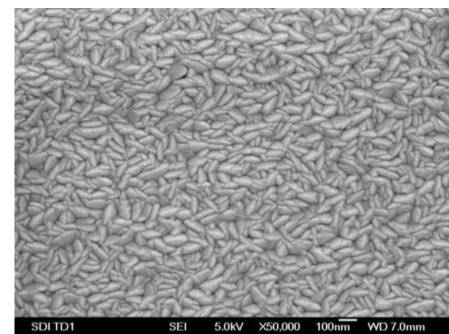


Figure 3 **Dispersion profile of boron across Moly 1.5K/GI**

As shown in Figure 4, the reason for being able to penetrate the Moly thickness of 1.5K is that the Moly thin film was grown in a columnar structure, so it was easy to pass through during doping and be injected into Poly Si.



(a)



(b)

Figure 4 (a) Mo column structure (b) Mo surface SEM image

Boron passing through Moly/GI changes the electrical characteristics of Poly Si under GI from semiconductor to conductor. By measuring the C-V curve, it was confirmed whether it had MIM (metal-insulator-

metal) characteristics. Figure 5 is the CV characteristics of the cap implanted on 1.5KÅ Moly with an ion implantor (acceleration voltage 60KV, dose 3E15). The Cap value was measured in the voltage range from -15V to 15V. It can be seen that the cap doped on top of Mo has MIM characteristics with the same flat CV curve as the cap doped on top of GI.

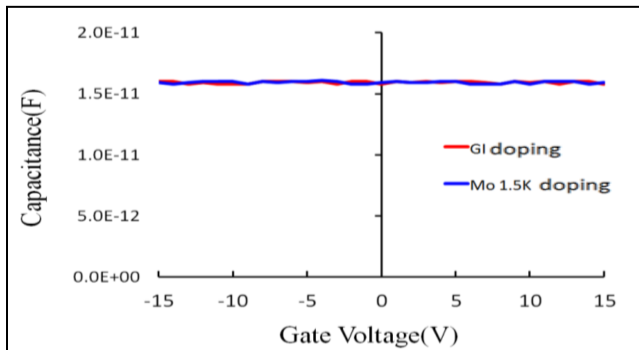


Figure 5 CV curve of cap doped on GI top and on top of Mo

In the new Process Architecture, the MIM Cap characteristics are secured, but it must be checked whether there is any problem with the signal transmission of the scan data line. QHD (Quad High Definition) resolution has 1440 pixels in one scan line, and HD (High Definition) resolution has 720 pixels. When the resolution is changed from QHD to HD in the same panel size, the cap usually decreases by 60%. Therefore, even if the resistance increases by about 60%, the RC delay can be adjusted to the same level. Since QHD PA uses Moly 2.5KÅ Gate, HD PA can be lowered to Moly 1.5KÅ Gate according to the 60% ratio. In addition, the CV curve in Fig. 6 is the data measured for TEG made by directly doping and depositing ILD on top of 1.5KÅ moly without etching the ILD. That is, the Moly thickness of the top of the cap is 1.5KÅ. However, when the ILD on the top of the cap is opened in the actual panel process, moly is also etched in the ILD etching step, and as shown in Figure 6, the moly thickness is reduced by 500~600Å, making it easier for boron to penetrate into Poly Si.
In other words, even if 2KÅ gate metal is deposited, 1.4~1.5KÅ of the actual cap upper electrode remains, making it possible to form a sufficient MIM cap. The uniformity of the sputter process is also an area to be reviewed. Considering that the deposition thickness distribution is less than 10%, when 1.8KÅ is deposited, 1.6~2.0KÅ is deposited as a whole. Then, after contact hole etching, 1.1~1.5 KÅ of moly on the top of the cap remains, and the moly thickness of the scan data line part is 1.6~2.0 KÅ as it is deposited because the ILD is not open. Therefore, it is possible to secure MIM Cap device characteristics and transmit normal scan data signals.

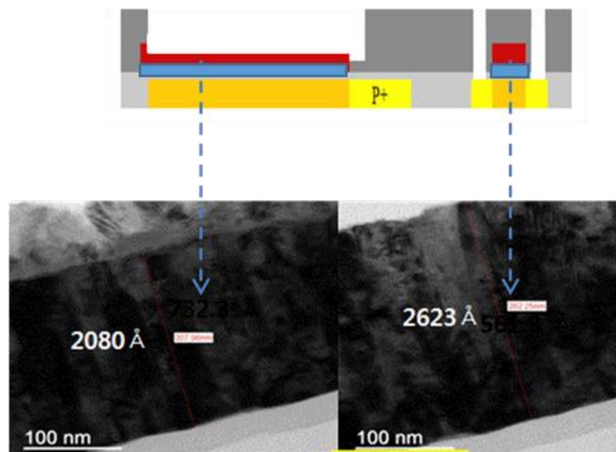
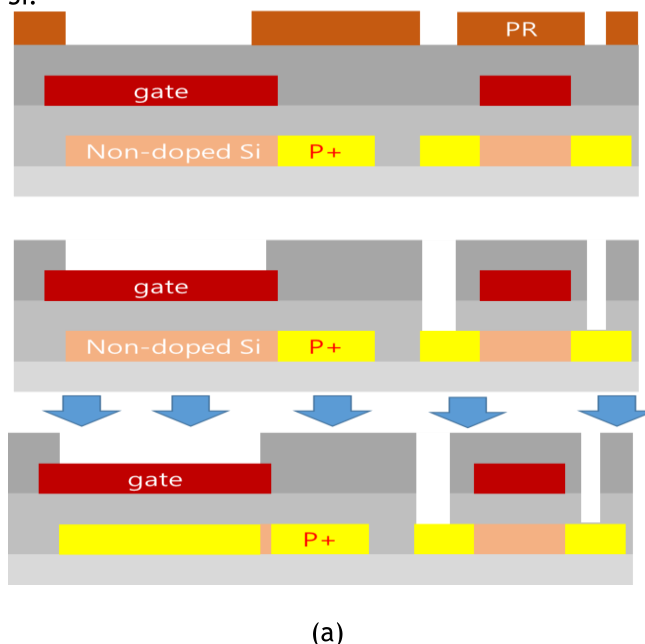
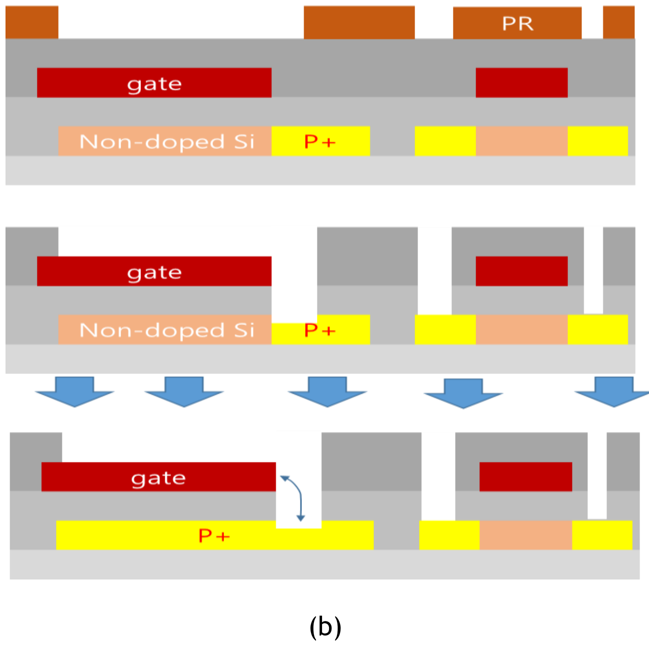


Figure 6 Mo etching SEM image of opening ILD Region

The reason for using the process architecture of Figure 7 is as follows. If Half-tone PR is not used and the ILD is designed to cover the cap lead-in end as shown in Fig. 7(a), the lead-in end is blocked by ILD during cap doping, making dopant penetration difficult. In addition, If the ILD and the gate are designed so that they do not overlap as shown in Figure 7(b), dark spots may occur due to short-circuiting of Poly Si due to exposure of Poly Si or gate-act short problem because GI cannot cover Poly Si.



(a)



(b)

Figure 7. (a) ILD and Cap inlet gate overlap structure
(b) ILD and Cap entrance gate structure isolated

Therefore, the contact hole Half-tone process developed in the 5-mask PA on the back of the TV was used. That is, the ILD is left only to the extent that Poly Si is not exposed. Therefore, problems such as Poly Si short circuit and Poly Si-gate short are solved. This Half-tone PR process is not for the purpose of adjusting CD bias or specific thickness of residual film, so it is a fair process with a wide process specification. The wide specification (0< residual ILD thickness< gate thickness) makes it easy to implement as shown in the SEM picture in Figure 8.

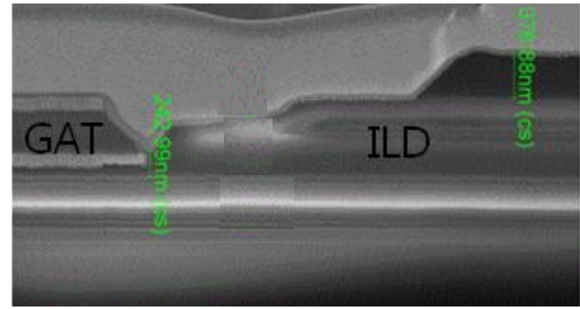


Figure 8 **SEM image of Cap inlet after half-tone process**

Conclusion

In this study, we succeeded in reducing the AMOLED backplane mask by implementing a poly Si-GI-Gate MIM cap in the contact hole process without using a storage mask. Conventional PA structure using storage mask is capable of up to 350 PPI in small and medium-sized displays, so this structure has many advantages such as high resolution and low cost.

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