Highly Robust, Dual-Gate Polycrystalline $In_{0.7}Ga_{0.3}O$ TFTs by Spray Pyrolysis for Low-Cost Manufacturing of OLED Display

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Abstract

We report dual-gate polycrystalline (Poly) $In_{0.7}Ga_{0.3}O$ thin film transistor (TFT) by spray pyrolysis (SP) process. The dual gate TFTs exhibits saturation mobility (μ_{SAT}) of ~40.23 $cm^2V^{-1}s^{-1}$ with excellent stability under bias and temperature stress (ΔV_{TH} = 0 V for PBTS, ΔV_{TH} = -0.1 V for NBTS). Furthermore, a 2.5-inch OLED display made of SP poly-$In_{0.7}Ga_{0.3}O$ has been demonstrated.

Author Keywords

Polycrystalline oxide; InGaO; coplanar TFT; high mobility and high stability; OLED display; spray pyrolysis

1. Introduction

Transparent oxides (TOs) based on the In (III) family have received significant attention as semiconductor layers for thin-film transistor (TFT) in active-matrix displays (AMDs) backplane electronics, thanks to their scalability for large-area applications, extremely low off-state currents, and cost-effective manufacturing process (1–10). The In_2O_3 itself is not suitable for the active semiconductor because of its high oxygen deficiencies. Therefore, compositions like In-Ga-O, In-Sn-O, In-Zn-O, In-Ga-Zn-O, In-Ga-Sn-O, In-Ga-Zn-Sn-O are studied extensively (2). However, the amorphous phase of these compositions cannot be able to meet the current high mobility requirement for high resolution AMOLED displays (11). To find a solution, crystalline phase of the corresponding material compositions is explored. The crystalline phase of the compositions demonstrate very high on-current compared to their amorphous counterparts(2,7,11–13). Polycrystalline (Poly) IGO is one of the best choice compared to the other compositions because of the crystallization temperature being as low as ~250°C, and the crystalline phase of both InO_6 and GaO_6 composed of edge sharing structure (2,7,11). The crystal growth mainly follow the In_2O_3 cubic bixbyite structure and the stronger Ga-O bonds provide better stability (7).

Several deposition methods, such as sputtering (2,4,11,13,14), atomic layer deposition, spin-coating and spray pyrolysis (SP) (1,3,10,12), are employed in the production of IGO thin films. Among these, SP stands out for its ability to produce large area uniform films through a cost-effective, open-air (vacuum free) process, offering simplicity and efficiency (7). The coplanar TFT structure with an offset design, which minimizes parasitic capacitance, is a more practical option for large area OLED backplanes compared to the bottom-contact, etch-stop (BCE) structure. Moreover, dual-gate coplanar structure provide very high on-current while driving in dual sweep, bulk-accumulation mode (15).

In this work, our study focuses on the poly-$In_{0.7}Ga_{0.3}O$ thin films deposited by a simple, cost-effective and environmentally stable SP process for active semiconductor. The incorporation of Ga into In_2O_3 plays a key role in regulating carrier concentration by substituting In^{3+} with a strongly bonded Ga^{3+} (7). We fabricate OLED backplane using dual-gate coplanar TFT structure, where the active semiconductor was 8 nm poly-$In_{0.7}Ga_{0.3}O$ thin films by SP. The dual gate TFT exhibits μ_{SAT}, V_{TH}, SS of 40.23 ± 3.43 $cm^2V^{-1}s^{-1}$, -0.28 ± 0.11 V, 145 ± 20 mV/decade, respectively. The poly-$In_{0.7}Ga_{0.3}O$ TFTs show negligible ΔV_{TH} of +0 V and -0.1 V under PBTS and NBTS, respectively. Moreover, under temperature dependency tests (RT to 100°C), TFTs exhibit stable performance. In addition, a 2.5 inch, 80 ppi green monochrome AMOLED display has been demonstrated, made of dual-gate coplanar SP poly-$In_{0.7}Ga_{0.3}O$ TFT backplane.

2. Experimental

A 200 nm SiO_2 buffer layer was deposited on the glass substrate using plasma-enhanced chemical vapor deposition (PECVD). Then, a 150 nm Molybdenum (Mo) deposited and patterned as bottom gate followed by a 100 nm SiO_2 deposition as bottom gate insulator (GI). Then, a 8 nm Poly-$In_{0.7}Ga_{0.3}O$ layer was deposited by spray pyrolysis at temperature of 370°C. The InGaO solution was synthesized in an N_2 glovebox environment using {$InCl_3$} and {$Ga(NO_3)_3 \cdot xH_2O$} as indium and gallium precursor and 2-methoxyethanol (2-ME) as solvent. The In:Ga proportion were 70:30. A 100 nm thick PECVD-SiO_2 and 150 nm Mo has been formed as top GI and top gate, respectively. The N+ Poly-$In_{0.7}Ga_{0.3}O$ thin film were formed by NF_3 plasma treatment. An interlayer of 300 nm thick PECVD-SiO_2 and 250 nm source/drain Mo layer was formed, followed by post-fabrication annealing at 250°C for 4 hr. A passivation layer of 200 nm SiO_2 has been deposited on top. For pixel electrode 200 nm IZO (anode for OLED) has been used followed by PSPI photoresist as OLED bank. Then, to form the transparent OLED stack, 1,4,5,8,11-

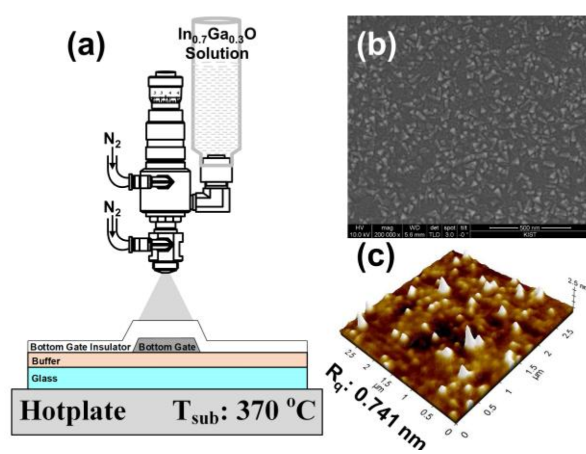

Figure 1. (a) Schematic of the experimental setup used in the spray pyrolysis (SP) deposition process on glass/buffer layer/bottom gate/bottom gate-insulator stack. (b) Scanning electron Microscope and (c) 3D Atomic Force Microscope images of the polycrystalline-$In_{0.7}Ga_{0.3}O$ thin films deposited by SP.

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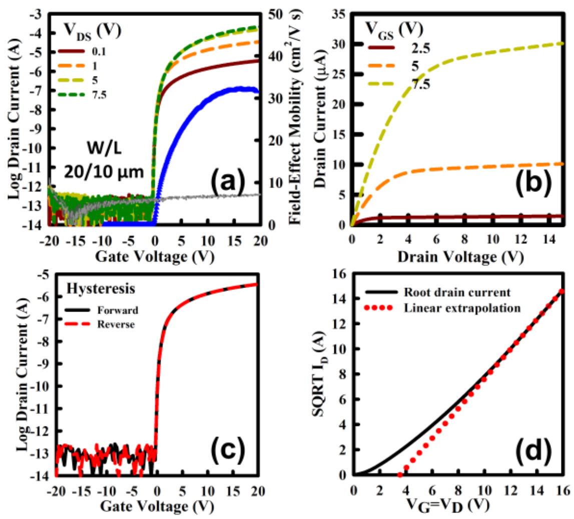

Figure 2. (a) Transfer, (b) output, (c) hysteresis and (d) square root drain current (SQRT I_D) vs (V_{DS}=V_{GS}) for the poly- $In_{0.7}Ga_{0.3}O$ TFT.

Table 1. TFT performance parameters (15 TFT devices over 15 cm × 15 cm substrate).

μ_{FE} (cm²/V.s)	30.51 ± 3.43
μ_{SAT} (cm²/V.s)	40.23 ± 2.55
V_{TH} (V)	-0.28 ± 0.11
SS (V/dec.)	145 ± 20

hexaazatriphenylenehexacarbonitrile (HAT-CN) (20 nm) as a hole injection layer, N,N′–di (naphthalene-1-yl)-N,N′-diphenylbenzidine (NPB) (50 nm) as a hole transport layer, 4,4′,4″-tris (carbazol-9-yl)-triphenylamine (TCTA) (5 nm) as an exciton blocking layer, TCTA:2,2′,2″-(1,3,5- benzenetriyl)-tris-[1-phenyl-1-H-benzimidazole] (TPBi):12% tris(2-phenylpyridinato-C2,N)iridium (III) ($Ir(ppy)_3$) (15 nm) as an emission layer, TPBi (45 nm) as an electron transport layer, and Al (100 nm) as a transparent cathode. Finally, the transparent OLED on TFT backplane was encapsulated with glass in a N_2 filled glove box (**Fig. 4**).

All electrical measurements were performed by the Agilent 4156 C semiconductor parameter analyzer in the dark at room temperature. The threshold voltage (V_{TH}) was defined as the V_{GS} corresponding to I_{DS}=W/L ×10 pA. The saturation mobility (μ_{SAT}) is derived from the slope from the plot of the square root of I_D with V_G=V_D. The TFT width (W) and length were defined from the overlap between top gate and active area. The subthreshold swing (SS) is taken as $(d\log(I_{DS})/dV_{GS})^{-1}$ of the range 10 pA ≤ I_{DS} ≤ 100pA, with V_{DS} = 0.1 V.

3. Result and Discussion

Fig 1(a) illustrates the schematic setup of the spray pyrolysis nozzle employed in this experiment. Prior to spraying, the hotplate was preheated to 370°C, and the glass / SiO_2 buffer / Mo gate / SiO_2 top-GI stack layer was mounted on it. The N_2 gas pressure was maintained at a constant level, and a steady flow rate of 0.05 mL sec^{-1} was used to ensure uniform deposition of the Poly-$In_{0.7}Ga_{0.3}O$ film over a 15 cm × 15 cm substrate. The heat flux from the preheated substrate causes the 2-ME solvent (evaporation temperature of 2-ME solvent ~180°C) in the spray droplets to evaporate into gas along with the additional chloride and nitrate ligands before reaching the surface, ensure defects free Poly-$In_{0.7}Ga_{0.3}O$ film formation. **Fig. 1(b) and (c)** shows the scanning electron microscope (SEM) and atomic force microscope (AFM) images of the corresponding Poly-$In_{0.7}Ga_{0.3}O$ thin film surface, respectively. The crystal formation with a grain size of >60 nm can be observed from SEM image, whereas the AFM image exhibits a roughness of 0.741 nm suggests a uniform growth of Poly-$In_{0.7}Ga_{0.3}O$ thin films. The crystallization process primarily relies on the rate at which the solvent in the spray droplets, containing M-O cations, evaporates. The thin-films made of spray process is environmentally stable compared to the vacuum process deposition, owing to its outside air deposition.

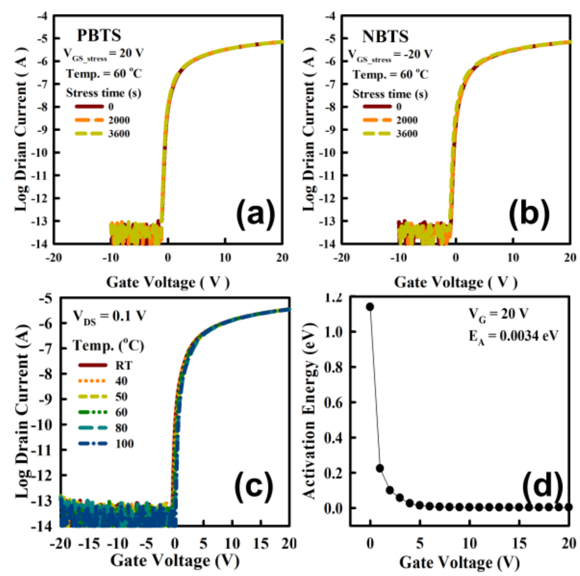

Figure 3. Evolution of the transfer characteristics under (a) positive bias temperature stress, (b) negative bias temperature stress at a constant temperature and bias of 60°C and ±20 V, respectively. (c) Temperature dependent transfer characteristics (RT to 100°C) and (d) extracted activation energy (E_A) using Arrhenius equation.

Fig. 2(a) and (b) shows the transfer, gate-leakage (V_{DS} = 0.1, 1.0, 5, and 7.5 V), field-effect mobility (μ_{FE}) at V_{DS} = 0.1V, and output (V_{GS} = 2.5, 5, and 7.5 V) characteristics of the dual-gate coplanar Poly-$In_{0.7}Ga_{0.3}O$ TFT (W/L = 20/10 μm). Uniform TFT performance was achieved with the μ_{FE}, saturation mobility (μ_{SAT}), V_{TH}, SS of 30.51 ± 3.43, 40.23 ± 2.55 $cm^2V^{-1}s^{-1}$, -0.28 ± 0.11 V, 145 ± 20 mV $decade^{-1}$, respectively **(Table 1).** A total of 15 TFTs chosen from the 15 cm × 15 cm substrate exhibit a very small standard deviation, suggesting excellent uniformity, which are critical for OLED performance. **Fig. 2(c)** presents the hysteresis behavior of the corresponding TFT with a V_{GS} sweep voltage of ±20 V and a V_{DS} of 0.1 V. No variation in V_{TH} was observed between the forward and reverse sweeps, indicating the absence of hysteresis. Square root drain current (SQRT I_D) at V_{GS} = V_{DS} sweep voltage has been demonstrated in **Fig. 2(d)** to extract the saturation mobility, μ_{SAT} of the corresponding TFT.

The evolution of transfer characteristics under positive bias temperature stress (PBTS) and negative bias temperature stress (NBTS) were carried out on the dual-gate dual-sweep coplanar TFT device at $V_{GS\text{-}stress}$ = ± 20 V at the temperature of 60°C as

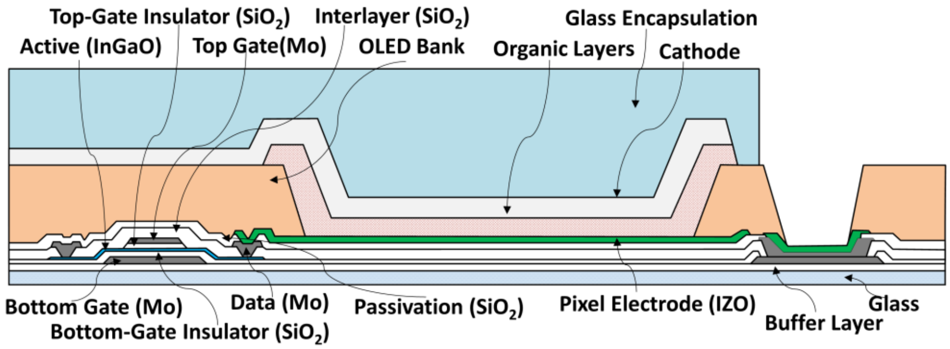

Figure 4. Cross-sectional schematic of display pixel of a 2.5-inch OLED using dual-gate poly-$In_{0.7}Ga_{0.3}O$ TFT and transparent OLED with an IZO/HAT-CN/NPB/TCTA: TPBi:12% Ir $(ppy)_3$/TPBI/Al.

shown in **Fig. 3(a) and (b)**, respectively. No shift under PBTS and a negligible ΔV_{TH} of -0.1 V has been observed under NBTS, suggesting defects free poly-$In_{0.7}Ga_{0.3}O/SiO_2$ GI interface formation. **Fig. 3(c)** demonstrates the evolution of transfer characteristics of the corresponding TFT under various temperature (RT to 100°C). A very negligible ΔV_{TH} of +0.2 V was observed. Moreover, activation energy (E_A) calculated from the temperature dependency data shows in **Fig. 3(c)** and exhibits in **Fig. 3(d)**. E_A of 3.4 meV can be observed at V_{GS} of 20 V suggests a very small conduction band offset suggests very easy carrier accumulation at the active/GI interface.

As shown in **Fig. 5,** we demonstrate a 2.5-inch array (160 × 120), OLED display based on dual-gate SP Poly-$In_{0.7}Ga_{0.3}O$ TFTs. The cross-sectional schematic of the dual gate TFT and OLED fabrication has been demonstrated in **Fig. 4** and explained in the experimental section. The photograph of the prototype panel is shown in **Fig. 5**. Green monochrome, OLED could be seen with conventional two transistors and one capacitor (2T 1C) pixel design.

4. Conclusions

In conclusion, dual gate coplanar Poly-$In_{0.7}Ga_{0.3}O$ TFTs by spray pyrolysis have been successfully fabricated. Since spray-pyrolysis is a vacuum-free process, therefore it is a cost-effective method. Mobility over 40 $cm^2V^{-1}s^{-1}$ with its excellent bias temperature stabilities shows its robustness. The demonstration of 2.5-inch OLED display suggests the excellent uniformity of the SP poly-IGO TFTs for large area AMOLED display application.

Figure 5. A picture of 2.5-inch 80 ppi AMOLED display.

5. Acknowledgments

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