Next-Generation Capacitive Fingerprint Sensing Device Using IGZO TFT Technology

Toru SAKAI[1], Eric DERCKX[1], Rob VAN LIER[1], Peter NOTERMANS[1], Said LOUDAGH[1], Kohichi OHHARA[2], Kohhei TANAKA[3], Masayuki HATA[3], Akinori KUBOTA[3], Shinichi MIYAZAKI[3]

[1]Touch Biometrix Ltd., Eindhoven, The Netherlands, [2]Sharp Display Technology Corporation, Mie, Japan, [3]Sharp Corporation, Osaka, Japan

ABSTRACT

The indium gallium zinc oxide (IGZO) TFT technology was applied to realize a next generation capacitive fingerprint sensor. Implementing a novel active pixel architecture in combination with a proprietary Read Out Integrated Circuit (ROIC), a sensing array of 1600 × 1500 pixels with 500ppi resolution has been successfully realized and it can deliver outstanding quality fingerprint image.

Keywords

IGZO TFT Technology; Capacitive Fingerprint Sensor; Active Pixel Architecture; ROIC; MUX

1 Introduction

Fingerprint sensing devices nowadays have been widely used as one of the key biometric identification and authentication methods. Whilst there are a numerous number of principles being studied and/or materialized into various products to sense the fingerprints, among others, a capacitive sensing technology began to be applied to not only industrial products but also consumer ones.

Conventional capacitive sensors currently available in the market, however, are normally manufactured by using Silicon wafer technology. Due to the cost of manufacturing, inherently the dimensions of the sensor chip tend to be rather small and, since Silicon is quite rigid, it will make it hard to integrate such a chip into various products, especially flexible ones.

In this paper, to realize the next generation capacitive fingerprint sensor built on glass substrate, we will present a novel active pixel architecture, the potential of IGZO TFT technology to be applicable to the capacitive sensing device and the overview of a proprietary ROIC technology specifically developed for this active pixel architecture.

2 Technology

The capacitive fingerprint sensors generate a fingerprint image by sensing the difference in capacitance between the ridges and the valleys that make up the fingerprint, as depicted in Figure 1.

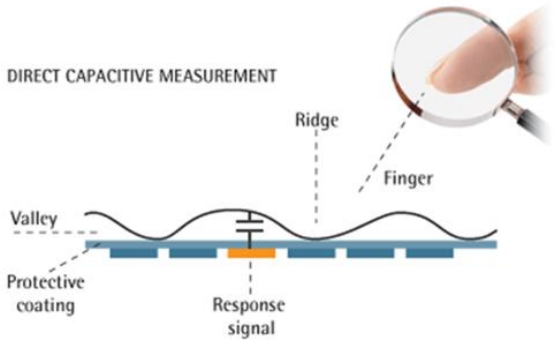

Figure 1 Measurement principle of capacitive fingerprint sensor

2.1 Active Pixel Architecture

Normally the difference in capacitance between the ridges and the valleys is extremely small such as few attofarads per μm^2. A specific detection principle with exceedingly high sensitivity is therefore required to realize a capacitive fingerprint sensing device. To achieve such high sensitivity of the detection while maintaining the versatility and the scalability of the technology, a novel 3T1C active pixel circuit is developed as depicted in Figure 2.

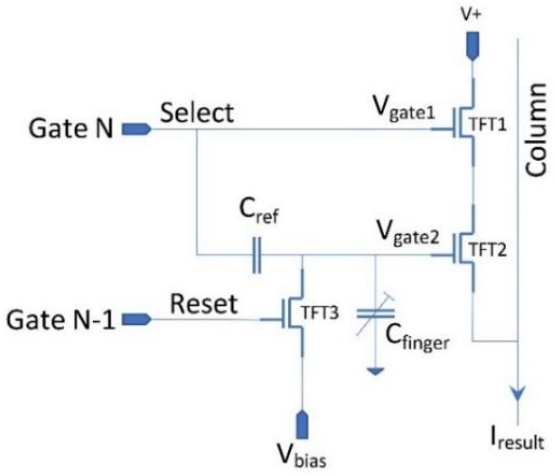

Figure 2 A novel 3T1C active pixel circuit

The timing diagram for driving and sensing from the novel 3T1C active pixel circuit is depicted in Figure 3.

ISSN 0097-996X/25/5601-0534-$1.00 © 2025

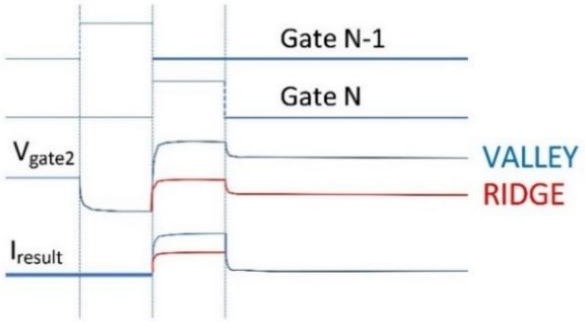

Figure 3 Timing diagram for the novel 3T1C active pixel circuit

Within the circuit, TFT1 selects the pixel to activate for sensing the capacitance, TFT3 resets the pixel prior to the activation for sensing and TFT2 serves to amplify the voltage applied to its gate, which is the gate voltage divided in the ratio among the capacitances associated with its gate, into the current by acting as a source follower.

In this circuit, the gate signal for the preceding gate line ("Gate N-1") is utilized to turn TFT3 on for setting the capacitances connected to the gate line of TFT2 at the fixed voltage prior to starting to sense the capacitance. Afterwards the sensing sequence will immediately start by turning TFT1 on and this will make sure that the 'live' capacitance will be measured by the sensing electrode connected to the gate line of TFT2.

When the ridge touches the sensing electrode, the electrical capacitance associated with the finger (C_{finger}) will reach the maximum value and it will lead to the sensing current (I_{result}) at the least value. In contrast, when the valley approaches over the sensing electrode, C_{finger} will become lower resulting in higher I_{result}.

In the case of an active addressing sensing device, generally when one pixel is active to sense the signal, all other pixels connected to the same column, i.e., data sensing line, shall be kept 'quiet' at off-state to maximize the signal-to-noise ratio. Whilst there are various components to potentially contribute as a noise source, among others the leakage current through a TFT at the off state is identified as the primary component to be contained.

Because of this reason, an IGZO TFT technology is deliberately chosen to realize the novel 3T1C pixel circuit since an IGZO TFT is known to have the extremely low leakage current in the off-state, i.e., the off-state current per µm in Channel W of IGZO TFT can be 10^{-25}(A/µm) as reported by S. Yamazaki et al. [1]

2.2 IGZO TFT

IGZO TFT Technology to realize the technology presented in this paper is fully matured and it has been released for mass production on G4.5 flat panel display manufacturing line for years.

The typical characteristics and the key parameters of the IGZO TFT, which is applied in the MUX circuitry of the sensing array in this exercise, are depicted in Figure 4 and Table 1, respectively.

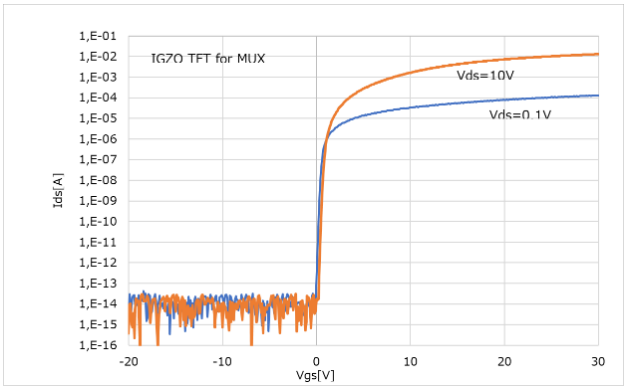

Figure 4 Typical transfer characteristics of IGZO TFT

Table 1 Key parameters of IGZO TFT

Parameter	Unit	IGZO TFT for MUX
Channel L	µm	7.5
Channel W	µm	800
μ_{FE} @Vds=10.0(V)	$cm^2/(V \cdot s)$	>18
Vth @Vds=10.0(V)	V	<2

As described hereinbefore, in comparison with any other TFT technologies, the leakage current of IGZO TFT in the off-state is extremely low as exhibited in the characteristics, which is far below the measurement limit.

2.3 ROIC

The ROIC block diagram is depicted in Figure 5 and the high-level features are summarized as follows. [2]

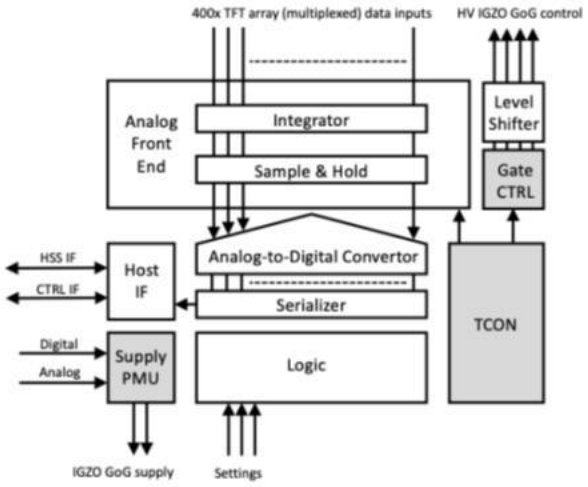

Figure 5 ROIC block diagram

The main features of the ROIC:

- 400 input current-to-digital readout channels
- 10-bit resolution per channel
- Fast 10µs and low-noise pixel conversion
- 3-phase pipeline cnfiguration of Integration, Sample & Hold and Analog-to-Digiital Conversion
- Ultra-compact (20µm pitch)
- Fast acquisition time
- 60ms for full FAP60 (2.4Mpels) read-out
- TFT gate drivers for Gate-on-Glass (GoG) scan and MUX-on-Glass (MoG) control
- Low power consumption
- Small footprint

2.4 Multiplexer (MUX)

2.4.1 Image Build

The ROIC developed dedicatedly to the active pixel architecture is designed to control the MUX-on-Glass (MoG) circuity up to 1:12 ratio, i.e., up to 4800 signal outputs from the sensing array. In the exercise described in this paper, as the number of signal outputs from the sensing array is 1600, 1:4 ratio MUX design is applied.

Because of the usage of a MUX, one full frame image will need to be built using a number of subframes, i.e., in this exercise 4 sub-frames. We deliberately chose a read-out strategy by which the subframe will be built by a 'bundle' of one out of four sensing lines. In another word, when one channel of MUX is open, the signal from the pixels connected to the sensing line will be read out one by one along the sensing line.

2.4.2 MUX Configuration

The number of signal outputs from the sensing array to the ROIC can be significantly reduced by using a MUX circuity. Because of the working principle of the MUX, only one sensing line is selected by opening only that corresponding one channel of the MUX and consequently the three other lines connected to the three other channels of the MUX will inevitably float electrically. To reduce the total amount of noise generated by any parasitic capacitance associated with the floating sensing lines, a resolute configuration of the MUX circuity was developed and applied as depicted in Figure 6.

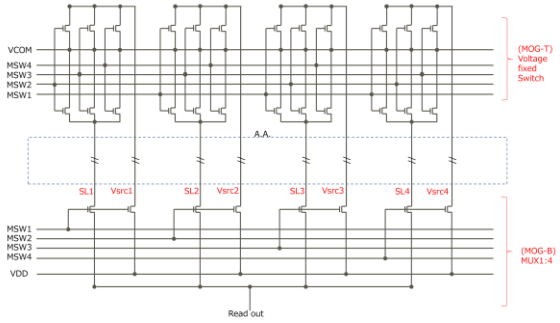

Figure 6 MUX configuration

Using this circuity, the non-selected sensing lines can be hooked up to any fixed potential. To minimize the noise level, in this exercise the same potential at the input of the ROIC is applied to all non-selected sensing lines during operation. Consequently, the configuration can also lead to the significant reduction in the power consumption of the sensing array.

In this regard, due to the high line impedance, the double gate IGZO TFT is specifically applied in the MoG circuitry because of its high current drive capability and the double gate IGZO TFT realizes the stable readout operation.

2.5 Half Module

A half module, i.e., the IGZO TFT sensing array equipped with the novel active pixel circuit and interconnected with the proprietary ROIC as chip-on-foil (COF), is realized as depicted in Figure 7.

Figure 7 Half module

The sensing array consists of 1500 gate lines driven by the GoG circuitry and 1600 sensing lines connected to the single ROIC with help of using the 1:4 MoG circuitry.

2.6 Demonstrator and Target Sensor Specification

The demonstrator, which contains the half module and a dedicated PCB which drives the half module and reads out the raw digital sensor pixel data from the ROIC, is built as depicted in Figure 8.

Figure 8 Demonstrator

The target specification of our first product, which will be the consciously optimized version based on the demonstrator, is summarized as follows.

The target sensor specification:

Active sensing area	81.3mm(H) × 76.2 mm(V)
Active sensing pixels	1600(H) × 1500(V)
Resolution	500ppi
Bare sensor thickness	0.5mm (glass)
Grey scale levels	1024 (10bit raw data)
Scan rate	15fps max
Interface to host	USB
Supply voltage	5V
Power max	<150mW at 15fps
Energy per frame read-out	<10mJ
Quick startup option	<1ms
ESD protection	IEC6100-4-2 - ±15kV
Hardness	≥6H (Pencil Hardness)
Operating temperature	-10 to +55 °C
Storage temperature	-40 to +80 °C
Compliance	FBI-EBTS Appendix F

3 Results

A typical example of the fingerprint image captured by the demonstrator is depicted in Figure 9.

Figure 9 The fingerprint image

Because of the high sensitivity of the novel active pixel architecture with 500ppi resolution, not only the fingerprints but also the sweat pores in the ridges are clearly visible in the captured image.

As 10bit Analogue-to-Digital conversion is performed on the signal from the sensing array, the dynamic range in this architecture is expected to be at least 60.2dB.

3.1 Analysis of the raw image data

The raw image data out of the sensor is 1600 × 1500 × 10bit. Figure 10 exhibits the histogram analysis of the fingerprint image depicted in Figure 9.

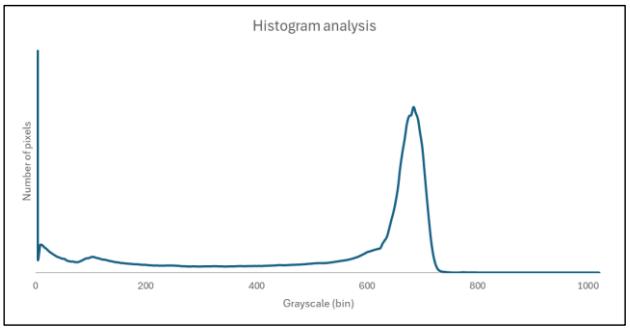

Figure 10 Histogram analysis

3.2 Low power performance

The maximum power consumption measured for full image 1600 × 1500 × 10bit scanning at 15 frames per second read-out is less than 150mW. Calculating it back to a single image read-out, the result is less than 10mJ of energy per frame.

4 Conclusion

Using the IGZO TFT technology, the next generation capacitive fingerprint sensor technology grounded on the novel 3T1C active pixel architecture is developed and the 3.2" × 3.0" technology demonstrator with 500ppi resolution has been successfully realized.

The evaluation of the demonstrator firmly verifies that (1) the IGZO TFT technology is the ideal platform to realize such a sensing device, which enables to detect extremely low current, and (2) the working principle of the active pixel architecture and the read-out technology as described in this paper are genuine.

Since it is developed in the existing fully matured IGZO TFT mass-manufacturing line, TRL (Technology Readiness Level) of the technology to industry release is inherently superb and it can also be implemented for flexible version with a potential scalability to any size, form factor or surface.

5 Acknowledgement

To develop the specific ROIC for our application, Touch Biometrix et al. express their sincere gratitude to SystematIC design B.V. (NL) for their excellent expertise on the design and implementation of sensor read-out circuitries.

6 References

[1] Yamazaki S, et al., "Properties of crystalline In-Ga-Zn-oxide semiconductor and its transistor characteristics", Jpn. J. Appl. Phys. 53, 04ED18 (2014)

[2] Sakai T, Derckx E, van Lier R, Notermans P, Loudagh S, "Touching is Believing" – The Next Generation Capacitive Fingerprint Sensing Technology, IDW '24 [FLX3-1] (2024)