Design of Micro-OLED Display Driver with OS/Si Structure Enabling Control of Multiple Functions Using 4 CPU-Embedded Drivers in Si Layer

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Abstract
We designed a 1.5-inch, 5009-ppi OLED display with a pixel array and drivers monolithically stacked using an OLED/OS/Si structure (OS: oxide semiconductor). The display also includes IR sensors. The drivers are compatible with foveated rendering and incorporate control circuits for this feature, enabling a 79.8% reduction in power consumption of analog circuitry.

Author Keywords
CAAC-OS; Si; Microdisplay; OLED; High-definition; Display driver; CPU; Foveated rendering; IR sensor

1. Introduction
The market of microdisplays as augmented reality (AR) and virtual reality (VR) head-mounted displays is expected to grow significantly. To resolve phenomena that cause discomfort to users, such as the screen-door effect [1,2], high definition, high pixel aperture ratio, and high frame rate are required as display performance. For this reason, demands have increased for silicon-based micro-organic-light-emitting-diode (micro-OLED) displays with higher definition [3,4].

A high-definition display with more than 5000 ppi and a pixel circuit configuration of four transistors and one capacitor (4T1C) using *c*-axis-aligned crystalline oxide semiconductor (CAAC-OS) field-effect transistors (FETs) has also been reported [5]. The CAAC-OS FETs can be monolithically stacked over silicon (Si) FET circuits, and OLEDs can be further stacked as the top layer (an OLED/OS/Si structure). The 55-nm Si complementary metal oxide semiconductor (CMOS) circuit in this structure increases the flexibility of display driver layout and enables on-chip implementation of multiple functions. For example, it has been proposed to incorporate the idea of foveated rendering into a display driver control system to reduce the overall power consumption [6]. The foveated rendering technique attracts attention for low-power VR displays but leads to a heavy load on peripheral circuits and a large device size with the placement of an integrated circuit. To make a compact VR device with a smaller number of components, peripheral circuits can be formed in the Si layer in the OLED/OS/Si structure. Like low-temperature polysilicon and oxide (LTPO) FETs [7], OS FETs formed over a silicon substrate exhibit a low off-state current [8], which also contributes to power reduction.

It is known that the user blinks less frequently when focusing on the screen for tasks requiring high concentration than when not [9]. Infrared (IR) sensors are incorporated in the display of this work to know the condition of user's eyes.

In this paper, we propose a new display driver for a high-definition VR microdisplay with the OLED/OS/Si structure, which achieves low power consumption by foveated rendering and has sensing capability.

2. OLED/OS/Si Monolithic Structure
Figure 1 shows the concept of the display with the OLED/OS/Si structure. The OLED/OS/Si display consists of a Si layer with functional circuits including display driver circuits, an OS layer with a pixel array above the Si layer, and an OLED layer as the top layer. The Si functional circuits can be laid out throughout the entire Si layer. This enables high flexibility in circuit layout and on-chip implementation of multiple functional circuits. Specific effects of the OLED/OS/Si structure are described below.

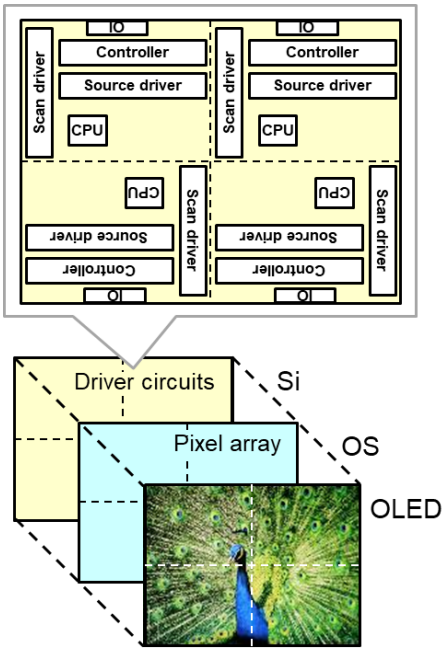

Figure 1. Display with OLED/OS/Si structure.

To improve the display definition with the OLED/Si structure, it is necessary to reduce not only the pixel pitch but also the control driver output pitch. In conventional configurations, drivers are placed at the periphery of the pixel array, which raises issues such as pitch limitations dependent on process nodes and increases in bezel size due to the placement of multiple drivers. In the OLED/OS/Si display, source drivers are provided separately for red, green, and blue (RGB), among which the source drivers in the upper and lower parts of the planar layout respectively drive source lines in odd- and even-numbered columns. Owing to this configuration, the high-density pixel array can be controlled even when the source driver output pitch is wider than the pixel pitch.

High-definition displays require a large amount of frame data, resulting in increasing the power consumption of the display driver with increasing frame rate. To address this issue, we propose incorporating into the display driver foveated rendering, in which high-definition display is performed only in the user's

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gaze area. With the OS/Si structure, gate lines can be divided at the boundaries of divided display areas, and the outputs of scan drivers in the lower layer can be supplied to the pixel circuits in the upper layer for controlling each display area. By contrast, the source lines are not divided at the boundaries of the display areas because the operation of the source drivers only needs to be logically controlled according to the resolutions set for the display areas selected by the scan drivers. By combining this technique with viewpoint detection processing, high-definition display can be efficiently performed only in the user's gaze area. In low-definition display areas, power consumption by circuit operation can be reduced.

The OLED/OS/Si structure can expand the functionality of the Si circuits. To maximize this feature, a control system that collectively controls multiple circuit functions is crucial. General-purpose circuits such as central processing units (CPUs) or field-programmable gate arrays (FPGAs), which can change their arithmetic processing through programming, are effective control means. For example, CPUs can freely execute different types of processing by changing software programs and can easily fulfill the requirements for system functions. This enables on-chip implementation of functions such as interrupt processing caused by sensor signals, sensor signal processing with an analog-to-digital converter (ADC), and amplifier offset compensation. Even if a CPU does not perform arithmetic processing at the same speed as data processing by the display driver, it can perform many functions for its footprint, which is more area-efficient than implementing multiple dedicated circuits for the functions.

These advantages can be obtained with the Si layer of the OS/Si structure. The advantage of the pixel array in the OS layer is no area restriction due to the placement of the peripheral circuits, which allows effective use of the size of one shot of an exposure tool and enables a size as large as 1.5 inches.

Hence, we designed an OLED/OS/Si display with specifications shown in Table 1. The display is formed by monolithically stacking the Si drivers fabricated using a 55-nm high-voltage (HV) CMOS process, the OS pixel circuits fabricated using a 130-nm CAAC-OS process, and OLEDs as display devices. The display has a size of 1.5 inches and a high resolution of 5009 ppi with 6000 × RGB × 4500 pixels.

Table 1. Display specifications.

Screen diagonal	1.5 inches
Resolution	6000 × RGB × 4500
Pixel size	5.07 μm × 5.07 μm
Pixel density	5009 ppi
Structure	OLED / OS / Si
Si CMOS process	55 nm HV Logic: 1.2 V, Analog: 6.0 V
CAAC-OS process	130 nm
Refresh rate	90 Hz
Source and Scan drivers	Integrated
IR sensors	Integrated

3. Design of CPU-Embedded Display Using Foveated Rendering

Design details are described in this section. Figure 2 shows the floor plan of the Si driver block. The Si circuit layer is constituted by four independent Si driver blocks. Each Si driver block includes an input/output (IO) circuit, a low-voltage differential signaling (LVDS) circuit (3 clock lanes, 24 data lanes), an inter-integrated circuit (I^2C) interface, a controller, source and scan drivers, a CPU (Cortex-M0), and temperature sensors. Internal logic parameters for controlling the resolution and frame rate are set to registers using the CPU, I^2C, and LVDS (data lanes). The controller is responsible for generating driver control signals and adjusting data transfer timing, for example. The scan drivers each output control signals for four gate lines. Display control is performed for each of 6 × 8 display blocks divided in the source and gate line directions; each display block corresponds to 750 × RGB × 750 pixels. The source lines are driven by a single source driver without being divided for each display block. By contrast, the gate lines are divided at the boundaries of the display areas and are driven by individual scan drivers, thereby reducing output wiring load. This configuration enables independent control of the display resolutions of the 48 divided display blocks.

The source drivers are provided separately for RGB to perform separate control. Since video data for each color is transferred unit by unit, logic transitions due to charging and discharging of the video data bus can be reduced. Additionally, the multiple source drivers are arranged two-dimensionally; thus, source potentials can be supplied to pixels with a narrower pitch than the output pitch of each source driver.

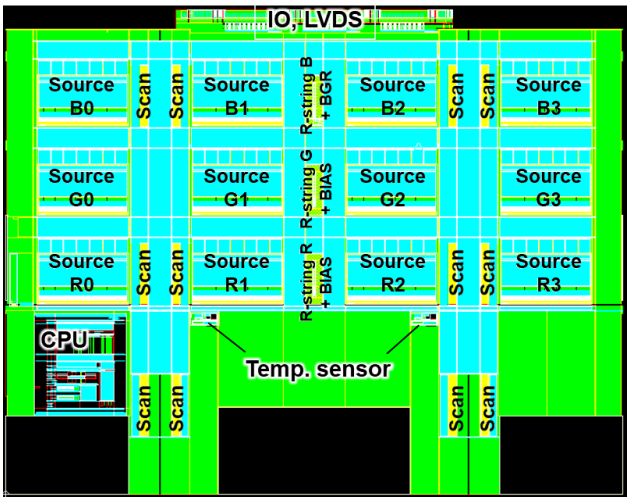

Figure 2. Floor plan of Si driver block.

Display control operation assuming foveated rendering is now explained using a block of 12 × 12 pixels shown in Figure 3. The display resolution can be changed between three levels: High Resolution (1 × 1), Low Resolution 1 (the same display with all 6 × 6), and Low Resolution 2 (the same display with all 10 × 10); here, the operation for Low Resolution 1 is described. As shown in Figure 3, source data that is output from the same amplifier is supplied to adjacent pixels of the same color. Amplifiers that do not need to supply data and their input logics can be put into a power-saving mode by standby operation and clock-gating. Standby and recovery operation can be performed at the time of changing the display control areas.

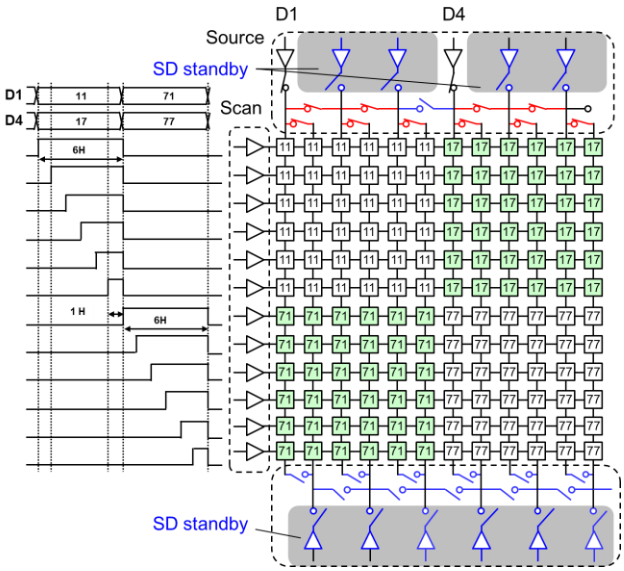

Figure 3. Driver control for Low Resolution 1.

For the resolution control by the source drivers, amplifier standby operation and output-node analog switch on/off operation are performed simultaneously. Note that the source lines in the odd- and even-numbered columns receive video data from different source drivers only in high-resolution display. In low-resolution display, the source drivers on one side supply video data to all pixels. Additionally, owing to individual offset compensation, the amplifiers do not affect image quality even in low-resolution display.

The operation of the scan drivers in low-resolution display is achieved by adjustment of the pulse width of selection signals through logic control. For the 6 × 6 display resolution, the selection period is set to 6 horizontal periods for the first scan line, 5 horizontal periods for the second scan line, and one horizontal period for the last sixth scan line of each unit, for example. In that case, one amplifier charges and discharges 6 source lines and 36 selected pixels.

4. Control System with Embedded CPU

Figure 4 shows the configuration of the control system with the CPU. The display driver includes four CPUs. Functions controlled by the CPU include setting display driver parameters, obtaining temperature sensor outputs, obtaining IR sensor outputs for eye fatigue detection, obtaining amplifier offset compensation values, and setting compensation data for the display driver. These functions were incorporated in this study for the demonstration of the control system. Another conceivable configuration for further multi-functionalization is that a circuit that should operate at the same speed as video data processing by a driver is included in the driver, while the function of a circuit that performs low-speed processing, such as a sensor, is processed by the CPU.

In the proposed display, the display driver can change its circuit operation based on parameter values, and thus the operation states of the drivers can be controlled by the CPU. However, if parameter transmission from the CPU and reflection in the display driver are synchronized, constraints will be imposed on these operations. To avoid this, pre-registers are provided in the display driver, and the CPU sets parameters for the next frame in advance. Flexible parameter control between the CPU and the drivers can be achieved by loading the parameters from the pre-registers at the desired time for reflection in the drivers. With this configuration, the CPU can control display resolution parameters in synchronization with the driver operation.

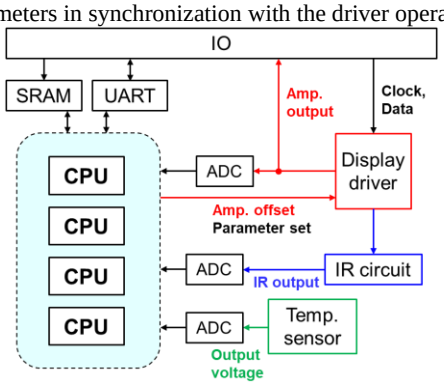

Figure 4. Control system with CPU.

5. Design Specifications of Sensor

According to previous studies, the times for eyelid opening and shutting change between normal and fatigue conditions [9]. The eye closing time under the normal condition is approximately 100–150 ms, whereas it is 50–200 ms longer under the fatigue condition. A difference of 50 ms between the eye closing times can be detected with a measurement interval as short as 25 ms. Thus, this display includes OLEDs as an IR emitting unit and organic photodetectors (OPDs) [10] as an IR receiving unit, as shown in Figure 5. Control signals for the IR emitting and receiving units are generated by the logics of the display driver.

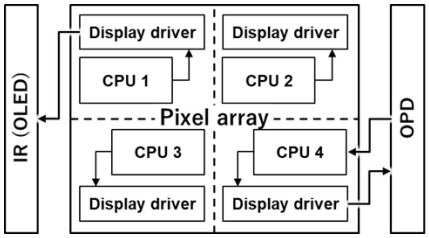

Figure 5. Block diagram of display.

The circuit diagram of the IR receiving unit is shown in Figure 6. IR light received by the OPD is converted into an electric current, and the output is read by a source follower. Figure 7 shows the result of a simulation assuming eyelid opening and closing. With an exposure time of 14 ms, output node OUT exhibits a difference of 32 mV depending on whether the eyes are open or closed. This difference in output is satisfactorily large for the resolution of the ADC (8 mV) of the embedded CPU and is large enough to detect the eye open/closed state in less than 25 ms. Feedback on the user's fatigue condition can be provided by storing data on the eye open/closed state in the CPU's internal memory every 25 ms and calculating changes in the eye closing time.

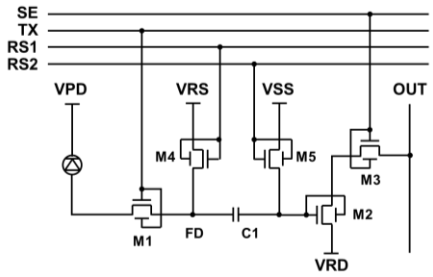

Figure 6. Circuit diagram of IR receiving unit.

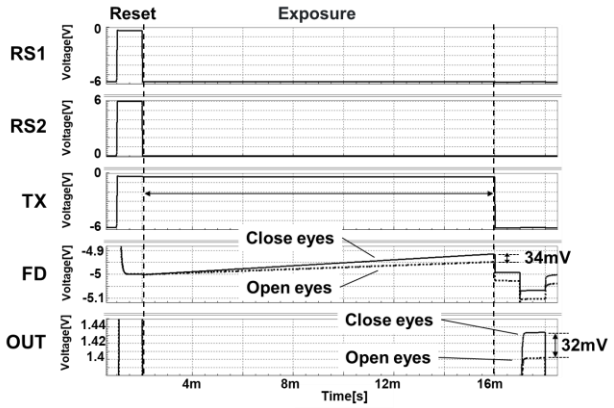

Figure 7. Simulation with IR circuit assuming eyelid opening and shutting.

6. Fabricated OLED/OS/Si Panel

Figure 8 shows a photograph of an image displayed on the fabricated panel, which has a display region of 30.42 mm × 22.815 mm. Image display was achieved using the high-definition OLED/OS/Si display.

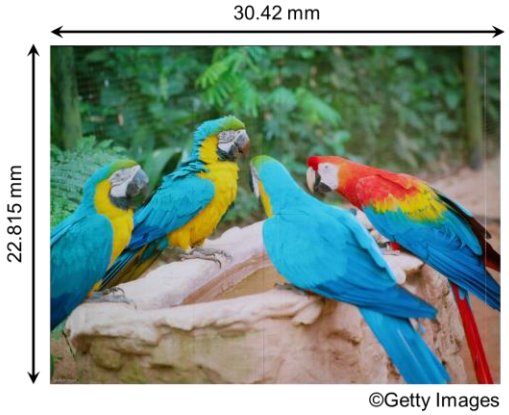

Figure 8. Photograph of image displayed in normal mode.

Table 2 shows the measured power consumption in two display operation modes: a normal mode at High Resolution (6000 × 4500), and a foveated mode at High Resolution in the gaze area (4 blocks at the center of the screen) and lower resolutions (Low Resolution 1 in 12 blocks and Low Resolution 2 in 32 blocks) toward the periphery (Figure 9). The measurement results reveal that the power consumption of analog circuitry in the foveated mode at 60 Hz is 79.8% less than that in the normal mode at 60 Hz, which is effective in reducing power consumption. The amount of the reduction achieved corresponds to the proportion of amplifiers stopped in the foveated mode (80%).

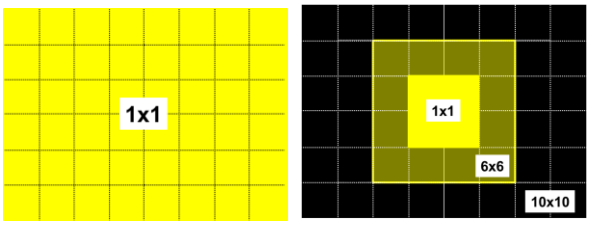

Figure 9. Resolution of each display area in normal (left) and foveated (right) modes.

Table 2. Power consumption of analog circuitry in each display mode.

	Normal	Foveated	Unit
Analog	1225	248	mW

7. Conclusion

We designed the high-definition, multi-functional display using the OLED/OS/Si structure, i.e., the 90-Hz, 1.5-inch, 5009-ppi OLED display with the monolithic stack of the pixel array and the drivers. Additionally, we measured the power consumption of the display driver of the fabricated panel and demonstrated the effect of reducing power consumption by resolution control for each display block in hardware, utilizing the foveated rendering technique. The display further incorporates the IR emitting and receiving units, and the feasibility of detecting differences in eyelid opening and closing times has been confirmed by simulation. The processing is controlled by the embedded CPUs. In future work, the OLED/OS/Si structure will be used for on-chip implementation of circuit functions closely related to display, which would contribute to improving the performance of AR/VR displays.

8. References

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