# Research and Optimal Driving Methodology for Image Quality Defects Occurring in 4K 1.3-in. OLEDoS

*Seongan Park*, Wonhee Lee*, Jinwoo Park*, Sangmyeon Han*, Jaebeom Choi**
*Samsung Display, Yongin, South Korea

## Abstract

***The demand for extended reality (XR) has been increasing rapidly, necessitating advancements in display technology. OLED on Silicon (OLEDoS) has emerged as a critical solution for XR applications due to its high integration and operation speed. However, compared to conventional mobile pixel circuits, OLEDoS behaves differently due to two key factors: The first is the capacitor dividing method of data write, which induces strong horizontal crosstalk. The second is the small storage capacitance compared to parasitic capacitance, which causes fast degradation, low step efficiency, and high temperature sensitivity.***

***In this study, we identified the mechanism of horizontal crosstalk in a 1.3-inch 4K OLEDoS display and applied theory-based tuning to achieve high-quality crosstalk specifications. Additionally, we introduced an anode coupling model that accurately predicts the effects of degradation, step efficiency, and temperature sensitivity. Through these analyses, we established an optimal driving methodology to address image quality defects and significantly contributed to the commercialization of micro-display products.***

***Furthermore, understanding the analyzed root causes of such defects provides valuable insights into improving the fundamental advancement of OLEDoS design technology for future XR applications.***

## Author Keywords

Extended Reality (XR), Mixed Reality (MR), Augmented Reality (AR), Virtual Reality (VR), OLEDoS, Micro Display, 4K Driving

## 1. Introduction

Recently, the demand for extended reality (XR) has rapidly increased. The form-factor of devices related to XR has several difficulties in applying OLED panels used in conventional mobile devices.

First, since the panel is located close to the pupil, it has a size constraint of about 1 inch. However, the boundary between pixels is more recognizable because it is right in front of the pupil. Therefore, it requires integration technology over 4000ppi.

Second, the image transition must be linked to human sight, which means it must be over 90Hz display frequency. However, due to the spatial limitation, the source amplifier cannot be placed 1:1 with the data line of the pixels. In practice, back-plane (BP) circuits should be operated at least N times faster than the refresh rate.

Finally, due to the above characteristics, the application of silicon BP is inevitable. In other words, wafer business with foundry companies must be accompanied. However, this business system forces longer design cycles and poor revision agility.

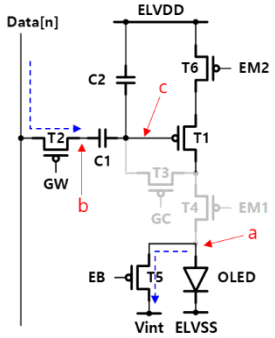
Therefore, it is critical to identify the mechanisms of unintended behavior in current designs logically. This will accurately categorize what can be solved by driving technology or what should be updated in the next design cycle.

## 2. Contents

This study analyzed the four major defects (Horizontal crosstalk, Current degradation, Step efficiency, and Temperature sensitivity). The knowledge and know-how will provide an optimal driving methodology to resolve the defects and lead to insights into fundamental product improvement.

### 2.1. Data Write with capacitance dividing method

OLEDoS requires fine current control, which means the Vgs of the driving transistor should be finely controlled, too. Since this fine control cannot be realized with the source DVO, a coupling capacitor was added between the data line and the gate of the driving transistor. Then, the difference between the pre-charge voltage of the data line and the data voltage is written to the gate of the driving transistor according to the circuit formula.




$$Vc = ELVDD + \frac{C1}{C1+C2} \times (Data[n] - Vpre) - |Vth|$$

**Figure 1.** Circuit formula of capacitor dividing data write

#### 2.1.1. Horizontal Crosstalk

The primary mechanism of strongly recognizable horizontal crosstalk is the pixel internal compensation operation within unstable ELVDD. Factors affecting ELVDD are data swing range, external stabilizing capacitance, and a factor affected is the Vth tracking process of the pixel driving transistor, so crosstalk can be avoided by controlling the above three methods. However, at the product level, fatal trade-offs exist in every method, so an optimal driving solution was applied based on strict understandable mechanism, controlling each factor adequately.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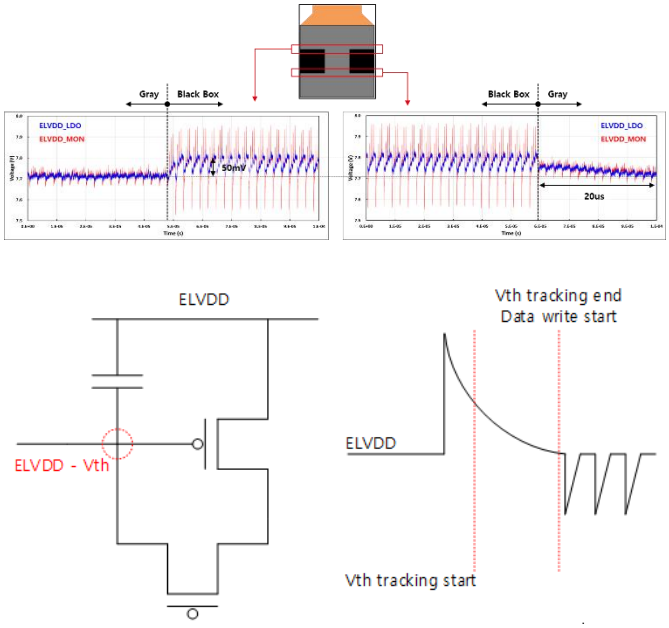


**Figure 2.** Conceptual drawing about ELVDD power fluctuation caused by data swing and T1 gate program error before the start of Vth tracking

Following is a simple zero-sum process explanation about optimal driving for horizontal crosstalk. At the beginning of pixel internal compensation, Vc will be programmed to be (ELVDD + error1 - Vth) with an error greater than Target. However, as ELVDD settles down significantly, causing coupling in the opposite direction of the original error, the final Vc will be (ELVDD + error1 - error2 - Vth). Calculating a Vth start point that satisfies (error1 = error2), we can eliminate the horizontal crosstalk.

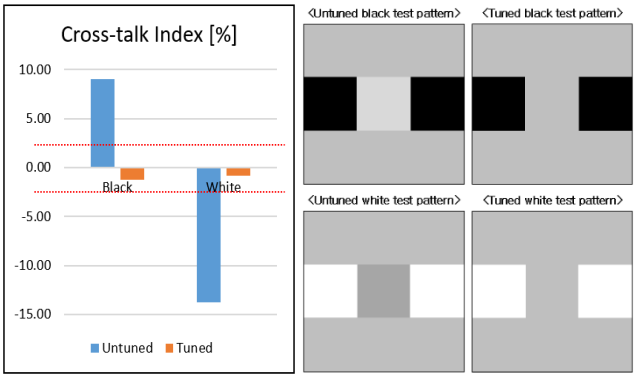


**Figure 3.** Comparison between before/after optimization (Spec. ±2%)

### 2.2. Small Storage Capacitance

The pixel area of a 1.3-inch 4K OLEDoS is calculated to be about 6um. The capacitor formed inside the pixel is determined by the shape and distance of the metal layer, and due to the physical limit, it is impossible to realize a large capacitance. The parasitic capacitance of mobile-sized pixels is negligible compared to the storage capacitance. However, in OLEDoS, it should be considered since the capacitance gap between storage and parasitic capacitance is under 10 times.

The above fact was found to be the cause of fast degradation, low step efficiency, and high temperature sensitivity. Therefore, the anode coupling model was newly applied to identify problems and propose improvements in this study.

#### 2.2.1. Anode Coupling Model

If the operation voltage of the OLED is Vop, Va changes from Vop to Vint at every initial state of the pixel, and the amount of voltage change affects T1 Vc voltage through the parasitic capacitance Cgd. When the Vop is moved to another voltage because of Vth shift of EL, or initial state error, or temperature or whatever, Vgs is changed together, resulting the current difference in driving transistor. We call it the anode coupling in this study.

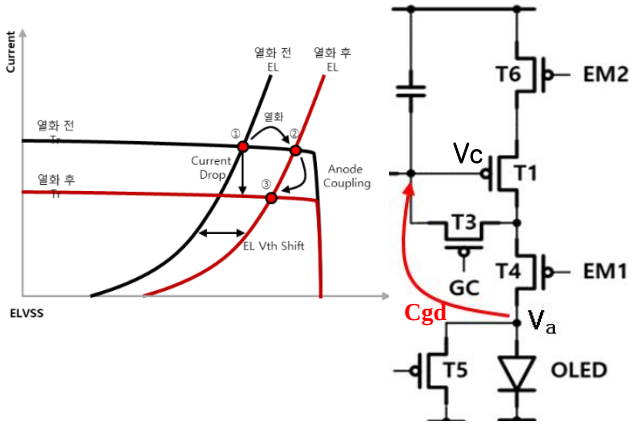


**Figure 4.** Anode coupling model of pixel

#### 2.2.2. Degradation

When the Vth of EL is shifted by degradation, the operation voltage of OLED is also moved. Then, the amount of change from Vop to Vint at the initial state of the pixel increases compared to before degradation. This causes Vc to change higher, which means that Vgs decrease. Therefore, even if the driving transistor is still within the saturation region, a current drop has occurred without any EL efficiency drop. Within this model, the design should firmly designate a maximum Vth shift range of EL specification to maintain life quality.

### 2.2.3. Step Efficiency

Due to the OLEDoS substrate structure, the initialization of the anode through pmos was forced. In other words, pmos was also used for pull-down operation, which means OLED operating point is involved in the T5 Vsource. Therefore, the degree of initialization of the anode can be various depending on the previous frame data. Then, the Vgs of T1 would also change based on the anode coupling model, resulting in poor step efficiency. With this mechanism, the initial voltage was tuned to enhance step efficiency.

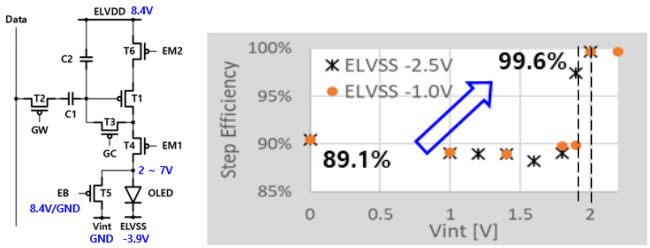


**Figure 5.** S/E enhancement by initial voltage optimization

### 2.2.4. Temperature Sensitivity

As the temperature increases, the efficiency of the OLED increases, lowering the OLED operating point and increasing the Vgs of T1 based on the anode coupling model, which increases the luminance.

Therefore, we proposed dynamic control of ELVSS that can efficiently respond to temperature changes while accomplishing contrast ratio. When the Vth of EL is positively shifted in a high-temperature situation, attaching ELVSS towards GND can minimize the data swing range between black and white. It was effective for ensuring luminance and contrast ratio stability, and improving power consumption by lowering the overall dynamic power.

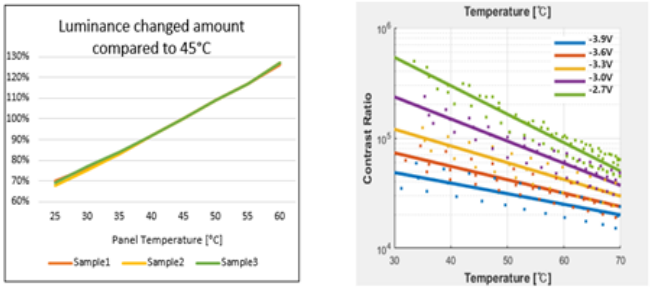


**Figure 6.** Luminance difference by temperature and contrast ratio by ELVSS voltage

## 3. Conclusion

This study analyzed the unexpected phenomenon in the OLEDoS and logically identified the mechanism. First, we accurately understood the horizontal cross-talk caused by the capacitor dividing data write method, applied optimal driving technology to minimize ELVDD coupling noise, and proposed a key target for the next design. In addition, we established an anode coupling model with the idea of the limitation of storage capacitance and verified its validity by simulation and experiment. Though the root cause cannot be eliminated due to space constraints, the sophisticated driving techniques can be applied with the logic of the anode coupling model. For example, extracting EL Vth shift quantity for current degradation specification, Vint control for step efficiency, and Dynamic ELVSS for temperature sensitivity.

The problems arising from the newly developed pixel circuit and driving scheme were clearly explained in a closed system without intervention of external factors, which will contribute as valuable intellectual know-how to the comprehension and future commercialization of our OLEDoS products.

## 4. References

[1] OLEDoS as a future display, http://www.thelec.kr/news/articleView.html?idxno=17905