# World's First OLED Display Using 12-inch IGZO-on-Si 3D Monolithic Integration

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## Abstract

***We prototyped a backplane with an IGZO-on-Si structure in a 12-inch wafer production line for the first time in the world. The monolithically formed Si FETs and OSFETs in the prototyped backplane exhibited good characteristics. Using the backplane, we successfully fabricated a 3527-ppi micro-OLED display for AR/VR application.***

## Author Keywords

CAAC-IGZO; OLED; OS/Si structure; IGZO-on-Si; 12-inch wafer

## 1. Background

Cross reality (XR) such as augmented reality (AR) or virtual reality (VR) has been attracting increasing attention in recent years. To enhance a sense of immersion, near-eye displays are required to have high definition, and there have been a number of reports on displays with 4000 to 5000 ppi. Display elements of near-eye displays can be liquid crystal, organic light-emitting diode (OLED), or micro-light-emitting diode (micro-LED) displays, but OLED and micro-LED are particularly preferable in terms of the response speed and contrast. Micro-LED, however, has a challenge in its mounting process, and reports on near-eye displays with OLED (also referred to as micro-OLED displays) are prevailing [1-4].

In this paper, Indium Gallium Zinc Oxide-on-Si (IGZO-on-Si) large-scale integrated circuits (LSI) fabricated by a 12-inch wafer process has been demonstrated for the first time. The IGZO oxide semiconductor field effect transistors (OSFETs) monolithically integrates with the Si transistors is reported. This integration enables the possibilities of introducing the powerful Si based digital, analog integrated circuits and embedded memories to IGZO display having both Si and IGZO advantages in a chip. Meanwhile, the feature size of the 12-inch wafer fabrication provide the high definition (>3500 ppi) choices of the backplane process. In contrast, a glass substrate is advantageous in that it allows a large screen to be fabricated at low costs, but has a difficulty in achieving definition higher than 2000 ppi due to photolithography limitations. Thus, the needs for high definition displays exceeding 3000 ppi would probably be mainly met by near-eye displays using Si wafers.

Transistors fabricated through Si wafer process, generally using single-crystal Si as the active layer, enjoy high mobility. However, in micro-OLED displays, current flowing through the OLED element in each pixel is small. Since the mobility of single-crystal Si transistors is too high, the channel length needs to be increased to achieve an optimal current value, which has been an obstacle in increasing the pixel density of displays with single-crystal Si pixel circuits. Meanwhile, oxide semiconductor field effect transistors that utilize oxide semiconductors as the active layer are able to provide current that is suitable for a micro-OLED display, with a small transistor size [5, 6]. In addition, transistors with high breakdown voltage are suitably used in AR devices, which are used under the outside light and require high luminance. Having high voltage tolerance, OSFETs are advantageous in achieving high luminance even with small transistor sizes.

Development of OSFETs have been conducted with a glass substrate process [7-10], but development and reports on OSFETs with Si-wafer-based LSI process are increasing. There are growing expectations for their application to low-power devices, taking advantage of the low off-state current (also referred to as Ioff) characteristics.

In the 12-inch wafer production line, we have developed a process for forming OSFETs over Si FETs. Figure 1 shows the 12-inch wafer used for our prototyping.

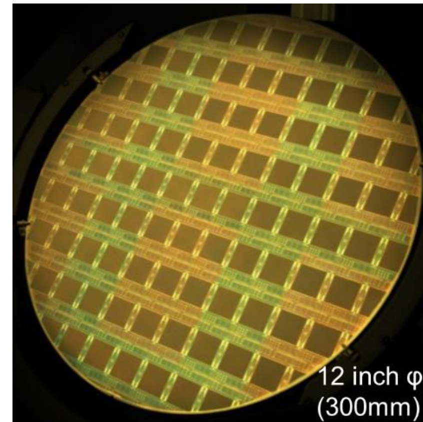


**Figure 1** Photograph of a 12-inch wafer the chip size is 24 mm x 32 mm

In this paper, we will report the characteristics of OSFETs that were fabricated in the 12-inch wafer production line and a micro-OLED display that was prototyped with use of the process.

## 2. Process overview

As described in References [5, 6], our configuration in which


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peripheral circuits including a source driver are formed of Si FETs, and OSFETs that constitute pixel circuits are stacked over the Si FETs, followed by OLED evaporation on top of the stack, enables narrow bezels and an increase in the number of chips that are obtained from each wafer.

We would also like to note that the definition, size, and pixel counts of displays vary depending on the product. In the case where the circuits are formed only of Si FETs, any change in such specifications would require the whole process to be modified, which would entail an increase in costs. In contrast, with IGZO-on-Si process, displays with desired specifications can be formed by changing only the OSFET part, unless the specifications do not exceed the capability of the peripheral circuits formed of Si FETs. In other words, using the common Si circuits, a variety of displays can be fabricated by only changing the OS process. This would make it possible to meet various needs more flexibly, as compared to a case where the display backplane is formed only of Si circuits.

The cross-sectional transmission electron microscopy (TEM) image of the display, which was fabricated based on the above concept, is shown in Fig. 2. Si FETs are first formed, followed by wiring process, and then OSFETs are formed. After that, wiring layers and a pixel electrode layer are formed. The OSFET includes *c*-axis-aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO) in the OS active layer. Improving the crystallinity can increase the stability of the OSFET characteristics.

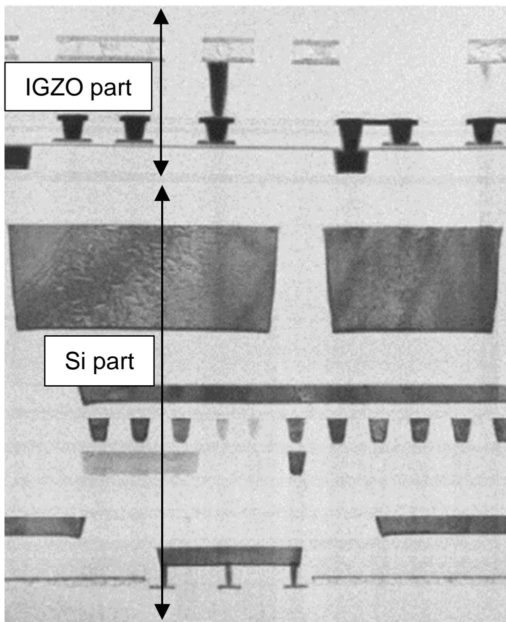


**Figure 2** Cross-sectional TEM image showing the monolithic IGZO-on-Si

## 3. Characteristics

Figure 3 shows the current-voltage (I-V) characteristics of the OSFET manufactured in the 12-inch wafer production line. With a size of $W/L$=130/200 nm, the OSFET exhibited normally-off characteristics.

The Id-Vg curves in Fig. 3 indicate that the Ioff is between 1E-13 to 1E-14 A, but this result would not the actual Ioff due to the measurement tool resolution. Thus, following the measurement procedure described in Reference [11], Ioff is extracted by the measurement on the Ioff test structure with twenty thousand OSFETs in parallel and the Ioff in $10^{-20}$ A/μm order of magnitude is proved on the 12-inch wafer.

Next, the characteristics of Si FETs are shown in Fig. 4. Since the FET characteristics changes between before and after OSFET process is within the transistor model coverage range, it can be said that the affinity between OSFET and Si FET is high.

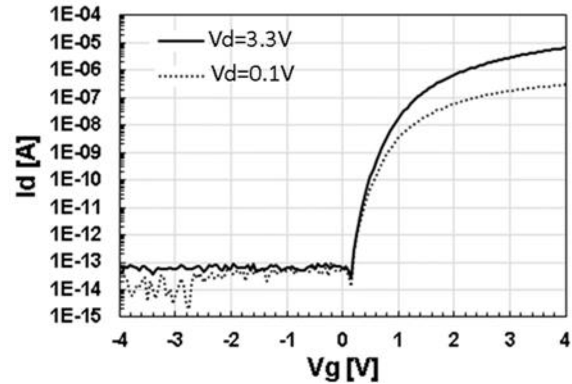


**Figure 3** Id-Vg characteristics of an OSFET

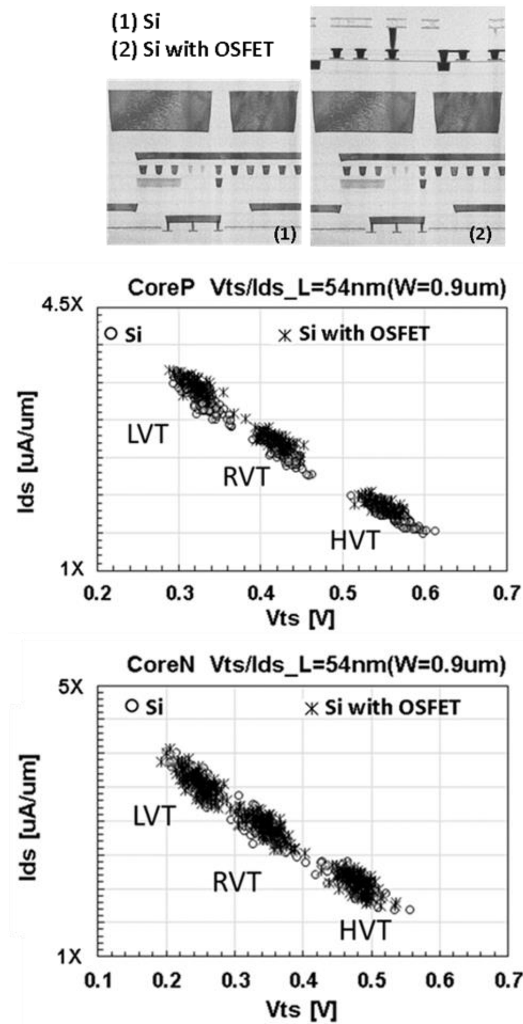


**Figure 4** Si low-Vt regular-Vt and high-Vt FET characteristics on the Si structure and the Si with OSFET structure

Voltage tolerance of the drain in the Si FET and OSFET is shown in Fig. 5. The voltage sweeps on the drain side and the other terminals ground. For Si MVN FET, the test element group with *W*/*L*=10000/1000 nm was used in measurement, and the leakage current increases as the Vd increases. For OSFET with a transistor size of *W*/*L*=130/200 nm, the drain exhibits ample tolerance without soft breakdown conduction before the hard breakdown.

Fig. 6 shows the negative bias temperature illumination stress (NBTIS) reliability test and the Vt shift is around 100 mV (125ºC 10 hours) on an OSFET with a size of W/L=130/200 nm.

The voltage tolerance and NBTIS reliability results indicate that our OSFET is sufficiently capable of driving the pixel circuit shown in Fig. 7 and is suitable for achieving displays with high pixel density. Furthermore, our device structure is compatible with different types of OLED formation methods, i.e., white OLED (WOLED) type and RGB side-by-side type, and is suitable for AR/VR displays that are required to have high luminance.

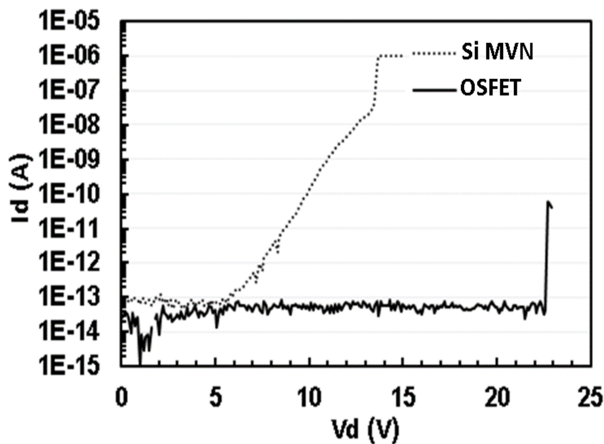


**Figure 5** Voltage tolerance of the drain of Si FET and OSFET

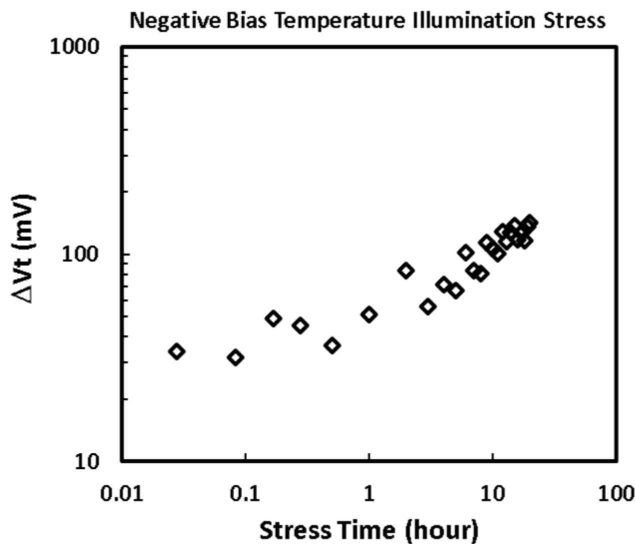


**Figure 6** Negative bias temperature illumination stress reliability

## 4. Pixel Circuit

Figure 7 shows the pixel circuit of the prototyped micro OLED display [12]. The pixel circuit is composed of all OSFETs, and the threshold voltage of the driving transistor (M2) is corrected by back gate bias.

The potential of the anode of an OLED device (NA) changes depending on the display luminance. To control the transistor M5 even when the luminance is high and NA is high, the amplitude of voltage to control the gate should be large. In other words, high voltage tolerance is required for the gate of M5. In addition, drain-source voltage (Vds) of a driving transistor changes greatly in accordance with the OLED device characteristics and the required luminance. Thus, drain-source voltage tolerance matters.

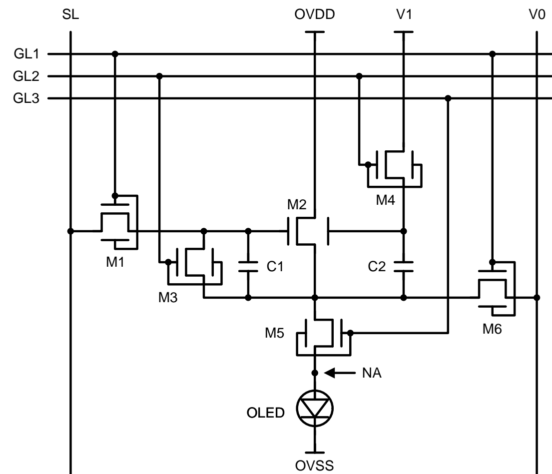


**Figure 7** Pixel circuit diagram

## 5. Panel Specification

The specifications of the display we prototyped are listed in Table 1. With OLED/OS/Si structure, the source driver, scan driver, and input/output circuits are composed of Si FETs whereas the pixel circuits are composed only of OSFETs.

Si FETs were fabricated using 55-nm technology process. For displays formed through glass-substrate-based process, the pixel circuit is fabricated using 180-nm technology process, for example, because of the large pixel size (i.e., the large pixel pitch). However, for micro-OLED displays, a more advanced process node is necessary because the pixel pitch is narrower with the pixel density increasing to around 3000 ppi or higher. In addition, the size of a transistor itself needs to be reduced in order to achieve a high frame rate such as 90Hz, which is required for VR application, with pixel counts of 2560 × 2560. Thus, we used 55-nm process to fabricate our display driver circuits.

For display coloring we used metal mask less (MML) technology in which OLED device patterning is performed by photolithography without using a metal mask [13]. The display image is shown in Fig. 8.

As can be seen in Fig. 8, normal display is observed. The luminance of the prototyped display is 5000 cd/m$^2$; by taking advantage of OSFET's voltage tolerance characteristics mentioned above, higher luminance can also be achieved.

**Table 1.** Panel specifications

| | Specifications |
|---|---|
| Screen diagonal | 1.03 inches |
| Resolution | 2560 × 2560 |
| Pixel size | 7.2 μm × 7.2 μm |
| Pixel density | 3527 ppi |
| Aperture ratio | 52.9% |
| Frame rate | 90 Hz |
| Coloring method | MML |
| Emission type | Top emission |
| Source driver | Integrated (Si-CMOS) |
| Scan driver | Integrated (Si-CMOS) |

**Figure 8** Display image

## 6. Conclusion

We have succeeded in developing a process of stacking Si FETs and OSFETs on 12-inch Si wafers. We fabricated an OLED display by evaporating OLED on the stack, and the display exhibited normal operation.

We prototyped a display with a 3527 ppi, but there are needs for 5000-ppi or higher-ppi displays in the AR/VR market. A 5000-ppi display would require a pixel size of approx. 5 μm × 5 μm, as well as high luminance; thus, the transistors used inside the display need to be small in size and tolerate high voltage. OSFETs can meet these needs. In addition, application of OSFETs is not limited to the display market but there are also needs from the memory market. Having established the production line to manufacture OSFETs on 12-inch Si wafer, we will be able to meet these needs.

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