Submicron c-IGO TFT Exhibiting High Performance and Excellent Stability for Ultra-High-Resolution Display

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Abstract

We report a high-quality, stack poly-crystalline InGaO (c-IGO) thin-film transistor (TFT) for AMOLED display backplanes. The active layer with high Ga was sequentially deposited on low Ga IGO layer by spray pyrolysis. The TFTs with a high-Ga top layer demonstrated superior stability for the TFT with 0.74 µm channel length, exhibiting the field effect mobility of 9.18 cm^2/V·s and V_{TH} of 0 V with a high on/off ratio of > 10^8.

Author Keywords

Low-cost display manufacturing; spray pyrolysis; short channel TFT; solution process

1. Introduction

The continuous demand for high-performance and cost-effective display technologies has driven significant advancements in thin-film transistor (TFT) materials and fabrication methods (1-4). Among these, indium gallium zinc oxide (IGZO) is very popular due to its outstanding properties such as low leakage current, superior bias-temperature stability, and excellent uniformity (5). To meet the requirements of next-generation display technologies, such as augmented reality/virtual reality (AR/VR) displays, thin-film transistors (TFTs) with high mobility and stability are essential for manufacturing high-resolution active-matrix organic light-emitting diode (AMOLED) and micro-LED displays (6).

Crystalline indium-based oxide semiconductors are gaining increasing attention for next-generation TFTs due to their high performance. However, indium oxide requires stabilizers like Ga, La, or Al because of its unstable nature, and the use of these stabilizers increases the crystallization temperature (7-8). These methods often involve additional crystallization steps at high temperatures, making them less cost-effective than amorphous MOS and preventing the use of flexible substrates (9, 10). In contrast, the spray pyrolysis deposition technique allows crystalline MOS growth in air, enabling cost-effective, large-area TFT backplane production (11).

In this work, we propose a self-aligned, top-gate TFT by sequentially depositing IGO with different metal cation compositions. IGO with low In composition in IGO (low-In IGO) is deposited on high-In composition IGO (High-In IGO) layer. This can modulate the electronic properties of the TFT. This approach aims to optimize key performance metrics, such as field-effect mobility (μ_{FE}), threshold voltage (V_{TH}), and subthreshold swing (SS), while maintaining excellent stability under bias stress. We demonstrate that the c-IGO stack TFTs, particularly those with a high Ga content in the top layer, offer promising performance for short-channel TFT. This concept can be applied to design the MOS materials for the TFT active layer.

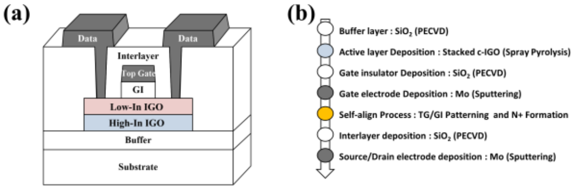

Figure 1. (a) Cross-sectional schematics of fabricated, stack TFTs by spray pyrolysis process. (b) Fabrication process steps of stack c-IGO TFTs with self-aligned, coplanar structure by spray pyrolysis.

2. Experimental

The IGO precursor solution was prepared by dissolving indium chloride ($InCl_3$, 99.999%) and gallium nitrate hydrate ($Ga(NO_3)_3 \cdot xH_2O$, 99.9%) in anhydrous 2-methoxyethanol ($CH_3OCH_2CH_2OH$, 99.8%) with a 0.1 M. Ammonium acetate ($CH_3CO_2NH_4$, ≥99.99%) was used as a stabilizer to improve solubility and enhance the film quality by facilitating bubble-free and uniform films (19). For the IGO solution, the ratios of In and Ga precursors were varied to control the compositions of In and Ga in the thin films. The total metal cation concentration was maintained at 0.1 M. All precursors were purchased from Sigma Aldrich and synthesized without modification. The precursor solutions were stirred at room temperature for 24 h to obtain homogeneous and transparent solutions.

The fabrication process for the stack c-IGO TFTs is summarized in Fig. 1. The fabrication was performed on 6-inch glass substrate (15 × 15 cm^2). First, a 100 nm SiO_2 layer was deposited as a buffer layer using plasma-enhanced chemical vapor deposition (PECVD). Then, c-IGO layer was grown by spray pyrolysis at a substrate temperature of 390 °C. The distance between the spray nozzle and the substrate was maintained to be about 11.5 cm. The total time for each cycle of the spray deposition step was 60 s. The process was repeated to get the desired thickness of semiconductor film, and the IGO film was deposited over three cycles. The IGO film was deposited over three cycles. For the stack thin film, one cycle of high-In IGO was initially deposited, followed by two cycles of low-In IGO. Then, a 100 nm SiO_2 layer

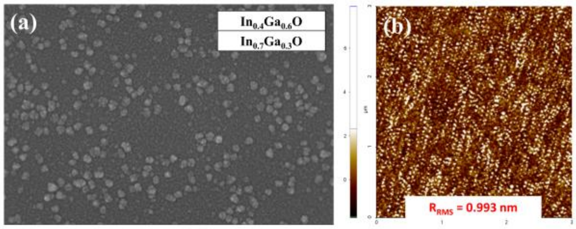

Figure 2. (a) Top-view SEM images of low-In IGO / high-In IGO film by spray pyrolysis on glass substrate. Atomic force microscope images of the polycrystalline (b) low-In IGO / high-In IGO thin films deposited by spray pyrolysis.

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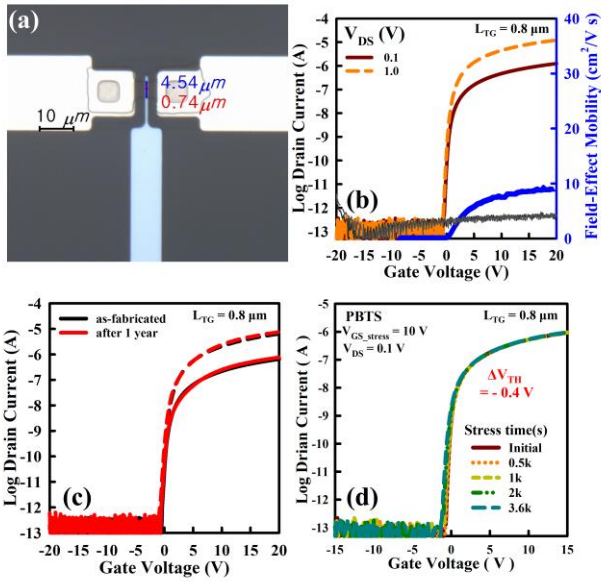

Figure 3. Device performances of the short channel TFTs. (a) Optical image and 0.74 μm length IGO TFT. (b) The transfer curves of the TFTs with 4 μm channel width and 0.74 μm channel length fabricated with low-In IGO / high-In IGO. (c) 1-year environment stability result and (d) PBTS for 0.74 μm channel length TFTs with V_{GS_stress} = +10 V at 60 ℃ for 1 h.

and a 150 nm molybdenum (Mo) layer were deposited as gate insulator (GI) and gate electrode, respectively, by PECVD and sputtering. The gate metal and GI were patterned, and the N+ region was formed by NF_3 plasma treatment in the contact area. Then, 300 nm SiO_2 and 200 nm Mo layers were deposited as interlayer and source/drain electrodes, respectively. The fabricated TFTs were annealed in a vacuum furnace at 250 °C for 2 h.

All electrical characteristics were measured by Agilent 4156C, semiconductor parameter analyzer. The V_{TH} was determined as the V_{GS} corresponding to the constant IDS of W/L × 10 pA at the V_{DS} of 0.1 V. The μ_{FE} was calculated from transconductance; $\mu_{FE} = (L \cdot g_{m\_max})/(W \cdot C_{OX} \cdot V_{DS})$. The SS was calculated as $(d\log(I_{DS})/dV_{GS})^{-1}$ over the range of 10 pA ≤ I_{DS} ≤ 100 pA, with V_{DS} = 0.1 V.

Active Material	Method	L (μm)	V_{TH} (V)	μ_{FE} ($cm^2/V \cdot s$)	Year (ref)
a-IGZO	Sputtering	3	0.4	-	2019 (12)
a-IGZO	Sputtering	2	1.0	2.4	2020 (13)
a-IGZO	Sputtering	1.5	0	-	2021 (14)
a-IGZO	Sputtering	0.87	-2.16	6.44	2022 (15)
a-IGZO	Spray Pyrolysis	1.69	-0.8	40.95 (μ_{sat})	2023 (16)
a-IGZO	Sputtering	1.3	0.03	9.77	2024 (17)
c-IGO	**Spray Pyrolysis**	**0.74**	**0**	**9.18**	**This Work**

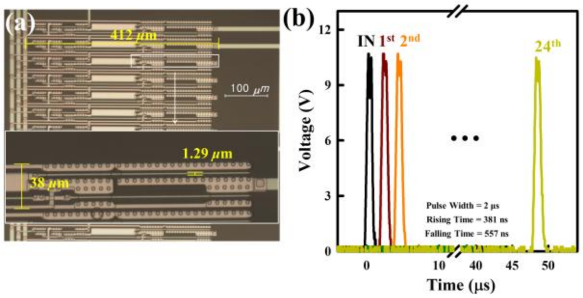

Figure 4. 8T1C scan driver circuit fabricated with stack IGO TFTs. (a) The optical micrograph of the 8T1C scan driver. (b) The output of the 24-stage scan driver circuit with the pulse width of 2μs.

3. Result and Discussion

Fig. 1(a) shows the schematic representation of the a-IGZO The microstructural characteristics of the stack c-IGO films by spray pyrolysis, were investigated by using a Scanning Electron Microscope (SEM) and atomic force microscope (AFM). SEM images of spray pyrolyzed low-In IGO on the high-In IGO layers are shown in Fig. 2(a). Even the high Ga content, the film has a polycrystalline phase. AFM images are shown in Fig. 2 (b), indicating that the stack IGO film exhibits excellent surface roughness.

We fabricated TFTs with short channel lengths TFTs and analyzed their electrical characteristics. The TFT channel width and length are 4 and 0.74 μm, respectively. Fig. 3(a) illustrates the top-view, optical image of stack TFT with 0.74 μm channel length. The low-In IGO/high-In IGO TFT with 0.74 μm length exhibits V_{TH} of -0 V, and μ_{FE} of 9.18 cm²/Vs as shown in Fig. 3(b). The comparison of the short channel coplanar oxide TFTs from the literatures is shown in Table 1. The stability test was carried out on short-channel TFTs. The TFT performance remains unchanged without any degradation even after one year in an atmospheric environment. Fig. 3(d) illustrates the results of a positive bias temperature stress (PBTS) test performed on the 0.74 μm TFT under the gate stress (V_{GS}) of +10 V at a temperature of 60 ℃. Excellent stability was observed, with a very small ΔV_{TH} of -0.4 V.

To demonstrate the stack TFT integrated circuits by using the IGO, a scan gate driver circuit was fabricated. The scan gate driver circuit was designed with the channel length of 1.3 μm. The operation of the gate driver can be found in our previous article (18). The pulse width of the starting and clock signals was set to 2 μs, corresponding to 4k (3840 × 2160) and 240 Hz display panel. The starting and CLK signals swing from 0 V to 10 V. The low voltage is set to 0 V. The fabricated scan driver circuit operates fully to the last stage of the 24th, with an output voltage swing of 10 V. The output signal of the last stage exhibits a rising time of 381 ns and a falling time of 557 ns.

4. Conclusions

This study demonstrated a self-aligned top-gate TFT manufacturing using spray-pyrolysis using a crystalline indium gallium oxide (c-IGO) semiconductor layer. By sequential deposition of different In:Ga ratio, the stack TFT with submicron channel length exhibited high performance, excellent bias stability and negligible hysteresis. The 0.74 µm channel stack TFT exhibited the V_{TH} of 0 V and field effect mobility over 9 cm^2/Vs. The gate driver circuits made of 1.3 um TFTs are well operated until the last stage. These results demonstrate that the stack c-IGO TFTs offer promising potential for short channel TFTs for high resolution AMOLED and micro-LED displays.

5. Acknowledgments

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