

# Layout Engineering for Oxide Mura Mitigation in AMOLED Displays: A Data-Driven Causal Analysis

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## Abstract

*The development of AMOLED products utilizing the oxide semiconductor HOP has faced challenges due to the occurrence of oxide mura, a reliability issue marked by display non-uniformity. Although changes in oxide properties are hypothesized to result from hydrogen diffusion in the ILD(interlayer dielectric) layer, the exact causes behind the inconsistent occurrence of oxide mura across products with identical process conditions remain an open question. This study investigates the potential causes of oxide mura by analyzing layout changes due to the implementation of BRS (Border Reduction Structure) technology, which was identified as a likely contributing factor. Given the complex correlations and hierarchical relationships among candidate causes, we utilized Graphical Causal Modeling (GCM) to infer causality, providing a robust analysis of distribution changes under varying influences, such as PA process conditions, pixel design layout, product specifications, and operating driving conditions. Our findings enable the prediction of oxide mura risk in new products, identifying critical parameters for modification and offering insights into the simultaneous effects of layout and process conditions. This approach enhances our understanding of the factors influencing oxide semiconductors, facilitating improved product reliability and quality in future AMOLED developments.*

## Author Keywords

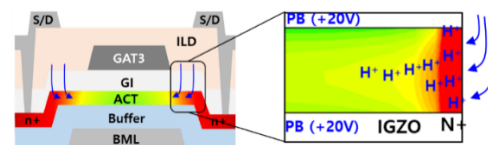
Pixel Circuit design, Graphical causal model-based inference, Oxide Mura

## 1. Introduction

AMOLED's HOP (hybrid of Oxide semiconductor and Polysilicon TFT) technology was developed to meet market demands for low power consumption. [1] Also, the IGZO oxide process was developed alongside new driving technology to support the low driving frequency operation. During the reliability evaluation of IGZO transistors under high-temperature and drive state conditions, a smearing issue was observed due to changes in the threshold voltage ( $V_{th}$ ). This problem is attributed to a combination of mechanisms: the introduction of oxygen (an acceptor) during the PBTS test and the infiltration of hydrogen (as a donor) in the ILD layer. At elevated temperatures, particularly above 70 degrees Celsius, excess hydrogen diffuses into the channel, leading to a shift in the parasitic channel characteristics, as illustrated in Figure 1. [2]

Despite the explanations for changes in the characteristics of IGZO semiconductors, these explanations were insufficient to account for the variations observed in actual products. In other words, even when the same process conditions and PA(Process

Architecture) structure were applied, the reliability varied. A simple trend analysis indicates that BRS technology is more disadvantageous compared to non-BRS, and QHD resolution is more problematic than FHD, suggesting that resolution may also contribute to these reliability issues. However, the exact causes have not been fully analyzed. In this paper, we examine the factors contributing to these reliability differences and discuss strategies to prevent them.



**Fig. 1** Explanation of  $V_{th}$  migration due to diffusion of intrusive hydrogen from the ILD layer

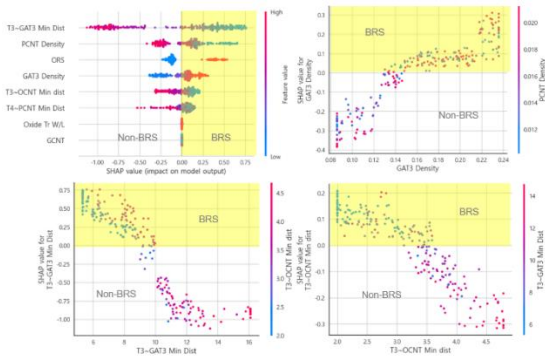
## 2. SHAP based analysis

In this analysis, we collected reliability evaluation results from 28 products with HOP, gathering data on pixel layout information, process conditions, driving methods, voltage conditions, and other relevant factors. A total of 94 parameters were collected for each product as potential candidate parameters.

### - BRS Design impact analysis to layout

BRS is an innovative technology aimed at reducing dead space by minimizing the number of spiders that transmit data at the base of the existing network. This technology offers several advantages, such as reducing heat generation by situating the area within the active region and simultaneously integrating ELVSS wiring. Despite these benefits, the relationship between BRS and Oxide Mura has been a subject of ongoing investigation due to a noticeable increase in Oxide Mura following the implementation of BRS, although a definitive analysis has not yet been conducted.

To address this issue, we utilized SHAP (SHapley Additive exPlanations) to analyze the impact of design layout changes induced by BRS (see Fig. 2). [3][4] Our findings indicate the parameter with the largest influence was the T3-GAT3 minimum distance, followed by PCNT density, ORS, GAT3 density, T3-OCNT minimum distance, and several other factors anticipated to influence oxide transistors. However, at that time, the analysis of causality remained unclear, which nonetheless assisted in identifying potential candidate parameters for further investigation.

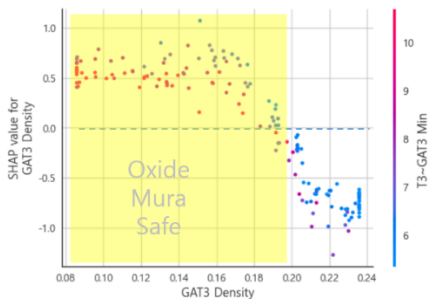


**Fig. 2** Impact analysis using SHAP to evaluate the effect of BRS wiring on the pixel circuit layout. The results show that BRS wiring increases the GAT3 pattern density, reduces the distance of T3-GAT3, and decreases the distance between T3 and OCNTs.

**- Single-variable design rule consideration**

Before conducting a thorough causal analysis, we explored the possibility of deriving a single-variable design rule to prevent oxide mura based solely on correlational data. Single-variable design rules are prevalent in semiconductor design due to their simplicity, ease of application to design rule checks (DRC), and automatic verification capabilities. However, given the complex interactions among various variables, we found that only GAT3 density could be isolated as a potential single-variable rule. (Fig.3)

GAT3 density is recognized as a factor influencing H+ inhalation. Our study determined that GAT3 density should be maintained within approximately 22%, accounting for a 10% margin. Despite this finding, the single-variable rule for GAT3 density proved insufficient for accurately predicting oxide mura.



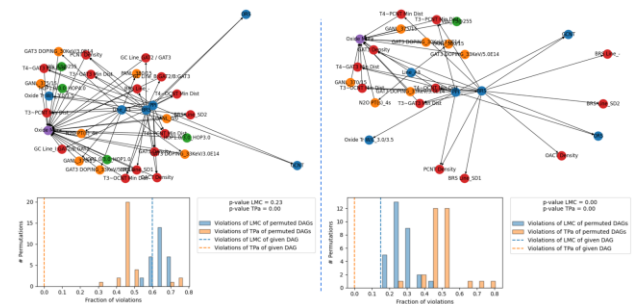
**Fig. 3** We developed a machine learning model to predict oxide mura based on the collected dataset. Our objective was to identify a single variable that could reliably prevent oxide mura, allowing us to establish a definitive design rule. However, the analysis indicated that configuring a single parameter for this purpose was challenging, with the exception of GAT3 density, which emerged as the only variable demonstrating a significant predictive capability.

**3. Graphical causal model-based inference**

While previous analysis methods employing machine learning

and SHAP have gained popularity due to their utility, they possess inherent limitations rooted in their foundational assumption that parameters are independent, lacking any correlations or causal relationships. [5] In analyses such as the one presented here, where BRS is applied to a multitude of design layouts exhibiting hierarchical causal relationships among parameters that influence oxide mura, the accuracy of SHAP computations is compromised. As a result, it is advisable to exclude causal relationships when employing SHAP. In light of these considerations, this study employed a Graphical Causal Model (GCM), constructed using SHAP information as a foundational reference. [6][7]

Traditional methods for inferring causal relationships from observational data are often hindered by strong assumptions and the lack of a clear baseline for evaluating the accuracy of proposed graphs. To address this challenge, we utilized a surrogate baseline approach that involves generating random permutations of nodes within the graph. By comparing the inconsistencies of our proposed causal graph against these surrogate graphs, providing an interpretable metric to assess the model's fit relative to random configurations. This method provides a practical metric of the graph's validity, demonstrates that our proposed causal structure for oxide mura provides a more accurate representation than random alternatives. This technique provides a robust framework for validating our model, supporting our hypothesis about the causal mechanisms underlying oxide mura and enhancing confidence in the model's applicability for predictive and corrective interventions in the manufacturing process. [8] The results of the DAG evaluation are presented in Figure 5. Initially, the constructed DAG showed a rise in the LMC p-value to 0.23, indicating discrepancies between the data and the DAG (left of Figure 4). However, after correcting the errors, the LMC p-value was reduced to 0.00, leading us to select this DAG for further analysis (right of Figure 4).



**Fig. 4** The results of the DAG evaluation. The constructed DAG showed a rise in the LMC p-value to 0.23, indicating discrepancies between the data and the DAG (left of Fig). After correcting the errors, the LMC p-value was reduced to 0.00, leading us to select this DAG for further analysis (right of Fig).

A formal approach based on graphical causal models seeks to identify the root causes of changes in a variable's probability distribution. [9] The ability to quantify the contribution of each variable allows developers to focus on the most relevant variables and make real improvements. Here's a sequential breakdown of the methods used.

1) Factorization of Joint Distribution: This method used factorizing the joint distribution of variables into conditional distributions of each variable, given its parents (the "causal mechanisms"). This is represented as:

$$PX_1, \dots, X_n = \prod_{j=1}^n PX_j|PA_j$$

Where  $PX_j|PA_j$  denotes the causal mechanism of variable  $X_j$  given its direct parents  $PA_j$  in the causal graph.

2) Definition of Probabilistic Causal Model: A probabilistic causal model is defined as a pair  $C := \langle G, PX \rangle$  consisting of a causal graph  $G$ , and a joint distribution  $PX$  over the variables in  $G$  that is compatible with  $G$ .

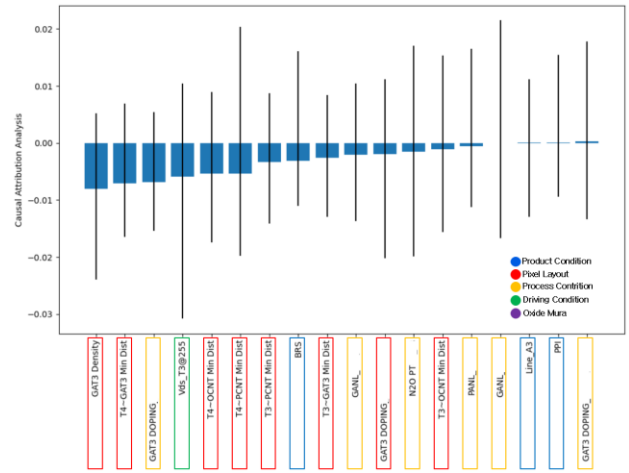
3) Mechanism Changes: this method defines mechanism changes in a causal model  $C := \langle G, PX \rangle$  as transformations that result in a new joint distribution  $PT_X$  by replacing old causal mechanisms  $PX_j|PA_j$  with new ones for a subset of  $PX_j|PA_j$  variables.

4) Kullback-Leibler (KL) Divergence: To quantify the change in the joint distribution, this method uses the KL divergence, defined for discrete random variables as:

$$D(P||Q) := \sum_{x \in X} P(x) \log \left( \frac{P(x)}{Q(x)} \right)$$

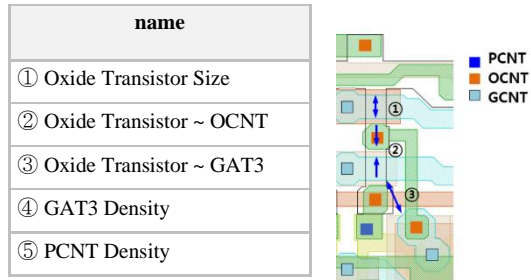
5) Contribution to KL Divergence: The contribution of each node  $X_j$  to the KL divergence from the joint distribution  $PX$  to  $\tilde{P}\tilde{X}$  is the KL divergence from its causal mechanism  $PX_j|PA_j$  to  $\tilde{P}\tilde{X}_j|PA_j$ .

By applying this DAG along with a method for inferring the causes of distribution changes, we were able to analyze the impact of various factors, such as process, design parameters, layout, and operating conditions, on the occurrence of oxide mura (Figure 5). In terms of layout, the GAT3 density had the most significant influence, followed by the T4-GAT3 minimum distance. The distances T4-OCNT and T4-PCNT were also identified as important factors, with the BRS application following. While PA processes such as GAT3 doping, GANL conditions, and N2O PT application are already well-known variables, this influence diagram provided insights into the order of influence from the perspective of the final product.



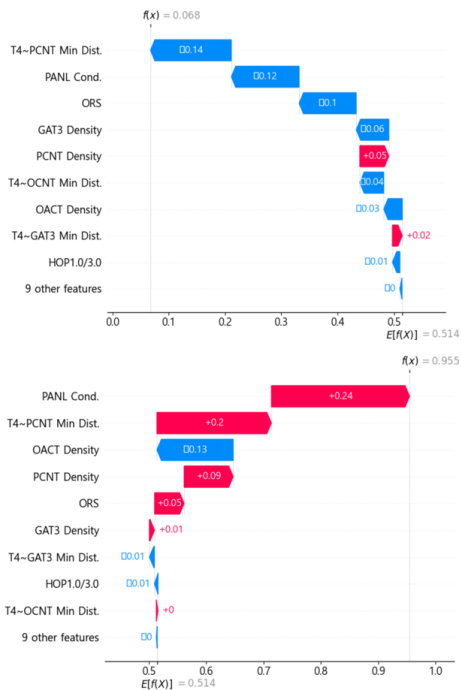
**Fig. 5** Causal attribution analysis of Oxide mura parameters by GCM. The parameter in red was analyzed as the cause related to Layout and oxide mura. Even after accounting for all other influences, it is analyzed that the difference in hydrogen density due to layout is responsible for the difference in oxide mura between products.

Through this analysis, the important factors from the layout perspective can be shown in the table below and Fig.6. It can be concluded that these factors simultaneously affect the hydrogen distribution of the ILD membrane in or around the oxide transistor, which in turn affects the oxide mura.



**Fig. 6** The simplified layout impact also shows five factors.

Ultimately, the analysis and modeling did not yield a simple design rule for predicting oxide mura in new products. However, it enabled us to predict the risk by using parameters identified through various causal inferences. Additionally, by explaining why certain parameters had a significant impact on risk or safety, we were able to determine what adjustments should be made during development (Figure 7).



**Fig. 7** In the case of the upper model, when predicting using the AI developed this time, the probability of reliability success was predicted to be low at 0.068, indicating the reason why it was judged to be so. Below is the bottom model, which endured reliability test, and the casual AI predicted the success probability well with 0.955 and showed the reason.

#### 4. Conclusion

Over the past year, we have faced challenges related to the unreliability of oxide mura in the development of AMOLED products using an oxide semiconductor known as HOP. While we proposed that changes in oxide properties could be attributed to hydrogen diffusion within the ILD layer, the precise reasons for the variance in occurrence between different products, despite identical process conditions, remained unclear. In this study, we focused on analyzing layout changes brought about by the application of a technology called BRS which was hypothesized to be a likely cause of oxide mura. By leveraging data-driven approaches, we aimed to infer the actual causes of oxide mura. Given the complex interdependencies and hierarchical relationships among candidate causes, a simple SHAP analysis was insufficient. Instead, we used Graphical Causal Modeling (GCM) to analyze changes in the distribution of oxide mura results. This allowed us accurately to infer causal relationships under various influences, including process conditions, design layout, product specifications, and operating conditions.

Through this causal analysis, we were able to predict the risk of oxide mura in new products, assessing the level of risk and

identifying which parameters need modification to mitigate this risk. This approach enabled us to pinpoint actual product risks and make informed decisions about necessary design and process adjustments. By identifying the simultaneous effects of layout and process, our analysis highlighted factors that were previously undetectable in simple TEG evaluations. This is significant because the characteristics of oxide semiconductors are influenced by a variety of factors. This research establishes a comprehensive framework for analyzing and predicting the risks associated with oxide mura, thus improving the reliability and quality of future AMOLED products.

While this analysis provides valuable insights into the relationship between layout parameters and oxide mura, it's crucial to recognize that these findings are specific to the particular process conditions used in this study. Further research is needed to validate these findings across a wider range of process parameters and manufacturing environments.

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