Improving the Reliability of High-Mobility Oxide TFTs through TCAD Simulation of Optimizing Device Structure

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Abstract
High-mobility oxide TFTs have great application prospects in high-end display products. To achieve mass production applications, improving the reliability of high-mobility oxide backplanes has become an urgent issue to be resolved. During the development of IGZTO oxide devices, we found that the TFT device is turned on, as Vds voltage increases, drain current will suddenly drop sharply at a certain critical point. In response to this issue, we analyzed the degradation mechanism: the hot-carrier effect under large electric field in the pinch-off region leads to defects increase of channel at the drain end, causing device degradation. TCAD simulation reproduced the IV degradation phenomenon, confirming the defects increase of channel at the drain end. The simulation of device size's impact on the channel electric field showed that increasing channel length and reducing drain voltage can effectively reduce the maximum electric field, while device width has no effect. Additionally, the simulation compared electric field distribution of different TFT structures, and the results indicated: horizontal electric field TG LS-Gate ≈ LS-Source > TG without-LS > TG Double-Gate, which provides a reference direction for achieving high-reliability high-mobility oxide backplanes and improving drain current down phenomenon .In this simulation work, we have developed a new AI-TCAD combined high-efficiency intelligent tuning model, significantly improving efficiency.

Author Keywords
Amorphous oxide; thin-film transistor; high mobility; TCAD；reliability; drain current down.

1. Introduction
In recent years, thin-film transistors (TFTs) based on amorphous indium gallium zinc oxide (a-IGZO) have become the standard backplane electronic devices for advanced liquid crystal and organic light-emitting display devices, due to their high mobility (about 10 cm^2/Vs), good uniformity, low processing temperature, optical transparency, and low process manufacturing costs [1,2]. As consumer demands for display devices increase, ultra-high-definition (UHD) displays, low power consumption, high refresh rates, and interactive functions are becoming more popular, leading to a growing demand for high-performance thin-film transistors (TFTs) [3,4]. High-mobility oxide TFTs, due to their high mobility characteristics, can provide greater driving current and faster response speeds, meeting the requirements for higher resolution and frame frequency. In this regard, indium gallium zinc tin oxide (IGZTO), as a special compositional system derived from SnO2, has a high carrier mobility rate (>30 cm^2/Vs) due to the enhanced infiltration path formation and effective mass densification from the loading of Sn into the IGZO matrix, and its improved chemical selectivity and resistance to wet etching using PAN can enhance its production capacity and quality[5]. Although the feasibility of high-mobility and reasonably stable IGZTO TFTs has been reported[6,7], there are few reports on the degradation measures related to the drain current drop phenomenon caused by the hot-carrier effect in circuit application.

In this paper, we analyzed the mechanism of device degradation and reproduced the phenomenon of device degradation before and after the drain current drop through TCAD device simulation. Based on the impact of the horizontal electric field in the device channel, we optimized the device size and structure through simulation to improve the drain current drop phenomenon caused by the hot-carrier effect, providing design references for improving device reliability.

2. Experiment details

2.1 Fabrication of the Experimental Devices
The TFT device structure prepared in this paper is shown in Figure 1, and its fabrication process is described as follows. First, a metal film is sputtered and patterned on a glass substrate to form a light-shielding layer (LS). Silicon nitride (SiN) and silicon dioxide (SiO) buffer layers are deposited using plasma-enhanced chemical vapor deposition (PECVD), followed by an annealing process. Then, an indium gallium zinc oxide (IGZTO) semiconductor channel layer is sputtered and patterned. Subsequently, a gate insulator (GI) layer is deposited using PECVD and annealed, followed by the deposition of a metal layer, which is patterned to form the top gate electrode. An interlayer dielectric (ILD) layer is deposited using PECVD and patterned to open vias. After sputtering and patterning to form the source/drain electrodes, a passivation layer is deposited for protection, and an organic planarization layer is applied. The TFT three-terminal pad area is etched out.

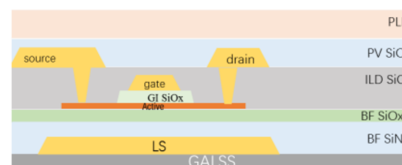

Figure 1. TFT device structure

2.2 Device measurement and analysis
In order to solve the issue of IGZTO TFT device，all electrical measurements were monitored by a Keithley 4200 source meter. The transfer characteristic curves were plotted measuring drain current (IDS) by sweeping gate voltage (VGS) from -10 V to 20 V with a drain voltage (VDS) of 10 V. The threshold voltage (Vth) was calculated by extracting VGS when IDS reached 1 nA under the condition of VDS = 10 V. The output characteristic curves were plotted measuring IDS by sweeping VDS from 0 V to 50 V with VGS = Vth+5V. The drain voltage fail point (VFP)was defined as the critical VDS corresponding a drain current down (DCD) phenomenon. Some measures were implemented to solve the issue of DCD. To verify hypothesized DCD mechanism based on experimental results, we performed the Technology Computer-Aided Design (TCAD) simulations that confirm the electrical field distributions in channels and reproduce the transfer characteristics.

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3. Property analysis of IGZTO-TFTs

Figure 2(a) shows the DCD phenomenon under the drain voltage sweep from 0 V to 50 V at VGS = 5V, when the gate slightly open, the IDS drops rapidly as the VDS exceeds the crit voltage (25.5V). The IDS could not reach the previous level after the DCD phenomenon. The transfer characteristics curves before and after the DCD phenomenon are shown in Figure 2(b).

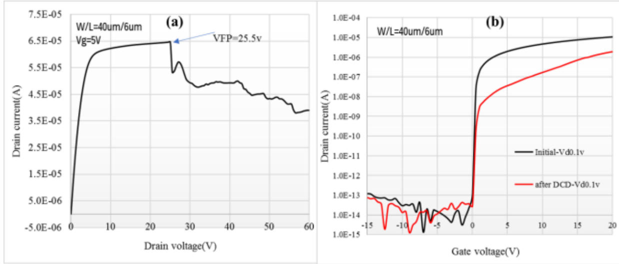

Figure 2. (a) The DCD phenomenon. (b) Transfer characteristics before and after the DCD

Through TCAD simulations, we obtained the internal electric potential distribution and the electric field distribution in the channel of the device at the critical state of the DCD phenomenon, as Figure 3(a)and 3(b) shows. When the drain voltage is higher than the gate voltage, the conductive front channel on the drain side is pinched off, thereby forming a high resistance region. Under the action of a strong electric field, an electron is accelerated to have a sufficiently high energy. And in the interaction with the crystal lattice, another electron transitions from the valence band to the conduction band, thereby generating a new electron-hole pair[8]. On one hand, electron and hole trapping centers are formed on the drain and source sides, respectively. Since the rate of electron capturing is higher than that of hole capturing, the current decreases and the Vth drifts forward [9,10]. On the other hand, the generated hot carriers are momentarily accelerated by the concentrated electric field. Then the carriers break the Zn-O bond, which is the weakest bond in an IGZO matrix. The broken Zn-O bond forms an acceptor like an electron trap site, which could degrade the electron transport [11]. The atomic ratio of each metal element in the IGZTO material was tested, and the content of Zn was the highest. through first-principles density functional theory calculations, we obtained the binding energies of oxygen with various metal elements in IGZTO, as shown in Table 1, where the binding energies of Zn-O are lowest, making them the most susceptible to breakage and forming defect states during collision ionization. Figure4(a) shows the mechanism diagram of the DCD phenomenon in IGZTO TFTs. According to the mechanism analysis described, after the DCD phenomenon, the defect states in the TFT channel are divided into three regions. like Figure4(b)shows, the density of states (DOS) near the drain of the channel increases, while the rest regions of the channel maintains the initial DOS like before DCD phenomenon.

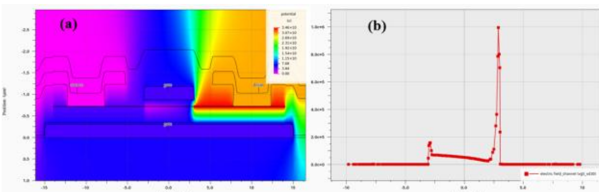

Figure 3. (a) potential distribution (b) channel electric field distribution at V_{GS}=5V and V_{DS}=30V TCAD simulation.

Table 1. Oxygen bond dissociation energy of each binary oxide in IGZTO matrix

Bond	In-O	Ga-O	Zn-O	Sn-O
Dissociation energy of diatomic bond (eV)	2.04	2.56	1.94	2.26

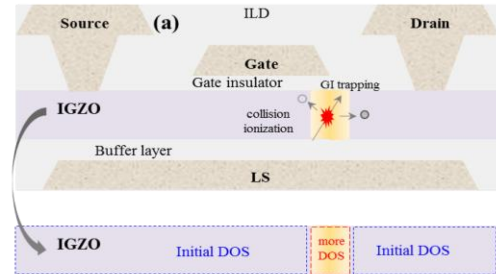

Figure 4. The mechanism diagram of the DCD phenomenon in TFT and DOS setting in TCAD.

The TCAD simulation DOS parameter settings are shown in Table 2, the comparison reveals a significant increase in acceptor-like defect states. Figure 5(b) and Figure 5(c) shows the changes in the energy band distribution diagrams of the DOS in the two regions, Figure 5(a) shows the IDVG curve of TCAD simulated and Experiment, which accurately reproduced the DCD phenomenon. Therefore, it can be reasonably deduced that the change of the transfer characteristics of IGZO-TFTs after the DCD phenomenon is a combination of a defect creation and an electron trapping.

Table 2. sub-gap DOS parameters in TCAD simulation

	Parameter	Unit	Initial	After DCD	
			Channel	Channel	Near-Drain channel
DOS Parameters	Nta	$cm^{-3}\cdot eV^{-1}$	0.8e20	0.8e20	1.2e22
	Wta	eV	0.025	0.025	0.04
	Nga	$cm^{-3}\cdot eV^{-1}$	5e17	5e17	1e19
	Wga	eV	0.06	0.06	0.067
	Ntd	$cm^{-3}\cdot eV^{-1}$	1e20	1e20	1e20
	Wtd	eV	0.05	0.05	0.05
	Ngd	$cm^{-3}\cdot eV^{-1}$	2e17	2e17	2e17
	Wgd	eV	0.1	0.1	0.1

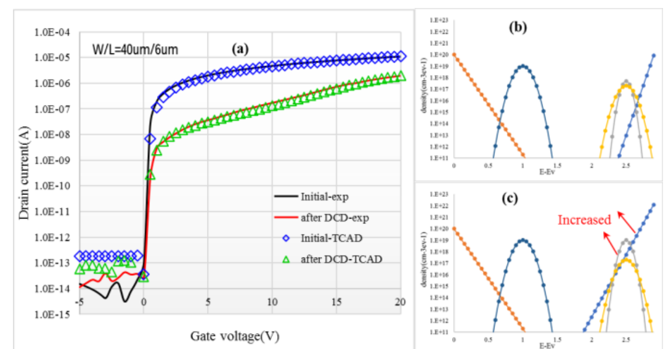

Figure 5. (a) simulation & Experimental IV curve (b) initial DOS (c) DOS in collision ionization region after DCD.

4. Results and Discussion

To improve the DCD phenomenon, we established devices of different sizes and simulated their internal electric field distribution under the same saturation region conditions using TCAD. The results show that as the channel length increases, the maximum electric field value in the channel pinch-off region tends to decrease, as shown in Figure 6(a); whereas changes in device width do not affect the maximum electric field value in the pinch-off region, as shown in Figure 6(b), and reducing the drain voltage lowers the maximum electric field value.

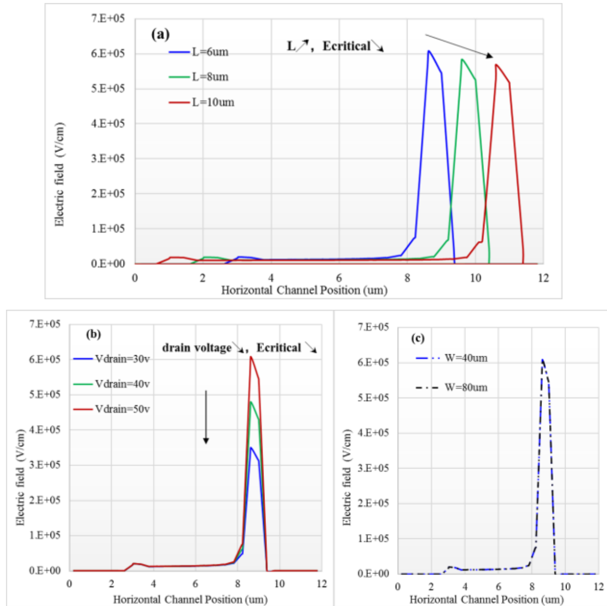

Figure 6. Channel horizontal electric field of (a) TFT channel length (b) drain voltage (c) TFT width.

Based on the relationship between channel length and the horizontal electric field, we tested the VFP of TFT devices with different channel lengths under the same process conditions, and the results showed that as the channel length increases, the VFP value increases, and the maximum critical electric field in their corresponding states is comparable; as shown in Figure 7(a). With this conclusion, we simulated the maximum critical electric field of devices with different structures using TCAD to predict the VFP of the devices, as shown in Figure 7(b). The results indicated that increasing L is beneficial for enhancing VFP, but the improvement tends to decrease after L increases to a certain extent.

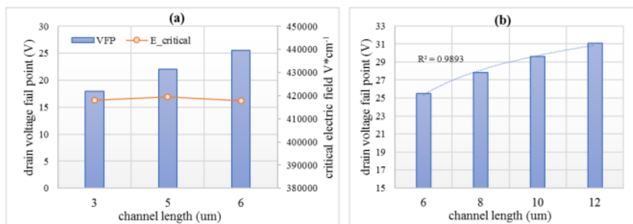

Figure 7. (a) Experimental VFP by channel length and Critical electric field at DCD phenomenon (b) Simulation VFP by channel length

Optimizing the device size can improve the VFP value, but the degree of improvement is limited. Therefore, we established four different device structures in the hope of further enhancing the VFP value and mitigating the DCD phenomenon. By simulating the internal potential distribution of the devices using TCAD, as shown in Figure 8, and extracting their channel horizontal electric fields, as shown in Figure 9, we found that the maximum electric fields of the TG LS-Gate and LS-Source structures are comparable, while the TG without-LS shows a significant reduction. The TG Double-Gate structure, by slightly reducing the conductivity at both ends of the channel, can simultaneously lower the maximum electric field. However, this approach can increase the source-drain transfer resistance, leading to a decrease in drain current. Therefore, when using this structure, it is necessary to comprehensively assess the degree of conductivity. The TG without-LS and TG Double-Gate structures can effectively reduce the maximum electric field in the pinch-off region, which is beneficial for the enhancement of the device's VFP.

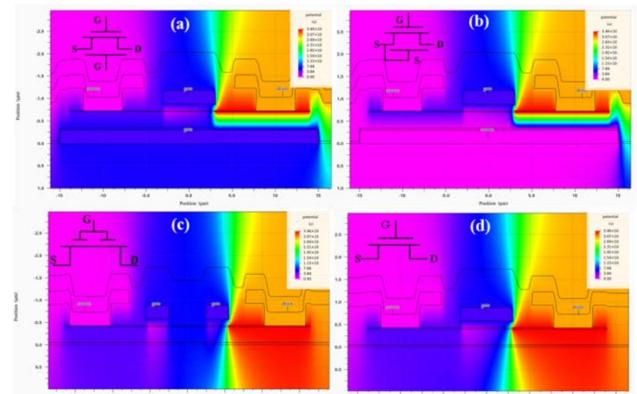

Figure 8. Potential distribution of (a) TG LS-Gate (b) TG LS-Source (c) TG Double-Gate and (d) TG without-LS.

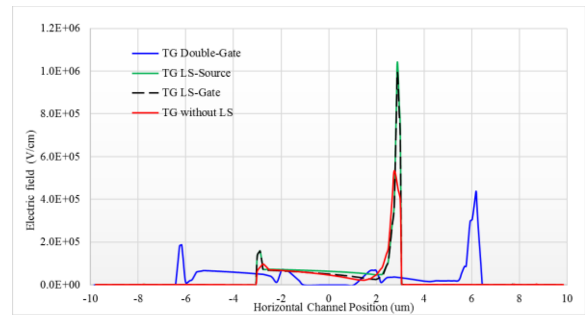

Figure 9. Channel horizontal electric field of (a) TG LS-Gate (b) TG LS-Source (c) TG Double-Gate and (d) TG without-LS.

Finally, it is worth mentioning that the TCAD simulation modeling in this paper was carried out using an AI-TCAD combined high-efficiency intelligent tuning model. The model includes a rapid tuning model based on an MLP regressor and a particle swarm optimization algorithm, as well as a fine-tuning model based on physical model TCAD device simulation, the logical algorithm of which is shown in Figure 10. Originally, it would take an ordinary engineer 2 to 3 days to complete the manual modeling, but with the assistance of the AI-TCAD intelligent algorithm, the modeling work can be completed in one day, significantly improving tuning efficiency. The development of this model is still ongoing, and in the future, we will further expand and optimize the application modules of AI in TCAD simulation.

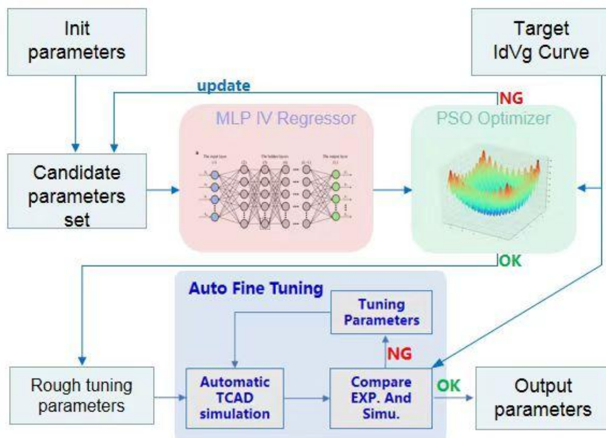

Figure 10. Parameter optimization algorithm logic base on AI-TCAD

5. Conclusion

In summary, to mitigate the DCD phenomenon in IGZTO high-mobility oxide TFT devices in circuits, TCAD simulation was used to reproduce the Transfer characteristic performance degradation caused by the hot-carrier effect under the influence of high electric field in the pinch-off region, leading to an increase in channel defects at the drain end and device degradation. The impact trend of device structure on the DCD phenomenon was explored, with width having no effect, while an increase in channel length being beneficial for improving the DCD phenomenon. The TG without-LS and TG Double-Gate structures showed a significant advantage over the TG LS-Gate and LS-Source structures. This provides design references for the application of IGZTO high-mobility devices and helps avoid device circuit failure due to the DCD phenomenon.

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7. References

[1] T. Takahashi, R. Miyanaga, M. Fujii, J. Tanaka, K. akechi, H. Tanabe, J. Bermundo, Y. Ishikawa, Y. Uraoka, Hot carrier effects in InGaZnO thin-film transistor, Applied Physics Express, 12 (2019) 094007

[2] T. Kamiya and H. Hosono, "Material characteristics and applications of transparent amorphous oxide emiconductors," NPG Asia Mater., vol. 2, no. 1, pp. 15–22, Jan. 2010, doi: 10.1038/asiamat.2010.5.

[3] M. H. Cho et al., "Impact of cation compositions on the performance of thin-film transistors with amorphous indium gallium zinc oxide grown through atomic layer deposition," J. Inf. Display, vol. 20, no. 2, pp. 73–80, Apr. 2019, doi: 10.1080/15980316.2018.1540365.

[4] P. Barquinha, A. Pimentel, A. Marques, L. Pereira, R. artins, E. Fortunato, Influence of the semiconductor thickness on the electrical properties of transparent TFTs based on indium zinc oxide, Journal of non-crystalline solids, 352 (2006) 1749-1752

[5] Il Man Choi, Min Jae Kim, Achieving High Mobility and Excellent Stability in Amorphous In–Ga–Zn–Sn–O Thin-Film Transistors IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 67, NO. 3, MARCH 2020

[6] X.-H. Lu et al., "Highly reliable amorphous indium-gallium-zinc-tin oxide TFTs with back-channel-etch structure," SID Symp. Dig. Tech.Papers, vol. 48, no. 1, pp. 291–293, May 2017, doi: 10.1002/sdtp.11608.

[7] M. Ochi et al., "Electrical characterization of BCE-TFTs with a-IGZTO oxide semiconductor compatible with Cu and Al interconnections," SID Symp. Dig. Tech. Papers, vol. 46, no. 1, pp. 853–856, Jun. 2015.

[8] F. Jin, Y. Tian, J. Chen, Y. Yang, X. Liu, Z. Yan, B. Wang, Nonsequential double ionization of helium in IR+ XUV two-color laser fields: Collision-ionization process, Physical Review A, 93 (2016) 043417.

[9] Y. Kim, J. Smith, P. Jain, Harvesting multiple electron–hole pairs generated through plasmonic excitation of Au nanoparticles, Nature chemistry, 10 (2018) 763.

[10] J. Li, Z. Yuan, S. Chen, X. Gong, S. Wei, Effective and noneffective recombination center defects in Cu2ZnSnS4: Significant difference in carrier capture cross sections, Chemistry of Materials, 31 (2019) 826-833.

[11] Hyun-Woo Park, Jungmin Bae, Hara Kang, Dae Hwan Kim, et al. "A Study on the Hot Carrier Effect in InGaZnO Thin Film Transistors,"