Prediction of Electrical Properties in LnIZO Thin-Film Transistors Based on Machine Learning Solutions

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Abstract

High-mobility oxide thin-film transistors (TFTs) are promising candidates for high-end display applications. Traditional TFT process development involves performing design of experiments (DOEs) based on empirical process parameters, which can lead to significant experimental costs. In this study, we developed a predictive model for the electrical properties of high-mobility LnIZO TFTs using machine learning (ML) techniques, based on actual DOE data. The proposed model accurately forecasts the electrical performance of devices across various process conditions. Among the ML models and architectures evaluated, a stacking-based ML model demonstrates the highest predictive accuracy for electrical parameters. To improve interpretability and practical implementation, SHAP-based explainable AI (XAI) analysis was conducted to assess the influence of process parameters, and the model was encapsulated into a program. This approach significantly reduces the number of required DOEs and improves the efficiency of process development for high-mobility TFTs.

Author Keywords

Amorphous Oxide; Thin-film Transistor; High Mobility; LnIZO; Machine Learning.

1. Introduction

In recent years, thin-film transistors (TFTs) utilizing amorphous oxide semiconductors (AOS) as channel layers have emerged as pivotal components in future display devices and flexible electronics, owing to their exceptional performances [1]-[2]. The TFT backplane technology based on IGZO, a representative AOS material, has been commercialized and is widely applied in advanced display products. However, the electron mobility of IGZO TFTs is around 10 cm²/V·s, falling short of the requirements for next-generation technologies that typically demand mobility exceeding 30 cm²/V·s, or even higher in some cases [3]. High mobility in TFTs is crucial for mobile applications such as smart tablets and laptops, driven by the growing market demand for ultra-high resolution and high frame rates. In display backplanes, AOS TFTs can be manufactured using either bottom-gate or top-gate structures. Among these, top-gate TFTs with a self-aligned structure (SATG) demonstrate superior stability compared to bottom-gate counterparts. Moreover, the SATG structure enables the fabrication of TFTs with shorter channel lengths, a critical factor for achieving high-resolution and ultra-narrow bezel displays [4].

For SATG TFTs, device performances are primarily influenced by the fabrication process, making the optimization of process parameters crucial for achieving good electrical performances. Traditionally, process parameters are selected through design of experiments (DOEs), which is time-intensive and relies heavily on the expertise of experimenters. To overcome these limitations, AI-driven data technology offers an innovative approach to TFT process development. By leveraging existing data, AI can build predictive models to forecast outcomes, effectively replacing physical DOE experiments with virtual simulations. AI technology has recently gained significant attention in the display industry, with valuable applications in areas such as panel production, development and research [5]-[6]. It has been reported that AI can be utilized in the development of display materials, panel drive circuit design, layout design automation, and production defect detection. For instance, machine learning models have demonstrated the ability to accurately predict the luminescent characteristics of OLED materials, offering an efficient approach to design new OLED materials [7]. Similarly, developing a machine learning model that correlates AOS TFT DOE process parameters with electrical properties could significantly improve the efficiency and effectiveness of device process development.

In this paper, we developed a machine learning model that establishes a correlation between fabrication process parameters and the electrical characteristics of high-mobility amorphous LnInZnO (LnIZO) TFT devices. After comparing the performance metrics of different ML models and architectures, a stacked-based approach was selected to map process parameters to electrical properties. This model enables accurate prediction of the devices' electrical performance under various conditions through virtual experiments. Furthermore, SHAP XAI analysis was employed to evaluate the impact of individual process parameters on the model, offering a reliable reference for selecting process parameters in DOE experiments.

2. Experiment details

The schematic diagram of the AOS TFT device structure prepared in this paper is shown in Fig. 1, with the detailed fabrication process described in the following. Initially, a metal film was sputtered and patterned on a glass substrate to form a light-shielding layer (LS). Subsequently, SiN_x and SiO_2 buffer layers were deposited using plasma-enhanced chemical vapor deposition (PECVD), and an LnIZO semiconductor channel layer was sputtered and patterned on the buffer layers. Following this, the gate insulator (GI) layer and the metal top-gate electrode layer were deposited via PECVD and patterned consecutively. Plasma treatment was employed to form the source/drain regions. Then, the interlayer dielectric (ILD) layer was deposited via PECVD and patterned to create via holes. After sputtering and patterning to form the source/drain electrodes, the first passivation layer (PV1), planarization layer, and second passivation layer (PV2) were sequentially deposited and patterned with via holes. Finally, ITO was sputtered and patterned to form the pixel electrodes. Besides, devices underwent several annealing processes between each thin-film deposition step.

Upon completion of the device fabrication, the electrical properties are measured using a semiconductor parameter

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analyzer, with the LS layer grounded during the process. After obtaining the device transfer characteristic curves, key electrical parameters, including the threshold voltage (V_{th}), subthreshold slope (SS), linear mobility, and drain-induced barrier lowering (DIBL), are extracted. The method used for parameter extraction follows standard practices [8].

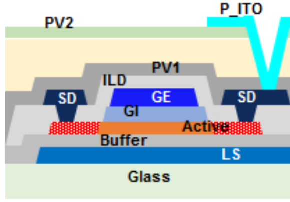

Figure 1. The schematic of AOS TFT device structure.

3. Proposed ML methodology

Fig. 2 illustrates the schematic of machine learning architecture for predicting electrical parameters of AOS TFT. DOE experiments involving process parameters of buffer layer, active layer, GI layer, ILD, PV1, and annealing are conducted and the resulting data are collected for ML modeling. The deposition process parameters of various film layers in TFT preparation process server as features for ML modeling, including the buffer layer power during PECVD deposition, the parameters of flow rates, pressure and temperature of different gases. The targets of ML model include the device's electrical parameters, such as V_{th}, Mobility, SS, DIBL, V_{th} range, and V_{th} 3σ. The first four parameters are the average values from 16 test points on the glass substrate, the V_{th} range represents the difference between the maximum and minimum V_{th} values, and the V_{th} 3σ is calculated from the V_{th} values.

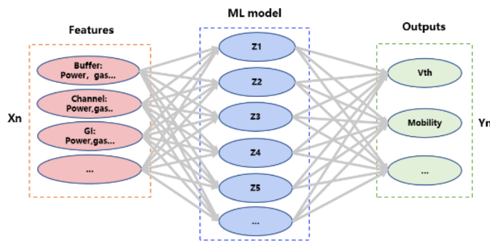

Figure 2. Schematic of illustrating input and output data of machine learning model.

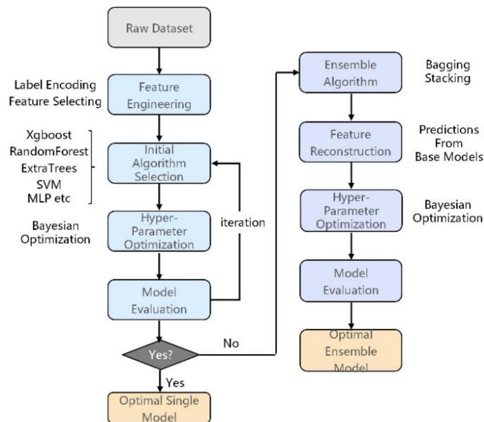

Figure 3. The process of training and selecting the optimal machine learning model for predicting electrical parameters of AOS TFT.

Fig. 3 illustrates the process of training and selecting the optimal machine learning model for predicting the electrical parameters of AOS TFTs. First, feature engineering is applied to the raw data, including encoding categorical labels and scaling features using a Min-Max scaler. Next, multiple algorithms, such as Random Forest, AdaBoost, SVM, Gradient Boosting, LightGBM, and ExtraTrees, are trained, and their prediction accuracy is compared. To enhance the generalization performance of these models, nested cross-validation and Bayesian optimization are used for hyperparameter tuning. Subsequently, models with strong performance are selected to construct bagging and stacking ensembles. For the bagging model, predictions are averaged across high-performing individual models. In the stacking model, a two-layer approach is implemented, with base models feeding into a meta-model. Finally, these three machine learning architectures are compared, and the best-performing model is chosen for predicting the electrical parameters. The model performance is evaluated using the metrics of MAE and RMSE, with their respective equations provided below:

$$MAE = \frac{1}{N}\sum_{i=1}^{N}[y_i - \hat{y}_i] \tag{1}$$

$$RMSE = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(y_i - \hat{y}_i)^2} \tag{2}$$

where y is the ground truth value, $\hat{y}$ is the predicted value, and $\bar{y}$ is the mean ground truth value.

Fig. 4 illustrates the schematic of nested cross-validation algorithm. It is a model evaluation technique that helps to mitigate overfitting and provides a more reliable estimate of a model's performance. It involves two levels of cross-validation. The outer loop is responsible for estimating the generalization performance of the model, while the inner loop is used to tune the model's hyper-parameters. In both inner and outer loops, 10-fold cross-validation is employed to split training and validation datasets.

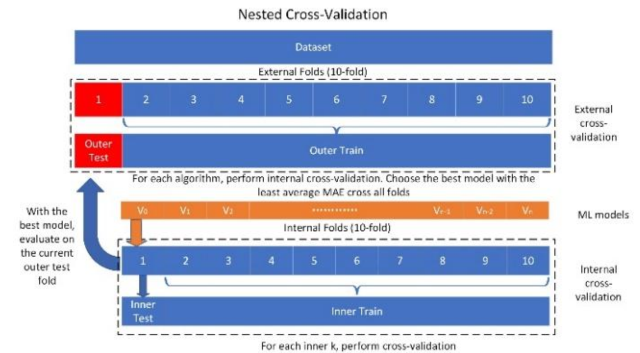

Figure 4. Schematic of nested cross-validation algorithm.

4. Results and Discussions

Several ML algorithms, including Gradient Boosting, LightGBM, Random Forest, ExtraTrees, Adaboost, SVR, and Linear Regression, are initially trained. The hyperparameters of these models are optimized using Bayesian optimization and nested cross-validation. Each model's performance is evaluated based on 10-fold cross-validation, with the mean and variance of the metrics calculated. Note that the R^2 metric is not included, as the size of the validation data is insufficient for its evaluation. As

shown in Table 1, Gradient Boosting (GB), Random Forest (RFR), Extra Trees (ETR), and Adaboost (Ada), demonstrate relatively better performance than the other models, and these four will be selected as the base models for constructing the bagging and stacking models. Notably, the Random Forest model achieves the lowest mean MAE and RMSE, making it the optimal single model for further comparison.

The bagging model is constructed using four parallel individual ML models, with the output being the average of their predictions. The stacking model consists of a base model and a meta model. The base model is made up of the four parallel ML models, and their predictions are used as features for the meta model. In this study, nine different meta models were compared, including Kernel Ridge, Ridge, Lasso, XGBoost, Random Forest, and others. Due to space limitations, a detailed comparison of the meta models is not provided here. In this research, the optimal meta model was found to be Random Forest, which will be used for further comparisons. As shown in Table 2, the bagging model achieves the highest accuracy for predicting Vth, mobility, and DIBL, while the single Random Forest model provides the most accurate predictions for SS. However, the stacking model yields the lowest errors for both Vth range and Vth 3σ. Overall, the stacking model demonstrates the best performance, delivering the lowest average error. Consequently, the stacking model, comprising the base models (GB, RFR, ETR, and Ada) and the meta-model (RFR), is selected as the optimal model for predicting electrical parameters.

Table 1. The performance comparisons of various single machine learning models.

Model	MAE	RMSE
GB	0.069±0.029	0.093±0.042
LGBM	0.095±0.039	0.121±0.057
RFR	0.063±0.027	0.085±0.041
ETR	0.066±0.027	0.089±0.04
Ada	0.075±0.028	0.098±0.043
SVR	0.316±0.026	0.334±0.021
LR	0.117±0.115	0.166±0.192

Table 2. The comparisons between the optimal single machine learning model and ensemble machine learning models.

Y	Random Forest		Bagging		Stacking	
	MAE	MSE	MAE	MSE	MAE	MSE
V_{th}	0.020	0.001	0.019	0.001	0.022	0.001
Mobility	0.046	0.003	0.042	0.002	0.046	0.003
SS	0.060	0.006	0.065	0.007	0.064	0.006
DIBL	0.051	0.004	0.046	0.004	0.048	0.004
V_{th} Range	0.033	0.002	0.041	0.003	0.029	0.002
V_{th} 3σ	0.022	0.001	0.028	0.001	0.021	0.001
Average	0.039	0.003	0.040	0.003	0.038	0.003

Fig. 5 presents the prediction performance of the stacking model tested on an independent dataset. The electrical parameters of the AOS TFT have been normalized in this figure for confidentiality. The predicted values of the various electrical parameters show strong alignment with the experimental values. Specifically, the coefficient of determination (R^2) scores for V_{th}, mobility, SS, DIBL, V_{th} range, and V_{th} 3σ are 0.54, 0.9, 0.78, 0.89, -0.41, and 0.01, respectively. Notably, while the R^2 scores for V_{th} range and V_{th} 3σ are low, this does not imply poor predictive performance for these parameters. In fact, their MAE scores are 0.03 and 0.02 respectively, indicating very low absolute errors. The low R^2 values actually result from the narrow data distribution of V_{th} range and V_{th} 3σ within the test dataset.

Table 3 presents the average prediction errors of the ML model for various electrical parameters. All prediction errors are within an acceptable range, hence the device electrical properties predicted under different process conditions based on this ML model are highly referential. It should be noted that the prediction error for SS is less than 0.01, which is related to the minimal fluctuation in device SS across different process DOEs.

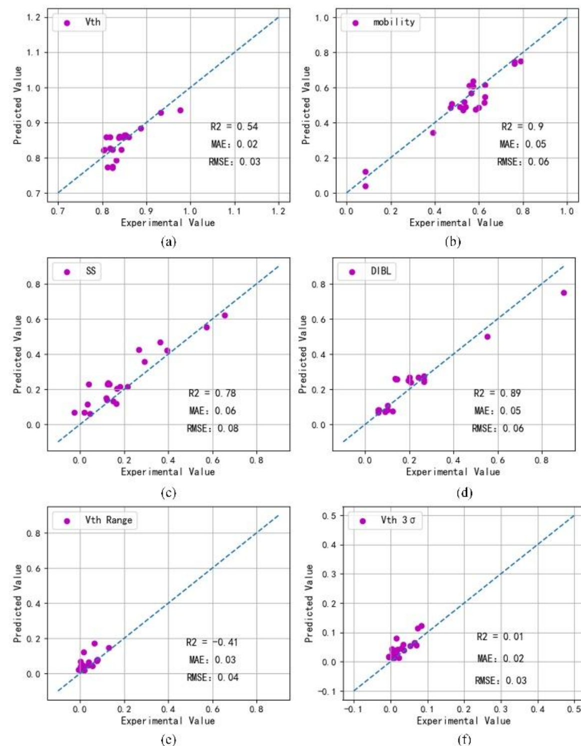

Figure 5. Performances optimal machine learning model for the normalized (a) V_{th}, (b) mobility, (c) SS, (d) DIBL, (e) V_{th} range and (f) V_{th} 3σ on the independent testing set.

Table 3. The average prediction deviations of the ML model for the device electrical parameters on the independent testing set.

Parameter	V_{th} (V)	Mobility (cm^2/Vs)	SS (V/dec)	DIBL	V_{th} Range (V)	V_{th} 3σ (V)
Deviation	0.130	0.1678	0.007	0.098	0.351	0.199

SHAP XAI analysis is employed to elucidate the impact of various input features on the output. This approach evaluates the importance of process parameters influencing the electrical performance of devices, offering a reliable reference for selecting process parameters in subsequent DOE experiments. Fig. 6 presents the SHAP plots for (a) V_{th}, (b) mobility, (c) SS, (d) DIBL, (e) V_{th} range, and (f) V_{th} 3σ. From the SHAP analysis, we identified the 10 most significant factors affecting the DOE

experiments and their respective influence trends. For instance, in the case of mobility, key process parameters include the plasma treatment time for the source/drain regions, the sputtering power and thickness of the active layer, the oxygen flow rate during active layer sputtering, and the plasma treatment time before GI deposition, among other potential factors.

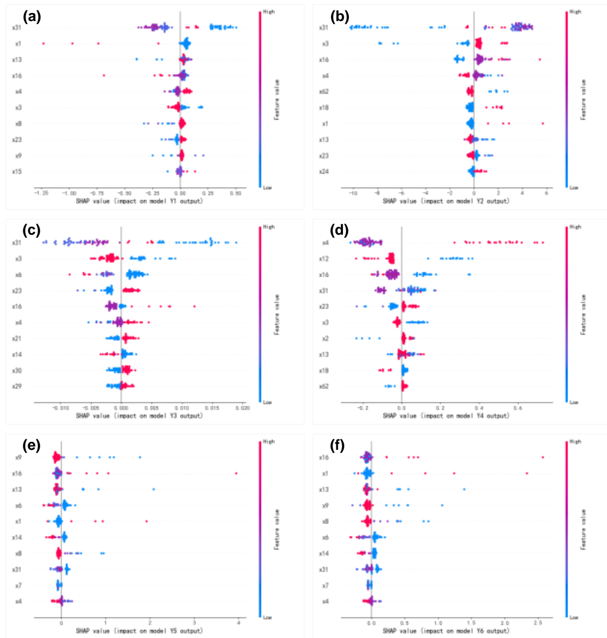

Figure 6. SHAP values of (a) V_{th}, (b) mobility, (c) SS, (d) DIBL, (e) V_{th} range and (f) V_{th} 3σ.

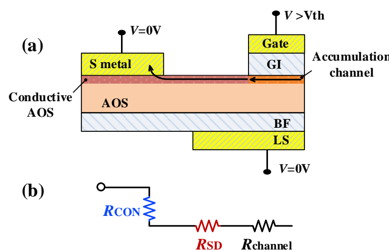

Figure 7. (a) Cross-sectional schematic diagram of the current path near the source region and (b) the total device resistance for a fabricated TFT.

Focusing on the plasma treatment time for the source/drain regions, Fig. 6(b) shows that longer treatment times under DOE conditions result in higher mobility. This is because, during the plasma treatment process, the surface of the AOS layer in the source/drain regions forms a conductive layer due to ion bombardment, as shown in Fig. 7(a) [9]. The conductivity of this conductive layer is positively correlated with the degree of bombardment. Insufficient treatment time leads to inadequate conductivity, introducing a significant parasitic resistance R_{SD} during device conduction as shown in Fig. 7(b), which results in a decrease of the extracted mobility [4]. Therefore, it is essential to ensure adequate plasma treatment duration to obtain a relatively higher device mobility. The analysis of the impact of other factors on electrical properties follows a similar rationale. Consequently, SHAP XAI analysis effectively identifies key process factors for each electrical parameter and, based on the target of electrical tuning, provides trends for adjusting these factors, offering guidance for subsequent device process optimization directions.

Finally, based on the aforementioned model, we have developed a web-based electrical property prediction program for DOE electrical property forecasting. By uploading a model trained on existing DOE electrical data and the required DOE conditions for prediction, electrical properties can be quickly predicted. The use of this program assists in the design of DOE schemes and enhances the efficiency of device fabrication process development. It is important to note that there is still potential for improvement in model optimization, particularly in enhancing the model's generalization ability beyond the training feature range. This remains a challenge that will continue to be addressed through ongoing efforts.

5. Conclusion

In this paper, we developed a machine learning model to establish a correlation between manufacturing process parameters and the electrical performance of high-mobility LnIZO TFTs, enabling accurate predictions of device performance under various process conditions. Additionally, we applied SHAP for explainable artificial intelligence (XAI) analysis, offering a reliable reference for selecting process parameters in DOE experiments. These research methods enable rapid and accurate prediction of device electrical performances, significantly reducing the number of required DOE experiments and enhancing the efficiency of fabrication process development.

6. References

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