High-Performance P-Type Tellurium-Based Thin-Film Transistors on a 6-in. Wafer and Their Applications

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Abstract

Here, we report on the sputtered p-type Tellurium (Te) thin-film transistors (TFTs) and circuits with high device performances. We also fabricate and optimize the device characteristics of p-type Te TFTs with sub-100 nm channel length using a novel photolithography method. Finally, vertically integrating p-type TFTs with n-type ones are demonstrated for monolithic 3- dimensional (M3D) applications.

Author Keywords

Tellurium; short-channel; thin-film transistor; monolithic 3D integration; heterostructure

1. Introduction

As silicon-based transistor technology approaches its fundamental physical limitations, researchers and engineers have increasingly turned their attention to innovative approaches such as monolithic three-dimensional (M3D) integration, which has emerged as a highly promising solution to sustain the progress of device scaling. M3D integration facilitates the vertical stacking of electronic devices, thereby enabling a significant increase in device density within the same physical area. To successfully implement M3D technology, particularly on top of complementary metal oxide-semiconductor (CMOS) devices, it is crucial to employ low temperature processing techniques, specifically those operating below 400°C, in order to preserve the performance and integrity of the pre-existing circuits situated underneath. Given the stringent requirements for low-temperature processability, large-scale uniformity, transparency, and outstanding electrical properties, metal oxide semiconductors have emerged as some of the most suitable candidate materials for enabling M3D integration [1,2]. Despite the successful development and widespread commercialization of n-type thin-film transistors (TFTs) based on metal oxide semiconductors, the progress in achieving high performance p-type metal oxide TFTs has been significantly less advanced. This has created a substantial challenge in the development of p-type semiconductors that are capable of realizing TFTs with high performance and reliability. Recently, however, the semiconductor material Tellurium (Te) has garnered considerable attention as a highly promising candidate for p-type semiconductors, owing to its remarkable electrical properties. These properties include thickness-dependent bandgaps, tunable optical characteristics, and high charge carrier mobility, which collectively make Te an attractive material for advanced applications [3]. In this study, we conduct a systematic investigation into the structural, optical, and electrical properties of sputtered Te films by utilizing a comprehensive set of characterization techniques, including X-ray photoelectron spectroscopy (XPS), ultraviolet-visible spectroscopy (UV-Vis), X-ray diffraction (XRD), transmission electron microscopy (TEM), and atomic force microscopy (AFM). By optimizing the properties of Te films, we demonstrate the fabrication process and evaluate the performance characteristics of p-type Te TFTs with ultra-short channel lengths measuring below 100 nm. These TFT devices are fabricated using an innovative photolithography technique and exhibit exceptional electrical performance, characterized by a mobility exceeding 14 $cm^2/V \cdot s$ and an on/off current ratio greater than 10^4, achieved at a low processing temperature of 150°C. Finally, we extend our exploration to investigate the integration of these p-type TFTs with their n-type counterparts, highlighting their potential for use in M3D integration applications.

2. Experiment

Fig. 1 illustrates the detailed method employed for fabricating TFT devices with sub-100 nm channel lengths, which has been adapted from a previously established approach used for the creation of short-channel n-type metal oxide TFTs [4]. To summarize the process in greater detail, it begins with the formation of the initial source/drain electrode. This is achieved through the deposition of a molybdenum (Mo) film, followed by its precise patterning using a negative-tone photoresist (PR). Subsequently, a second source/drain electrode, also composed of Mo, is deposited directly on top of the patterned negative PR. Once this deposition step is complete, the negative PR is removed using acetone, leaving behind the patterned Mo electrodes. Following the electrode formation, the channel material, which is a 7 nm-thick layer of Te, is deposited via DC sputtering under specific conditions, including a DC power of 20 W. After the deposition of the Te film, a dry etching process is carried out to define the channel region. To complete the TFT structure, a dielectric layer composed of aluminum oxide (Al_2O_3) with a thickness of 10 nm is deposited. This dielectric layer is prepared using plasma-enhanced atomic layer deposition conducted at a low temperature of 150°C, ensuring compatibility with low-temperature processing requirements. The electrical properties of the fabricated TFT devices are evaluated using an Agilent B1500A semiconductor parameter analyzer, enabling precise measurements of their performance characteristics. **Fig. 2** provides a comprehensive view of the fabricated Te TFT devices on a 6-inch glass substrate. It includes a schematic representation of the device structure and a cross-sectional TEM image. The TEM image reveals that the channel length of the Te TFT devices is approximately 75 nm, highlighting the successful realization of ultra-short channel lengths. Finally, as a demonstration of their potential application in M3D integration, the vertical integration of p-type Te TFTs with n-type aluminum-doped indium-zinc-tin-oxide (Al-IZTO) TFTs is successfully implemented. This integration underscores the feasibility of utilizing these advanced devices in next-generation M3D architectures.

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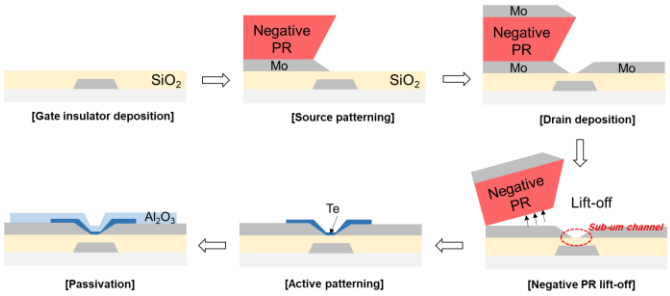

Figure 1. Schematic process for fabricating TFT devices with sub-100 nm channel lengths.

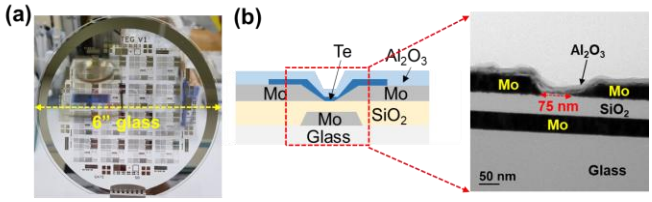

Figure 2. (a) Te TFT devices on a 6-inch glass substrate, (b) a schematic and a cross-sectional TEM image of Te TFTs.

3. Results and Discussion

The transfer and output characteristics of the fabricated Te TFTs are presented in **Figs. 3**(a) and 3(b), respectively, showcasing their excellent electrical performance. For the transfer characteristics, the gate voltage was swept from +10 V to -20 V, while the drain voltage was fixed at -1 V and -10 V for the respective measurements. The critical device parameters were calculated from the transfer curves obtained in the saturation region using the equation $I_d = (WC_i/2L)\mu_{sat}(V_g–V_{th})^2$, where W and L are the channel width and length, respectively, μ_{sat} is the saturation mobility, and C_i is the capacitance per unit area of the gate insulator. The Te TFTs exhibits a high μ_{sat} over 14 $cm^2\ V^{-1}\ s^{-1}$, and an on/off ratio over 10^4 (W/L=50 um/10 um), and μ_{sat} over 3 $cm^2\ V^{-1}\ s^{-1}$, and an on/off ratio over 10^4 with sub-100 nm channel length. Fig. 3(b) presents the output characteristics of the Te TFTs, displaying the relationship between the I_d and the V_d for various V_g set at 0, -5, - 10, -15, and -20 V. These measurements confirm the robust output behavior of the devices under the applied conditions. Importantly, all the electrical properties of the Te TFTs were evaluated in a controlled environment, conducted in the dark under ambient conditions, ensuring that the results reliably represent the intrinsic performance of the devices without interference from external factors such as light or temperature fluctuations. To better understand the origin of the high mobility observed in Te TFTs, we conducted an in-depth analysis of the structural and optical properties of Te thin films deposited under varying conditions. This comprehensive investigation employed advanced characterization techniques, including XPS, UPS, AFM, and XRD. By carefully optimizing the oxygen partial pressure in the argon (Ar) gas during the DC sputtering process, we were able to partially oxidize the Te thin films, leading to the formation of a tellurium dioxide (TeO_2) phase. This optimization proved to be a critical step, as it was confirmed that increasing the bandgap of Te through the presence of TeO_2 effectively reduced the off-current in the Te TFT devices, thereby enhancing their overall electrical performance [5].

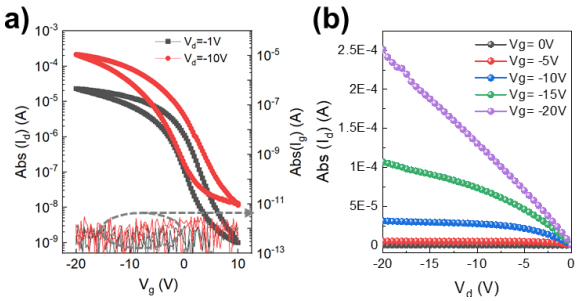

Figure 3. (a) The transfer curves and (b) the output characteristics of the Te TFTs with sub-100 nm channel length.

The presence of the TeO_2 phase within the Te thin films was verified through XPS and XRD analyses. These techniques provided clear evidence of the partial oxidation and the structural integration of TeO_2 within the films. Furthermore, UPS analysis corroborated the findings by demonstrating an increase in the bandgap of the Te films, which was directly attributed to the introduction of the TeO_2 phase. This bandgap engineering played a key role in suppressing the leakage current, which is crucial for improving the performance and reliability of the TFT devices. Building upon the optimized Te thin film, p-type Te TFTs were fabricated and utilized as M3D-stacked devices integrated on top of n-type Al-IZTO TFTs, as depicted in **Fig. 4.** In this design, the top gate electrode of the n-type TFT was reconfigured to serve as the bottom gate electrode for the overlying p-type device. The fabrication of the p-type TFTs included the addition of a dedicated top gate electrode, resulting in a dual-gate structure for both the ntype and p-type devices. This innovative architecture not only enabled the independent operation of each device but also facilitated their seamless integration into a vertical stack. As shown in Fig. 4(b), the vertically stacked n-type and p-type TFTs were interconnected to form an inverter, a fundamental building block for digital circuits. The electrical characteristics of this inverter were thoroughly evaluated, and the results demonstrated its robust performance, thereby confirming the feasibility and potential of M3D integration for advanced electronic applications. These findings underscore the capability of Te-based p-type TFTs to complement n-type devices, paving the way for the development of high-performance, vertically integrated electronic systems.

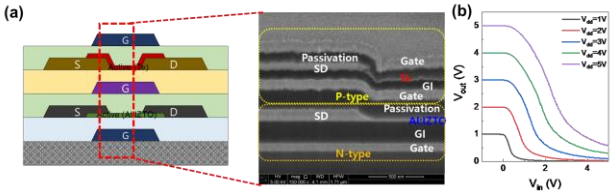

Figure 4. (a) The M3D integration of p-type Te and n-type Al-IZTO TFTs, and (b) inverter characteristic.

4. Conclusion

In this work, we explored the structural, optical, and electrical properties of sputtered Te films through comprehensive analyses. Utilizing the optimized Te films, we developed a novel fabrication process for p-type Te TFTs with sub-100 nm channel lengths, achieving impressive electrical performance at a low processing temperature of 150 °C. Furthermore, we demonstrated the potential for M3D integration by successfully combining these p-type TFTs

with n-type devices, highlighting their suitability for advanced electronic applications.

5. Acknowledgements

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6. References

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