# IGZO-Based Synaptic Transistors for Neuromorphic Applications

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## Abstract

*In this paper, we introduced indium-gallium-zinc oxide (IGZO) synaptic transistors based on charge trapping. By employing a degenerate IGZO trap layer, electron de-trapping efficiency was significantly improved. Additional process optimization was conducted to address the insufficient device characteristics as a synapse, resulting in notable improvements in program/erase and retention performance. The optimized device exhibits improved electrical characteristics, highlighting their potential as promising candidates for neuromorphic applications.*

## Author Keywords

Neuromorphic computing; InGaZnO (IGZO); Synaptic transistor; Spiking neural network (SNN)

## 1. Introduction

With the exponentially growing demands of data processing, neuromorphic computing has been considered a next-generation computing technology that can replace the inefficient computing system based on the Von Neumann architecture [1]. It enables efficient computation by minimizing data movement through parallel processing using artificial synapses and neurons, which mimic the mechanisms of the human brain [2]. For implementing a hardware-based neuromorphic computing system, developing artificial synapses that can mimic synaptic plasticity is essential [3]. Many studies have focused on the development of high-performance synaptic devices exhibiting the capability to achieve linear potentiation/depression, multi-state retention, and high endurance [4]. Recently, indium-gallium-zinc oxide (IGZO), which is expanding its applications beyond displays to fields like DRAM and sensors, is also being used in synapse development using various mechanisms such as ferroelectric, light stimulation, and charge trapping [5].

Charge trapping-based IGZO synaptic transistors offer advantages such as CMOS compatibility, linear conductivity control, and stable weight updates [6, 7]. However, this type of device has the drawback of low charge de-trapping efficiency because it is difficult to supply holes from the n-type IGZO channel, relying solely on electron de-trapping [8]. Thus, previous studies had to temporarily generate holes by illuminating the channel with light to increase charge de-trapping efficiency [9, 10]. To address this issue, our group recently employed degenerate IGZO as a trap layer to improve charge de-trapping efficiency without using light [7]. However, there remain challenges that need improvement to meet the performance required for synapses: insufficient retention and high programming voltage (~20 V). Therefore, additional device engineering is necessary to enhance these properties so that IGZO synaptic transistors can become a promising candidate for synapses.

In this paper, we introduce our progress on charge trapping-based synaptic transistors based on IGZO. We found that IGZO can be used not only as a channel but also as a trap layer when IGZO is in a degenerate state. Trapped electrons in the IGZO trap layer can act as free electrons, and the voltage drop across the trap layer is negligible, enabling Fowler-Nordheim (FN) tunneling with enhancing charge de-trapping efficiency. In addition, we successfully implemented long-term potentiation (LTP) and long-term depression (LTD), which are essential characteristics for synapses. However, the device had drawbacks such as poor retention and the need for a high voltage of 20 V to modulate the channel conductance. To overcome these issues, we optimized the synaptic transistor to improve the retention of multi-level conductance states and scale down the voltage program/erase.

## 2. Degenerate IGZO trap layer for improving charge de-trapping

We fabricated synaptic transistors using IGZO as both channel and trap layers, as shown in Fig. 1(a). A heavily p-type Si substrate was prepared. A 58 nm $Al_2O_3$ blocking layer (BL) was deposited using atomic layer deposition (ALD) using $H_2O$ reactant and trimethylaluminum (TMA) precursor. Then, the IGZO trap layer (40 nm) was formed using the RF reactive sputtering with oxygen partial pressure ($P_{O2}$) of 0%,1%, and 2% and a wet etching process. A 7 nm $Al_2O_3$ tunneling layer (TL) was deposited using the ALD with the same process condition as the blocking layer. A 40 nm IGZO channel was deposited by RF reactive sputtering and patterned by a wet etching process. The e-beam evaporated Ti (70 nm) was used as source/drain electrodes. Finally, the devices were annealed at 200 °C for 0.75 hours in an air atmosphere.

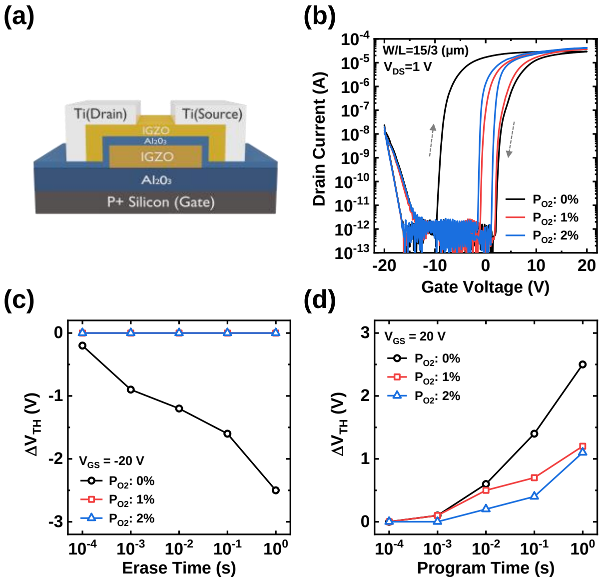

**Figure 1.** (a) Cross-sectional schematic of the synaptic transistor employing IGZO as both channel and trap layers. (b) Transfer curves of the synaptic transistors under different $P_{O2}$ conditions (from 0% to 2%) during IGZO trap layer deposition. Comparison of $\Delta V_{TH}$ for (c) program and (d) erase operations using various voltage pulses according to $P_{O2}$ [7].

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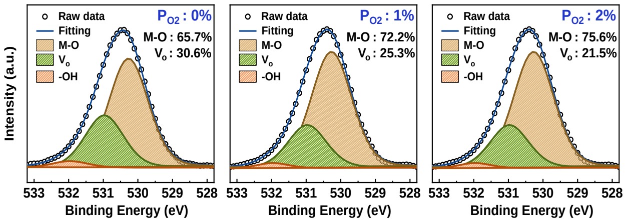

**Figure 2.** Fitting results of O 1s spectra of IGZO trap layer with respect to $P_{O2}$ [7].

Previously reported charge trapping-based IGZO devices adopting high-κ trap layers show the difficulty of de-trapping electrons trapped in deep states in trap layers [9, 10]. To improve de-trapping efficiency, it is important to utilize the trap sites near the conduction band ($E_c$), and IGZO, which has many donor states near $E_c$, can be an optimal candidate for the trap layer. In addition, the Fermi level ($E_f$) also plays a crucial role in determining the active trap/de-trap levels. Therefore, we investigated the effect of $P_{O2}$ on the IGZO trap layer because these characteristics can be modulated by $P_{O2}$ during the deposition of the trap layer [11, 12]. First, transfer curves of the synaptic transistors were measured with respect to $P_{O2}$. It is noted that the device with $P_{O2}$ of 0% shows the largest hysteresis window of 10.6 V when double-sweeping the gate voltage from -20 V to 20 V (Fig. 1(b)). For comparison of electron trapping/de-trapping efficiency for $P_{O2}$, program and erase operations were measured using voltage pulses with different widths, as shown in Fig. 1(c) and (d). For the program operation where electron trapping occurs, threshold voltage shift ($\Delta V_{TH}$) was observed under all $P_{O2}$ conditions. However, for the erase operation, $\Delta V_{TH}$ due to electron de-trapping was observed only at $P_{O2}$ of 0%, with no $\Delta V_{TH}$ appearing at $P_{O2}$ of 1% and 2%. This indicates that electron de-trapping behavior is highly sensitive to $P_{O2}$.

To examine the effect of $P_{O2}$, we analyzed the oxygen vacancy concentration related to donors and the Fermi level ($E_f$). First, depth profiling using X-ray photoelectron spectroscopy (XPS) was performed on samples that have the same material stack as the synaptic transistor to compare the oxygen vacancy concentration. As shown in Fig. 2, the trap layer with $P_{O2}$ of 0% shows the highest oxygen vacancy concentration of 30.6%, and it decreases with increasing $P_{O2}$ due to the formation of stable metal-oxygen bonds and a decline in oxygen-deficient states during the deposition of IGZO. Since the position of $E_f$ depends on the concentration of oxygen vacancy acting as donors, the band structure of the IGZO trap layer was examined by using ultraviolet-visible (UV-vis) spectroscopy and ultraviolet photoelectron spectroscopy (UPS) measurements (Fig. 3(a)). Only at $P_{O2}$ of 0%, a degenerate state was observed where $E_f$ is above the $E_c$, indicating that the IGZO trap layer exhibits metallic characteristics. In contrast, at $P_{O2}$ of 1% and 2%, non-degenerate characteristics were observed, implying that trap sites below $E_c$ can be utilized for electron trapping and de-trapping. Fig. 3(b) and (c) illustrate the comparison of charge transport mechanisms during the erase operation. Regarding the $P_{O2}$ of 0% case, the metallic trap layer allows the voltage drop across it to be negligible, inducing a large voltage drop across the $Al_2O_3$ TL with FN tunneling. In contrast, band bending occurs in the trap layer at $P_{O2}$ of 1% and 2%, reducing the electric field across the TL and leading to direct tunneling rather than FN tunneling. Additionally, electrons in trap sites below $E_c$ demand additional energy to de-trap, making charge de-trapping more difficult.

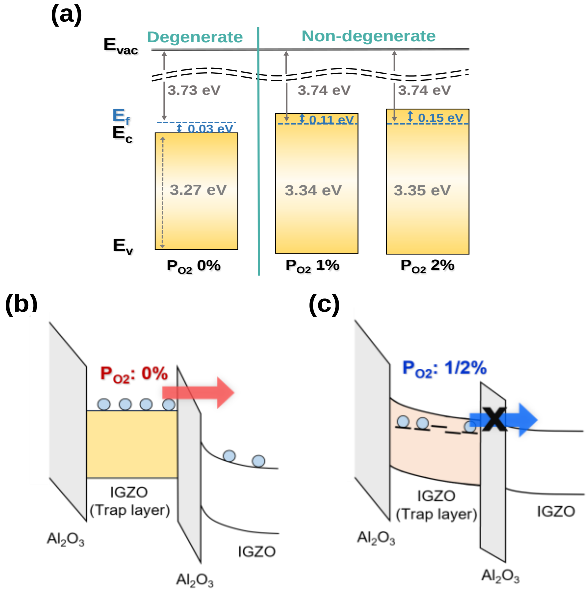

**Figure 3.** (a) Band alignment of the IGZO trap layer at different $P_{O2}$ based on UV-vis and UPS measurements. Mechanism comparison for erase operation (charge de-trapping) of the synaptic transistors for the case of (b) degenerate IGZO and (c) non-degenerate IGZO trap layers [7].

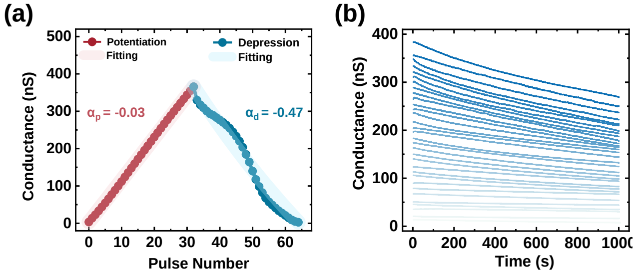

**Figure 4.** (a) LTP/LTD measurement and fitting results of the synaptic transistor. (b) Retention characteristics of multi-state for $10^3$ seconds [7].

To evaluate the synaptic plasticity of the synaptic transistor, we measured the LTP and LTD using the consecutive voltage pulses, where 32 identical negative voltage pulses (-20 V/1 ms) and 32 incremental positive voltage pulses (6~20 V/35 ms) with 0.5 V steps were used, respectively. The device shows the capability of linear conductance modulation with low nonlinear factors $\alpha_p$ and $\alpha_d$ (ideal = 0). The nonlinear factors were calculated using the previously reported equations [13]. Retention characteristics for multiple states were measured for $10^3$ seconds, which showed an average conductance degradation of 30.42% after $10^3$ seconds (Fig. 4(b)). This insufficient retention may lead to a decline in network accuracy or increased system power consumption due to frequent weight refresh operations [14]. Thus, the retention of the synaptic transistor should be further enhanced to improve the performance of neuromorphic systems.

## 3. Device optimization toward high-performance synaptic transistors

To enhance the program/erase efficiency and retention characteristics of the synaptic transistors described above, we modified the material composition and process conditions. An indium-tin oxide (ITO) gate was patterned by a wet etching

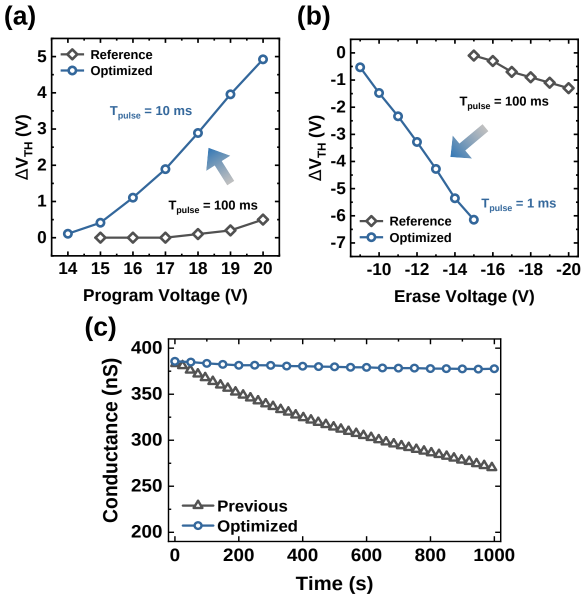

**Figure 5.** Comparison of $\Delta V_{TH}$ for (a) program and (b) erase operations using various voltage pulses between reference and optimized devices. (c) Improved retention of the optimized device.

process. To increase the electric field across the tunneling layer at a lower voltage, a thinner $Al_2O_3$ blocking layer was deposited using ALD. Then, a floating gate was formed, exhibiting higher conductivity than the IGZO trap layer. Achieving high conductivity of the trap layer is crucial for obtaining high efficiency of electron de-trapping [15]. A thicker $Al_2O_3$ tunneling layer was deposited using the ALD process to improve the retention characteristics. An IGZO channel was formed, and subsequently, the $Al_2O_3$ passivation layer was deposited. The devices were annealed at 150 ℃ for 1 hour in an air atmosphere.

Fig. 5(a) and 5(b) present the comparison of program and erase operations between the reference device (Fig. 1(a)) and the optimized device. The optimized synaptic transistor shows a larger $\Delta V_{TH}$ in both program and erase using voltage pulses of lower magnitude and shorter width. Specifically, regarding the program operation, the reference device required applying a voltage pulse of 20 V for 100 ms to attain a $\Delta V_{TH}$ of 0.5 V. In contrast, the optimized device exhibited a large $V_{TH}$ shift of 4.92 V with a shorter voltage pulse of 20 V for 10 ms. Similarly, in the erase operation, the reference device showed a minimal $\Delta V_{TH}$ of -0.1 V at -15 V for 100 ms, whereas the optimized device exhibited a large $\Delta V_{TH}$ of -6.15 V even with a shorter voltage pulse of 1 ms at the same voltage magnitude. Furthermore, the optimized device exhibited superior retention, where the conductance decreased by only 2.1% after $10^3$ seconds, as shown in Fig. 5(c). The synaptic transistor's characteristics were significantly improved through process modifications, indicating that the synaptic transistor has the potential for neuromorphic applications.

## 4. Conclusion

In summary, we introduced the synaptic transistor using IGZO as both channel and trap layers and found that degenerate IGZO plays a crucial role in improving the electron de-trapping efficiency. Although the device successfully implemented the synaptic plasticity of LTP/LTD, two challenges remain for meeting the requirements as an artificial synapse: insufficient retention and high voltage (20 V) for LTP/LTD. To address these issues, we engineered the fabrication process of the synaptic transistor. As a result, the optimized synaptic transistor showed a larger $\Delta V_{TH}$ using a lower magnitude and shorter width of voltage pulses compared to the reference device. In addition, the conductance state was sustained for $10^3$ seconds with a minimal decrease in conductance. We expect that the IGZO synaptic transistor employing charge trapping can be one of the promising synapse candidates for neuromorphic computing.

## 5. Acknowledgements

This research was supported by National R&D Program through the National Research Foundation of Korea(NRF) funded by Ministry of Science and ICT (RS-2024-00402495).

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