Design of OLED Capacitance by Material Combinations

Alexander Schubert*†, Falk May*, Sebastian Meyer*, Sebastian Stolz*, Jens Engelhart*, Natalie Tober*, Martin Kraska*, and Christof Pflumm*

***The Electronics business of Merck KGaA, Darmstadt, Germany**
†Alexander.Schubert@emdgroup.com

Abstract

Organic Light Emitting Diodes (OLEDs) are intricate multi-layer devices that play a pivotal role in modern display and lighting technologies. The transient phenomena associated with OLED panels, such as higher refresh rates and the integration of behind-screen cameras or sensors, necessitate rapid (de)charging of pixels, which is intrinsically linked to their capacitance characteristics. At the interfaces of different materials, charge carriers encounter abrupt changes in the energy landscape, often leading to accumulation effects that are evident in the capacitance-voltage curves. In this study, we demonstrate how the selection and combination of OLED materials across various layers can be aligned to engineer capacitance properties through dielectric spectroscopy and drift-diffusion simulations. Our findings reveal that one of the key parameters influencing capacitance is the polarity of the layers, which is attributed to spontaneous orientation polarization.

Author Keywords

OLED; Capacitance-Voltage Characteristics; Spontaneous Orientation Polarization (SOP); Material Polarity Factors (MPF); Hole Transport Materials (HTM); Triplet Matrix Materials (TMM).

Introduction

The advancement of Organic Light Emitting Diode (OLED) technology has significantly transformed the landscape of modern display and lighting applications. As demands for higher performance grow, the ability to achieve rapid charging and discharging of pixels has become crucial for optimizing device performance. However, the accumulation of charge carriers within the device can lead to adverse effects, including afterglow and charge leakage, which compromise the overall efficiency, color gamut, and longevity of OLED panels. These accumulation phenomena are reflected in the capacitance-voltage curves, providing vital insights into the charge dynamics within the device.

To better understand these dynamics, capacitance can be measured using dielectric spectroscopy and simulated through a drift-diffusion Poisson equation solver, coupled with a parameterized model of the OLED stack. This approach offers a comprehensive view of charge carrier behavior across various voltage conditions. Recent advancements in simulation software, particularly those that incorporate layer polarities[1], have proven essential for accurately reproducing experimental data. It is also important to note that systematically studying parameter dependence experimentally is challenging, as synthesizing a new molecule or derivative typically alters multiple parameters simultaneously. In contrast, simulations provide a means to change parameters systematically and independently, allowing for insights into their impact on performance characteristics.

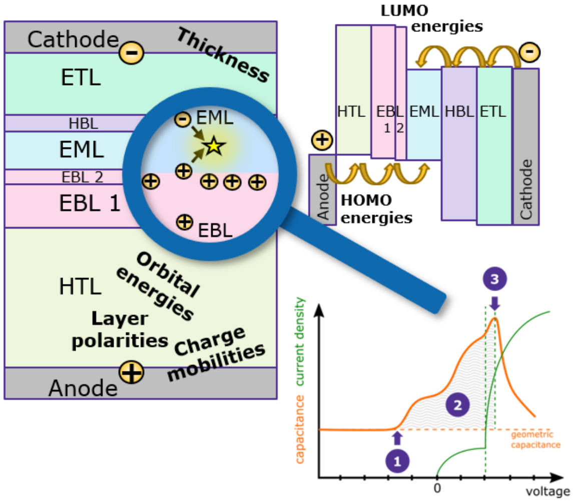

Figure 1 Drift-diffusion equations are solved for a parametrized OLED stack model with a double EBL setup. Obtained capacitance curves are characterized by (1) a C(V) onset voltage, (2) the area under C(V), and (3) the capacitance maximum C_{max}.

Our ongoing investigations leverage such simulation tools to explore the parametric dependence in modern OLED stack architectures, specifically those employing a double electron-blocking-layer (EBL) configuration, as illustrated in Figure 1. Here, the first EBL (EBL1) is separated from the emissive layer (EML) by an additional layer (EBL2) with a thickness of a few nanometers. Such a setup has demonstrated advantages in terms of driving voltage and device lifetime (see Figure 2). This study aims to further investigate the capacitance behavior of these innovative architectures, providing insights into their performance characteristics.

Method: Drift-Diffusion Simulations

The simulations for this study were conducted using SETFOS[2] version 5.3, developed by Fluxim AG. This software employs a well-established one-dimensional drift-diffusion formalism, which integrates the continuity equations for electrons and holes with the Poisson equation to model charge transport and accumulation in OLED devices. Capacitance-voltage characteristics are calculated via SETFOS' impedance module. The simulation framework allows for the inclusion of various material properties, including the effects of spontaneous orientation polarization (SOP) in polar materials, which significantly influence the electrical potential landscape within

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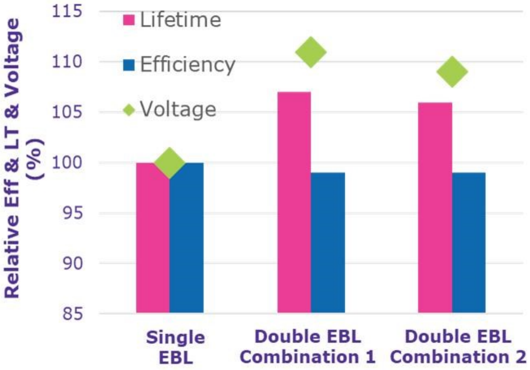

Figure 3 Improvement of Voltage (note that a higher relative value indicates a lower Voltage) and Lifetime at high-level Efficiency of a double EBL setup compared to a single EBL stack.

the device[3,4]. The most crucial material parameters for the OLED stack setup, illustrated in Figure 1, include the orbital energies of the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO), particularly the energy differences at layer interfaces, as well as charge carrier mobilities and layer polarities. These essential factors can be determined experimentally from the layer materials in solution or as neat films. Layer polarities arise from the ability of polar materials to arrange themselves with a preferred orientation within the layer morphology during vapor deposition[4] and depend on the processing conditions[5,6]. While molecular dipoles within the layer tend to cancel each other out, at the layer interfaces, the net partial charges remain uncompensated, resulting in an effective background field for the charge carriers. This property is reflected in the material polarity factor (MPF), where a negative (positive) MPF indicates a net negative (positive) partial charge at a layer's hole-injection side. Note that polarities of adjacent layers can therefore compensate (both MPFs have the same sign) or enhance (opposite signs) each other.

The model chosen for this work is based on a charge-balanced phosphorescent green OLED device employing a double electron-blocking-layer setup, which has shown promising advantages in terms of driving voltage and device lifetime (see Figure 2). By incorporating these parameters, we aim to accurately simulate the capacitance behavior of the OLED architecture under various voltage conditions.

Results

The first set of results, illustrated in Figure 3, examines the impact of varying parameters of the emissive layer (EML) on the capacitance-voltage characteristics (C(V)) of a typical state-of-the-art charge-balanced OLED device. The reference curve (left panel) demonstrates a characteristic late onset voltage for capacitance, with no distinct plateaus and a steep decay occurring just before the current onset voltage, indicating the point at which current density begins to rise significantly.

Subsequent panels in the figure highlight the effects of changing the EML HOMO energy level (middle panel, a darker/brighter shade indicates an orbital energy of +/-0.1 eV) and varying the hole mobility by a factor of 5 (right panel), indicated by red (reduced h mobility) and green (increased h mobility) curves. The results reveal only a minor impact on the capacitance curve under the typical operating conditions of the device suggesting that, within the explored parameter range, the C(V) characteristics are relatively robust to energy and mobility changes within the EML.

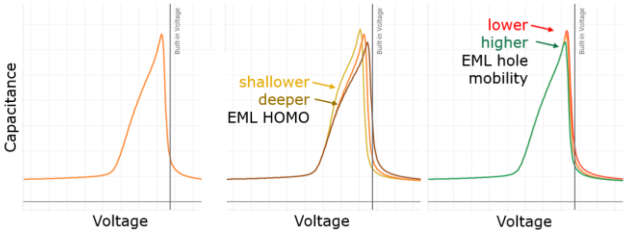

Figure 2 The Capacitance-Voltage (C(V)) characteristics of a typical OLED stack (left panel) only weakly depends on the HOMO energy (middle panel) and the hole mobility (right panel) within the emissive layer (EML).

However, under these conditions, the layer polarities – and particularly their combinations – are found to alter the shape of the capacitance curves significantly. Figure 4 provides a comprehensive analysis of C(V) characteristics in relation to the MPFs of the EML (colors) and the electron blocking layers, EBL1 (columns) and EBL2 (color shades). In the top row, the pure-color curves (also used in the lower panels) represent the reference condition with a vanishing EBL2 MPF, i.e. for a non-polar or fully isotropic material, while the shaded curves indicate the effects of different EBL2 MPFs. The lower panels quantify trends in the C(V) onset voltage, the area under the capacitance-voltage curve, and the maximum capacitance (C_{max}) in dependence of the EBL2 MPF as indicated in Figure 1.

Starting in the upper left panel, which corresponds to a negative EBL1 MPF, we observe a significant impact of the EML MPF on the capacitance-voltage (C(V)) characteristics. Specifically, the C(V) onset shifts towards higher voltages as the EML MPF becomes less negative and even positive (as indicated by the arrow in the figure), while C_{max} decreases correspondingly. It is important to note that the "EML MPF" here reflects an effective layer polarity resulting from the combination of host materials and the green dopant. The negative EBL1 MPF apparently leads to charge accumulation at both the hole transport layer (HTL)-EBL1 interface and the EBL2-EML interface. In the middle panel, with a vanishing EBL1 MPF, similar C(V) onset values are observed; however, C_{max} is lower, indicating that charge accumulation at the HTL-EBL1 interface is present while accumulation at the EBL2-EML interface is suppressed. The most pronounced changes occur when the EBL1 MPF turns positive. In this scenario, the polarity creates a barrier that prevents holes from reaching the HTL-EBL1 interface (and subsequent interfaces) approximately until the applied voltage exceeds the built-in voltage. Consequently, the C(V) onset voltage shifts to higher values, and C_{max} typically decreases significantly, as charge carriers only begin to enter the device once the voltage is sufficiently high for current to flow. Additionally, the sensitivity of the C(V) curve to the EML MPF becomes considerably weaker. This potential barrier configuration introduces a trade-off, as it

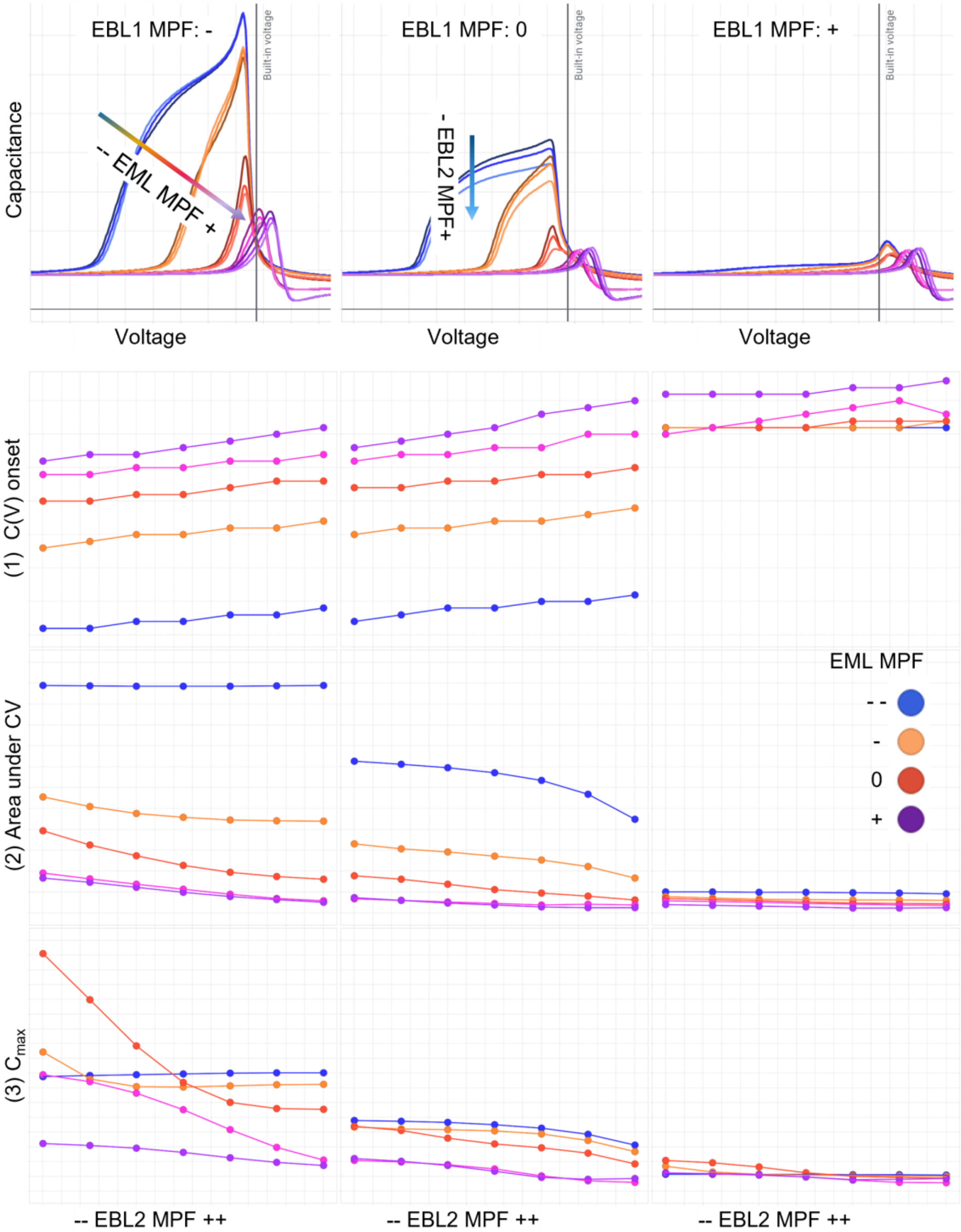

Figure 4 Capacitance curves strongly depend on the combination of Material Polarity Factors (MPFs) of the EML (colors), the EBL1 (columns), and EBL2 (shades in the top row panels, x-axis in the bottom panels for clarity).

increases the driving voltage required for the device to operate effectively.

The lower panels of Figure 4 illustrate the impact of the EBL2 MPF on the C(V) onset voltage (second row), on the area under the C(V) curve (third row) and on C_{max} (bottom panels). The results indicate that the MPF of the thinnest layer, EBL2, plays a relatively minor role overall; however, it can effectively tune the C(V) curves by modulating their shapes and exerting a weak influence on the C(V) onset voltage. Notably, the EBL2 MPF demonstrates its greatest impact onto the C(V) curves in certain scenarios when either the EBL1 MPF is vanishing (middle column, see arrow in top panel) or when the EML MPF vanishes (red curves, see, for example, bottom left panel), suggesting that the interplay between these layers is critical for optimizing device performance.

Conclusion

In summary, the simulations conducted in this study have facilitated a systematic investigation of parameter dependence, highlighting the significant role that the material polarity factor (MPF) plays in determining capacitance characteristics within OLED devices. Our findings indicate that the MPFs of the electron blocking layer 1 (EBL1) and the emissive layer (EML) are particularly influential, whereas the MPF of the thinner EBL2 layer is typically of minor importance but may have significant impact in certain scenarios.

The overall capacitance behavior and the effects of individual material MPFs are strongly contingent upon the interplay between the various layers in the OLED stack. Consequently, the challenge in stack design extends beyond merely identifying the optimal material for each layer—be it for charge transport, blocking, or recombination and emission—to finding the most effective combinations of materials across different layers. This approach aims to maximize multiple performance parameters while controlling the charging and discharging behavior to meet the diverse needs and requirements of various panel manufacturers. Our extensive material portfolio of transport and host materials provides a valuable resource for selecting the most promising combinations, enabling the fine-tuning of device performance to achieve desired operational characteristics.

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