**Paper 62-1** has been designated as a Distinguished Paper at Display Week 2025. The full-length version of this paper appears in a Special Section of the *Journal of the Society for Information Display (JSID)* devoted to Display Week 2025 Distinguished Papers. This Special Section will be freely accessible until December 31, 2025 via:

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**https://doi.org/10.1002/jsid.2059**

# Normally Off Top-Gate Self-Aligned Field-Effect Transistor Using Crystal $InO_x$ with Field-Effect Mobility of Around 100 $cm^2/Vs$

*Yukinori Shima*, Norihiko Seo*, Masami Jincho*, Chieko Misawa*, Marie Matsumoto*, Masahiro Watanabe*, Kayo Kumakura*, Yasutaka Nakazawa*, Junichi Koezuka*, Motoharu Saito**, Koji Kusunoki**, Satoshi Seo**, and Shunpei Yamazaki***

***Semiconductor Energy Laboratory Co., Ltd., Tochigi, Japan**
****Semiconductor Energy Laboratory Co., Ltd., Kanagawa, Japan**

## Abstract

***In this study, we designed and fabricated a crystal $InO_x$-based transistor on a 3.5th generation glass (600 mm × 720 mm) substrate line. The transistor exhibits high field-effect mobility around 100 $m^2/Vs$, an on-state current higher than that of a low-temperature polysilicon-based transistor, normally-off characteristics, and high reliability. By combining our organic light-emitting diode (OLED) patterning technology, we obtained an 8K4K OLED display with high luminance and low power consumption.***

## Author Keywords

Oxide semiconductor; Crystal IO; High mobility

## 1. Introduction

Recently, oxide semiconductors (OSs) have gained widespread applications in display backplanes. In particular, the low-temperature polycrystalline oxide (LTPO) backplane [1, 2], which combines the high mobility of low-temperature polysilicon (LTPS) and the low off-state current of OS, has become the mainstream of smartphones that require narrow bezels and low power consumption. In addition, there is an increasing demand for displays with higher resolution, higher luminance, higher frame rates, narrower bezels, lower power consumption, and lower costs in augmented/virtual reality and other applications. High-mobility OS materials have attracted attention as potential candidates for display backplane technology that fulfill the demand and have been studied by various groups.

Because of the high mobility (approximately 100 $cm^2/Vs$) of crystal $InO_x$ (crystal IO), we have fabricated field-effect transistors (FETs) with crystal IO active layers by applying our technology that has been cultivated through the research and development of display backplanes using crystalline OSs [3–9]. We have also conducted empirical studies to understand the high field-effect mobility of approximately 100 $cm^2/Vs$. In this study, we investigated the high mobility of crystal IO. We fabricated on a 3.5th generation (G3.5) glass substrate line a prototype 8K4K organic light-emitting diode (OLED) display with a crystal IO-based FET on the display backplane. Owing to the high on-state current of the crystal IO FET, the developed OLED display exhibits high luminance.

Many high-mobility OS materials, such as In-rich indium gallium zinc oxide (IGZO), indium gallium oxide (IGO), and IGO:H, have been reported [10–14]. Furuta et al. reported FETs with high field-effect mobility using polycrystalline $InO_x$:H, which was obtained by adding hydrogen during sputtering, as the active layers [15–17]. The FETs including high-mobility OS materials as the active layers exhibit high field-effect mobility; however, they exhibit negative threshold voltage ($V_{th}$), i.e., normally-on characteristics, and suffer gate-bias temperature (GBT) reliability. Furthermore, many reported FETs have a large channel length ($L$) of several tens of micrometers. To apply high-mobility OS materials to backplanes in next-generation high-resolution displays, FETs with an ease of fabrication on a glass substrate, short $L$, normally-off characteristics, and field-effect mobility and reliability as high as those of LTPS-based FETs must be achieved. In OS-based display backplanes, planar top-gate self-aligned (TGSA) FETs are mainly used. To obtain a TGSA FET with normally-off characteristics and high field-effect mobility, an intrinsic channel region and n-type source and drain (S/D) regions must be formed. In general, high-mobility OS materials easily become n-type; thus, process adjustment is required. Insufficient process adjustment results in overestimation of the field-effect mobility and poor reliability.

## 2. Fabrication of crystal IO

Figure. 1 shows annealing temperature dependence of Hall effect mobility of $InO_x$ formed with $H_2$ addition ($InO_x$:H) using a sputtering apparatus for G3.5 glass substrates and electron backscatter diffraction (EBSD) evaluation result of the InO*x*:H annealed at 350°C. Consistent with previous results, InO*x*:H is polycrystallized by annealing at approximately 200°C and has a high Hall effect mobility of approximately 100 $cm^2/Vs$. The graph also shows that the carrier density was low at annealing temperatures of 300°C or higher, which is probably because of a decrease in oxygen vacancies caused by further polycrystallization.

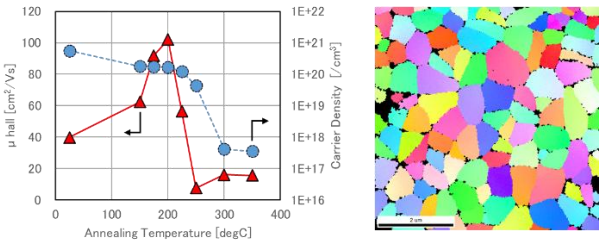


**Figure 1.** Hall effect mobility and EBSD results of $InO_x$:H. (Hall Effect: ResiTest8400, EBSD: JSM-7001F)

The Hall effect mobilities of IGZO and other OSs depend on their carrier densities [12, 16]. Figure 2 shows the carrier density dependence of the Hall effect mobility of the synthesized crystal IO. The carrier mobility of crystal IO varied with the carrier density. In actual FETs, carriers with approximately $1 \times 10^{19}$ $cm^3$ are induced by applying a gate bias voltage. Therefore, FETs with a crystal IO active layer would exhibit high field-effect mobility.


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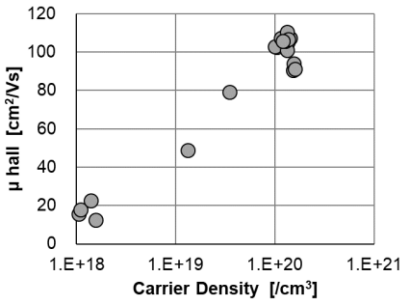


**Figure 2.** Hall effect mobility of crystal IO.
(Hall Effect: ResiTest8400)

To understand the reason for the high mobility of crystal IO, we examined the influence of grain boundary scattering on crystal IO. Figure 3 shows the temperature dependence of the Hall effect mobility of crystal IO and the estimated barrier height of the grain boundaries obtained using a Kelvin probe force microscope (KFM). The temperature dependence of the carrier mobility was fitted with a grain boundary scattering model [18]. The activation energy of crystal IO was approximately 20 meV. The barrier height of the grain boundaries in crystal IO was approximately 42 meV, as estimated from the KFM results. These two values (20 meV and 42 meV) are smaller than 60–80 meV, the barrier height of grain boundaries in LTPS [19], indicating that crystal IO is less susceptible to grain boundary scattering than LTPS, which may be a reason for the high mobility.

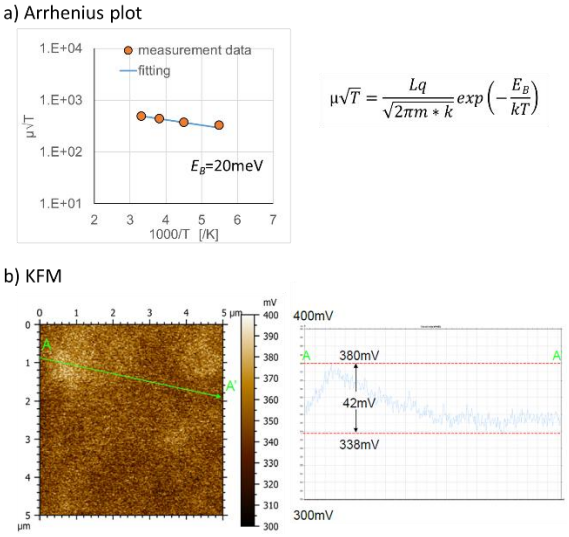


**Figure 3.** Arrhenius plot and KFM image of crystal IO.
(Hall Effect: ResiTest8400, KFM: AFM5000II)

## 3. Fabrication of the TGSA FET

Figure 4 shows a schematic of prototype TGSA FETs. A dual-gate FET and a single-gate FET were separately formed on a G3.5 glass substrate. A back-gate electrode was formed by sputtering and then patterned, after which a buffer layer was deposited via plasma-enhanced chemical vapor deposition (PECVD). Next, $InO_x$:H was deposited by sputtering and then patterned. Wet etching was performed with an oxalic acid solution. After that, annealing was performed so that the $InO_x$:H became polycrystalline. Next, a gate insulator (GI) was deposited on the $InO_x$:H by PECVD. A top gate electrode was then deposited on the GI via sputtering and patterned, after which a passivation layer was deposited by PECVD. Contact holes reaching the crystal IO were formed by dry etching, and extraction electrodes, i.e., S/D electrodes, were deposited by sputtering and patterned. A resin interlayer was also deposited and annealed. In general, the major challenge in obtaining OS FETs with normally-off characteristics is reducing the carrier density in the channel region by adjusting the PECVD conditions.

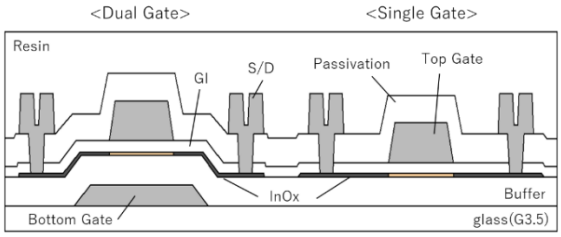


**Figure 4.** Schematic of TGSA FETs.

## 4. Electrical characteristics of the TGSA FETs

Figure 5 shows the micrograph and drain current–gate voltage ($I_d$–$V_g$) curves of the fabricated TGSA FETs with $L$ = 6 μm and channel width ($W$) = 3 μm. The TGSA crystal IO-based FET exhibited normally-off characteristics and a high field-effect mobility of 92.4 cm²/Vs, which is approximately 7 times higher than that of the conventional FET with In:Ga:Zn = 1:1:1 (IGZO(111)).

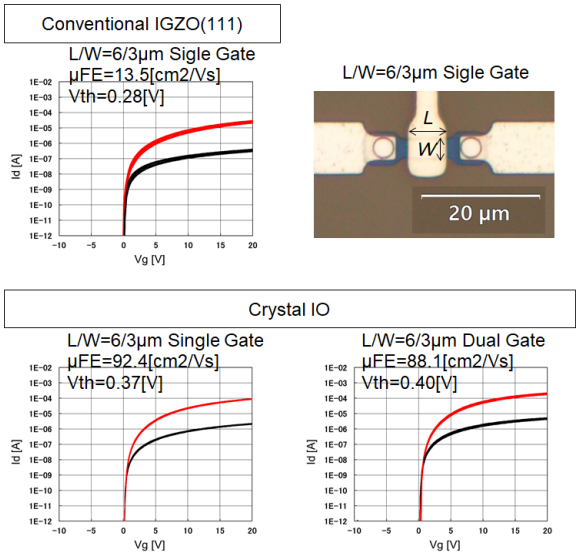


**Figure 5.** Micrograph and $I_d$–$V_g$ curves of the TGSA FETs.
($V_g$ = -10 V to +20 V; $V_d$ = 0.1 V (black line), 5.1 V (red line); $n$ = 20 on G3.5 glass; average values are shown; the mobility of the dual-gate FET was calculated from the composite capacitance of the top GI and the buffer)

Figure 6(a) shows the $L$ dependence of the field-effect mobility and $V_{th}$ in the single-gate FET. Figure 6(b) shows the carrier density distribution in an FET with $L$ = 6 μm, as visualized by scanning capacitance microscopy (SCM) [20]. Normally-off characteristics and field-effect mobilities of 90 cm²/Vs or higher

were recorded for different $L$ values, and the $n^+$-type regions barely extend under the gate. These results indicate that the field-effect mobility of 90 $cm^2$/Vs recorded for the fabricated FET is not overestimated due to a reduction in effective $L$ and that the external resistance, particularly the resistance of the $n^+$-type layers serving as the S/D regions, is significantly lower than the channel resistance. In other words, in the proposed TGSA crystal IO-based FET, the channel region with a low carrier density and the S/D regions with a high carrier density are sharply separated.

As shown in Fig. 1, the synthesized crystal IO exhibits a grain size of at most approximately 1 µm. When $L$ increases from 6 to 50 µm, the number of grain boundaries across which carriers flow in the channel direction is estimated to be nearly 10 times larger. However, as shown in Fig. 6(a), the field-effect mobility hardly decreases with increasing $L$. This result confirms that crystal IO is less susceptible to grain boundary scattering, as shown in Fig. 3.

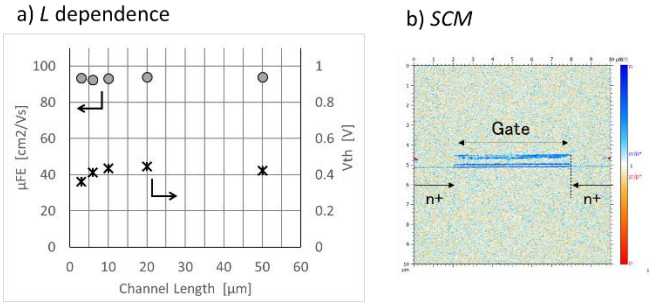


**Figure 6.** (a) $L$ dependence of field-effect mobility and $V_{th}$ in the single-gate TGSA FET and (b) SCM image of the FET.

Figure 7 compares the on-state current of the TGSA crystal IO-based FETs with that of TGSA OS-based and LTPS-based FETs used in commercial products. The proposed TGSA crystal IO-based FETs achieved on-state currents equivalent to or higher than those of the LTPS-based FETs, indicating that the proposed TGSA FETs are promising candidates for various driver circuits.

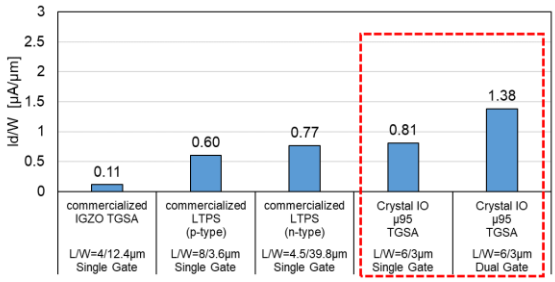


**Figure 7.** Comparison of the on-state currents of LTPS FETs and crystal IO FETs.

(Drain voltage $V_d$ = 0.1 V; $V_g$ = 20 V; normalized with $W$)

For applications in display backplanes, the GBT stress resistance of FETs is vital. Figure 8 shows the positive-bias temperature stress (PBTS) and negative-bias temperature illumination stress (NBTIS) of the fabricated dual-gate TGSA crystal IO FET. The FET exhibited excellent stability, as indicated by the $V_{th}$ shift at 60°C with a gate–source voltage ($V_{gs}$) of ±20 V for 6 h. Therefore, the proposed TGSA FET is suitable for driver and pixel circuits.

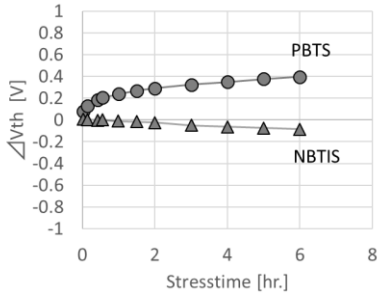


**Figure 8.** GBT stress of the dual-gate TGSA crystal IO FET.

($V_{gs}$: ±20 V; dark environment at 5,000 lx; temperature: 60°C; time: 6 h)

## 5. OLED display based on a TGSA crystal IO FET

A prototype 8K4K OLED display was fabricated using a TGSA crystal IO FET on a backplane. For colorization, we used metal maskless lithography (MML), an OLED patterning technology developed by our group. Table 1 summarizes the specifications of the prototype display, and Fig. 9 shows the illuminated display.

**Table 1.** Specifications of the developed OLED display

| | Specifications |
|---|---|
| Screen diagonal | 8.3 inch |
| Backplane | Crystal IO |
| Resolution | 7,680 × RGB × 4,320 (8K4K) |
| Pixel density | 1,058 ppi |
| Pixel size | 24 µm × 24 µm |
| Pixel arrangement | RGB stripe |
| Pixel circuit | 2Tr + 1C / pixel |
| Aperture ratio | 22.3% |
| Coloring method | RGB side-by-side patterning (MML) |
| Emission type | Top emission |
| Source driver | Chip on panel |
| Scan driver | Integrated |

**Figure 9.** OLED display based on crystal IO.

We compared the prototype display with a crystal IO FET and that with an IGZO FET. The two displays were fabricated using the same mask. As shown in Fig. 7, the crystal IO FET exhibited an on-state current approximately 8 times higher than that of the

IGZO FET. The on-state current is also higher than that of the LTPS FET. The voltage amplitude used in the gate driver of the crystal IO FET could be reduced to 82% of that of the IGZO FET. The driving frequency of the gate driver in the prototype display was high. Generally, smartphones and other devices require high frame frequencies of approximately 120 Hz. Because the dynamic power of a gate driver is proportional to the square of the voltage, a smaller voltage amplitude results in lower power consumption.

Owing to the high on-state current of the crystal IO FET, the display exhibited a high luminance of 785 cd/m$^2$ (with a white box filling 10% of the display), whereas the IGZO FET-based display exhibited a luminance of 640 cd/m$^2$.

Furthermore, owing to its high on-state current, the proposed crystal IO FET fabricated using the mask we have developed can reduce the buffer size of the gate driver by 55%. The buffer area, which covers most of the layout area of the gate driver, must be sufficiently large to charge a load that depends on the number of pixels. However, it can be small if its ability to transmit current, to which the power required for charging is proportional, is sufficiently high. Therefore, the crystal IO FET, which exhibited a higher on-state current than the LTPS FET, is more effective for narrowing the bezel.

These results demonstrate that using the proposed crystal IO FET, displays with narrow bezels, high luminance, and low power consumption can be fabricated.

## 6. Conclusion

In this study, we developed a TGSA FET with a crystal IO active layer. Using a facility for G3.5 glass substrates, normally-off characteristics and an extremely high field-effect mobility of 92.4 cm$^2$/Vs were obtained. Furthermore, we fabricated a prototype OLED display with TGSA FETs in the pixel and driver circuits. The OLED display outperformed the IGZO FET-based display. Crystal IO used in the display backplane has the potential for high luminance and low power consumption. This study shows that crystal IO is not only a promising replacement for LTPO in backplanes but also has high application potential in larger glass substrate lines.

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