Contact-Controlled Transistors as Sufficiently Fast Switches for Active-Matrix Pixel Circuits

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Abstract

Contact-controlled transistors (CCTs), such as source-gated transistors and multimodal transistors, can operate surprisingly effectively as switches in active-matrix display pixels, despite deliberately engineered source energy barriers. TCAD simulations of LTPS devices show that barrier optimization and driving in the triode region allow CCTs for use as effective switches. Additional desirable characteristics (low off-state current, low saturation voltage) recommend CCTs as highly advantageous for pixel circuits.

Author Keywords

Active matrix; pixel circuit; multimodal transistor; source-gated transistor; contact-controlled transistor; Schottky contact; LTPS; switching transistor.

1. Objectives and Background

Contact-controlled transistors (CCTs), such as source-gated transistors (SGTs) (1–5) and multimodal transistors (MMTs) (6–8), have several advantages over Ohmic-contact thin-film transistors (TFTs), with the implementation trade-off of introducing at least one additional step in the process (i.e. to ensure a rectifying source contact). To date, CCTs have been used as a pixel driver (3,4,9,10) because of their wide dynamic range, low saturation voltage V_{DSAT}, and low output conductance g_d. Despite the deliberate use of source energy barriers, there is little reason for concern about the level of on-current, since, depending on emitter technology, CCTs can be driven in saturation from low V_{DS} even at higher gate-source voltages V_{GS}. There is no penalty for the power-efficiency, as the low V_{DSAT} of the drive transistor allows a lower supply rail voltage V_{DD} (3,7) to be used. In addition, the MMT has advanced functionality enabling simplification of circuits with further benefit (7,8).

However, the fact remains that when considered for use as a switch, a CCT may appear to be unfavourable because the presence of the source energy barrier is equated to a significantly lower on-current. Yet, this might not be the case. Here, we show that when designed and used appropriately, SGTs and MMTs are capable of providing performance comparable to TFTs for use as an on-switch in display circuits. Coupled with their superior off-state performance (11), this could truly be a breakthrough for future low-complexity, yet powerful, backplane technologies. This is especially relevant for LTPS, in which striking the balance between the on- and off- current of the relevant TFTs, within the pixel circuit, has been a challenge for decades, in spite of numerous device and circuit techniques to alleviate the off-state leakage (12–18).

Using Silvaco TCAD, we outline design considerations for low-temperature polycrystalline Si (LTPS) CCTs, by way of example with use of the MMT, and demonstrate performance in a simple 1T1C switch with storage capacitor circuit, relevant to the vast majority of active-matrix pixel designs. We explore capacitor charge and discharge timing, contrasting conventional Ohmic-contact TFT and CCT performance. Since CCTs can be implemented in a variety of technologies, the principles apply to other material systems, including *p*-type LTPS, IGZO, and organic semiconductors.

2. Methods

In order to reflect realistic behavior of LTPS TFTs (Fig. 1a) and MMTs (Fig. 1b), devices were simulated using previously verified materials and models with Silvaco Atlas v5.28.1.R (2,11,13). Default parameters for *n*-channel polysilicon were used, with relevant device and materials parameters as per Table I. The off-state leakage behavior included Shockley Read Hall, band-to-band and phonon assisted tunneling models as verified in (13). Selberherr's impact ionization was also included to account for the kink effect (19). Aside from varying the work function (*WF*) of the contacts, *n*-type doping $2.3{\cdot}10^{19}$ cm^{-3} was included under both source and drain for the Ohmic-contact TFT, along with 1 µm *n*-type gate overlap low drain doping (LDD) of $4.6{\cdot}10^{19}$ cm^{-3} as per (13) to mitigate off-state carrier generation. Unlike previously reported LTPS contact-controlled devices (2,11,20), no field relief structures were implemented in the architectures presented here. Cutlines for electron concentration and potential were taken in the accumulation layer 1 nm from the CG1 insulator/ semiconductor interface. Electrical characteristics are shown in Fig. 2. Potential and electron concentration cutlines are found in Fig. 3. The simulated transistor width was 1 µm.

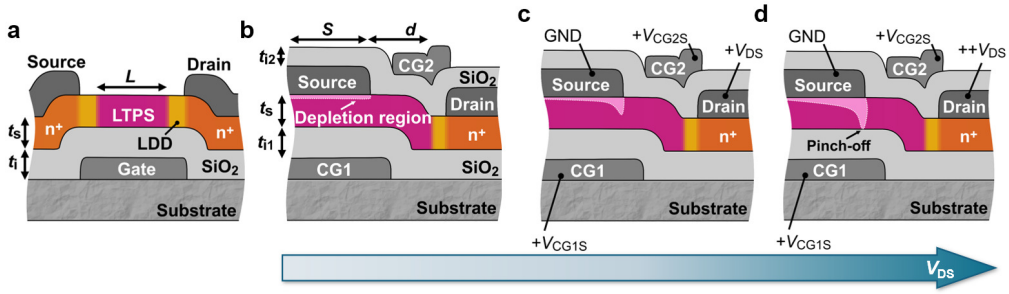

Figure 1. Schematic cross-section of simulated: a) TFT; b) MMT with current control gate (CG1) and channel switching control gate (CG2), along with a depletion region that forms due to the source energy barrier; c) MMT under low V_{DS} which reverse biases the energy barrier. d) Higher V_{DS} pinches-off at the source edge and drain current saturates.

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For a functional circuit use-case demonstration, Silvaco Mixed-Mode was used to simulate charging and discharging of a capacitor C1 = 0.3 pF, connected to either a TFT or a MMT as a switch (Fig. 4). The MMT's source contact work function *WF* was also varied to ascertain an appropriate barrier height that would allow high enough on-current for a switch, while maintaining behavior required for a drive transistor. Simulated transistor width, as implemented in the circuits, was 3 µm.

Table 1. Principal design parameters of simulated transistors

Parameter	MMT	TFT
Contact work function, *WF*	4.17, 4.37, 4.42, 4.47, 4.52, 4.57, 4.62 eV	4.17 eV
SiO_2 permittivity, ε_i	3.9	
Gate insulator thickness, t_{i1}, t_{i2}, t_i	100, 60 nm	60 nm
LTPS thickness, t_s	30 nm	
LTPS electron, hole mobility	300, 30 $cm^2V^{-1}s^{-1}$	
Source-CG1 overlap, *S*	2 µm	-
Source-drain separation, *L* or *d*	3 µm	

3. Results and Discussion

The present study represents a plausible starting point in terms of device sizing and construction, in the context of usual LTPS active-matrix emissive pixel designs. In practice, many additional considerations, such as threshold voltage V_{th} compensation and driving timing will play a role in the performance of the circuit. In all cases, charging and discharging the storage capacitor in a short time interval is a requirement. We will show that, contrary to conventional intuition, CCTs (with their desirable off-current characteristics) can be excellent candidates as switching devices, even in terms of on-current performance.

Transistor Operation: The reference device is an Ohmic-contact LTPS TFT (Fig. 1a). Its transfer (Fig. 2a) and output (Fig. 2b) characteristics reflect the expected behavior (13), with the exception of a deviation in the off-current around V_{GS} = -7.5 V, likely due to difficulties with numerical convergence. At V_{GS} = -5 V, drain current I_D = 633 fA. In comparison, the MMT's transfer characteristic with current control gate (CG1) as the input parameter (Fig. 2c) is nearly two orders-of-magnitude lower, at 6.05 fA, when the channel region is biased by the switching control gate (CG2) to a sufficiently conductive state. Both CG1 and CG2 are capable of turning the device off, however because CG1 operates in a manner similar to SGTs (6,21), it is able to turn the device off even if the channel is highly accumulated (11). To ensure correct MMT operation, CG2 should have no influence on the drain current magnitude, i.e. the CG2 transfer characteristics (Fig. 2d) should be flat. Excessive CG2 bias can induce more on-current due to carrier generation in the drain region (20). By varying the *WF* of the source contact, it is clear that increasing barrier height results in MMT behavior for lower CG2-source voltages V_{CG2S}. Since MMT charge injection is based on SGT mechanisms, the ability of the source to pinch-off with CG1-source bias will depend on the ability of the drain field to reverse bias the source energy barrier to ensure full depletion of charge carriers under the source edge. Thus, for conditions such as: low but non-negligible source contact barriers, high gate bias, or thick semiconductor layers leading to reduced vertical electric fields, the source edge will only be partially (Fig. 1c), rather than fully (Fig. 1d), depleted. Either of these can be exploited, among other techniques, to deliver higher currents required for the device to operate as a switch. In other words, for biasing conditions for which the source is not fully pinched off, the output characteristic of the MMT (or SGT) follows fairly closely the output characteristic of the similarly sized TFT (3), resulting in comparable on-resistance $R_{DS(on)}$ between the source and drain terminals.

In the interest of manufacturability, the source contact processing for the drive CCT and the switch CCTs should be identical. This implies optimizing for a contact barrier high enough to provide low voltage saturation and low g_d for the driver at low and moderate V_{GS}, and low enough to allow high on-currents at low V_{DS} and high V_{GS}.

The output characteristics in Fig. 2e show a single curve at high CG1 and CG2 bias (i.e. the channel is in an on-state and CG1 controls drain current magnitude). I_D increases with lower source

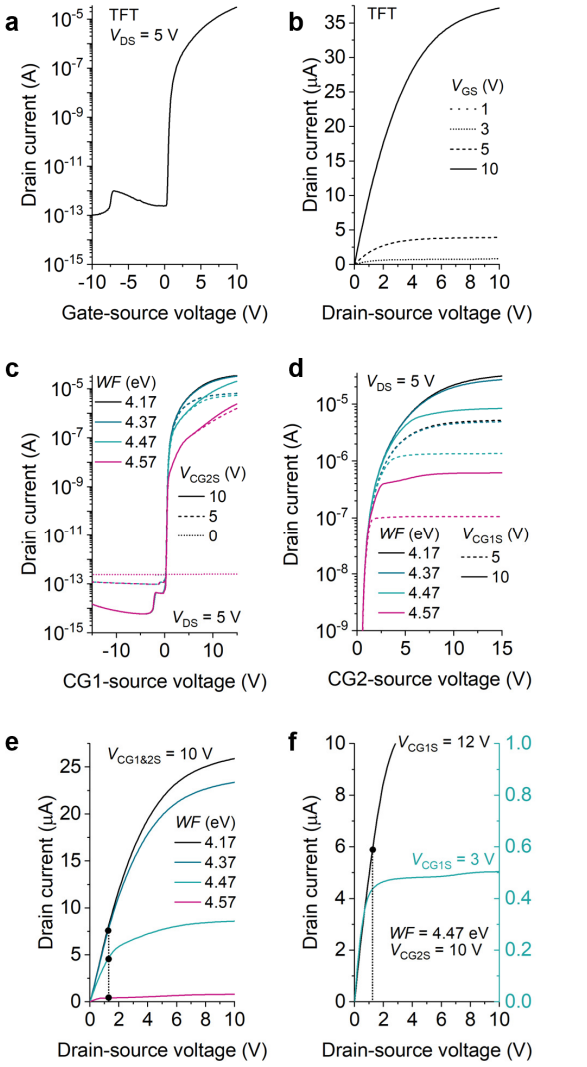

Figure 2. a) Transfer and b) output characteristics for the TFT. c) Source control gate (CG1) transfer characteristics for several source contact work function *WF* and channel gate (CG2) voltage V_{CG2S}. d) Transfer characteristics for CG2 with two values of CG1 bias. MMT behavior is fully achieved when the curve flattens. e) Output characteristics for various *WF*. V_{DS} = 1.25 V indicated. f) Output characteristic behavior at V_{CG1S} = 12 V and 3 V, for switch and drive MMT, respectively.

contact *WF* but is traded-off with low V_{DSAT} and g_d. However, in a practical switch application (Fig. 4a), one assumes that capacitor C1 charges or discharges from/to 0 V and to/from a value given by the magnitude of the DATA voltage. This voltage is comparatively low. From our previous studies (7) and in Fig. 3f, driving reasonably sized AMOLED pixels with currents in the orders of 100s of nA (16) requires at most 3 V for a LTPS drive CCT. In fact, the 1.25 V DATA voltage, considered in the circuit described below, would correspond to a low grey level (<10% of maximum brightness). Hence, from the perspective of the switch, operation is mostly in the triode region (black dots in Fig. 2e and 2f) for the duration of the charge/discharge transient of C1, if V_{DATA} is low compared to V_{SEL} (Fig. 4a). In this regime, the channel resistance dominates and the source contact is not in control of the drain current, shown by the weak source-side pinch-off and the low voltage drop at the edge of the source for *WF* = 4.47 eV in Fig. 3a and 3b, respectively. For this architecture, *WF* = 4.47 eV provides an energy barrier height suitable for higher I_D in the triode regime for switches (~61% of level provided by contact with *WF* = 4.17 eV at V_{CG1S} = 10 V in Fig. 2e at V_{DS} = 1.25 V, and which could be even higher if V_{CG1S} is increased further).Good saturation is seen at low V_{CG1S}, suitable for drive transistors (blue curve in Fig. 2f).

1T1C Circuit Operation: Here, we focus on the on-state performance of the switches. The experiment (Fig. 4) consists of rapidly charging and discharging C1 through transistor T1 and M1, respectively, emulating the transient behavior required in the programming and reset phases of an active-matrix pixel circuit. The gates of MMT M1 are shorted for convenience and, as such, operate in the same manner as SGTs. In practice, optimizations may be made to the driving of CG2 in order to reduce the likelihood of deleterious leakage current via hot-carrier generation (20).

The two transients considered, specifically for charging and discharging C1, are in principle symmetrical when a TFT switch is used, as its source and drain are identical. The small discrepancies are due to the imbalance in parasitic capacitance between the data line and the output voltage VOUT node (Fig. 4a), to which the gate of the drive transistor is connected. The transient response of the TFT circuit is able to track the SEL voltage ramp and will be used as the reference for the MMT circuit's behavior.

For the MMT switch, the situation is more complex, because its source and drain are not symmetrical. Considering whether to connect the source to the DATA or VOUT nodes ultimately depends on the overall function of the circuit. Assuming that in the emission period of an active-matrix pixel circuit, capacitor C1 is charged so that node VOUT is at the desired potential and that the DATA line is grounded, leakage can be minimized by utilizing a CCT switch only if the rectifying contact (indicated by the dot in Fig. 4a) is connected to the lower potential (DATA) (11). With the CCT switch connected in this polarity, we can analyze the resulting transients in Fig 4.

Charging C1 through M1 starts from the condition of node VOUT being at a lower potential than node DATA. Therefore, the electrical source of M1 is represented by its *Ohmic* contact (Fig. 1b) and its electrical drain is its *Schottky* contact (dot in Fig 4a). When select signal SEL is asserted, conventional current flows through M1 from DATA to VOUT. That is to say, electrons are injected across the Ohmic contact. Thus, M1's behavior is practically indistinguishable from that of the equivalent TFT, T1 (Fig. 4c, left), for all but the highest of energy barriers.

The discharging transient (Fig. 4c, right) shows a significant dependence on source contact metal work function, because in this condition, M1's source is indeed the rectifying contact, while the drain is the Ohmic contact. Even in this situation, the moderate energy barrier generated by using the *WF* = 4.47 eV source electrode shows an inconsequential degradation of transient performance, since M1's triode region is sufficiently similar to that of T1's response (Fig. 2e).

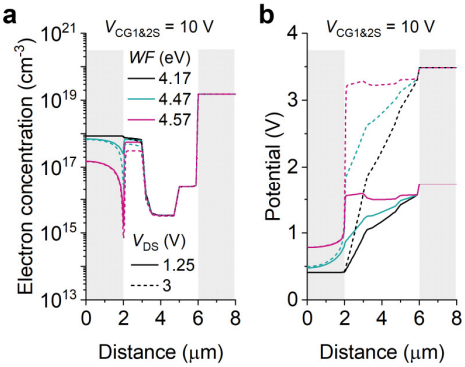

Figure 3. a) Electron concentration and b) potential distributions at the semiconductor-insulator interface for different biasing conditions and source contact *WF*. The source starts at *x* = 0 and ends at *x* = 2 μm.

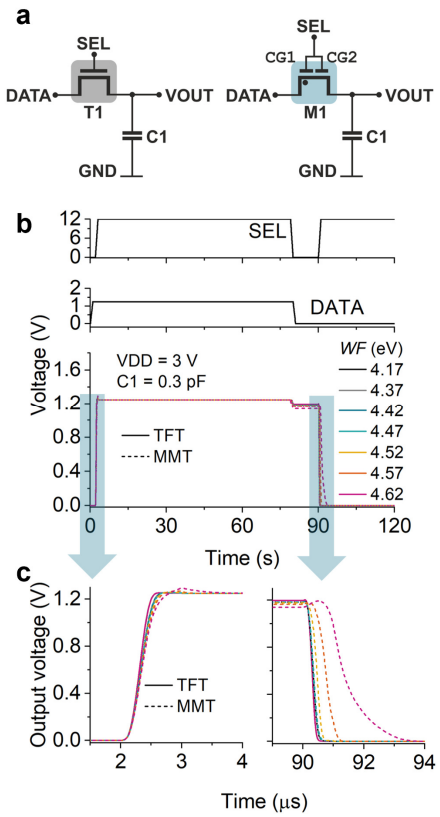

Figure 4. a) circuit schematics with the rectifying contact of the MMT indicated by a dot; b) timing diagrams for the circuits in a); c) detail of the rising and falling transients of the capacitor voltage vs. MMT source contact *WF*.

4. Impact and Outlook

Until now, contact-controlled devices, such as SGTs and MMTs, have been regarded as too slow for certain applications. Due to the source energy barrier, there has been little incentive to explore such devices as switches, which are the fastest part of the pixel array. However, on closer inspection, SGTs and MMTs are capable of delivering the required performance, as long as the energy barrier is suitably designed and they are operated in or close to the triode regime of the output characteristic at drain voltages lower than those required for source-side pinch-off of the channel, i.e. before the contact control takes over.

In conjunction with their superior off-state performance, the SGT or MMT make viable switches. This finding opens a route toward effective implementation of contact-controlled transistors in high performance active-matrix backplanes, both as switches and as drive transistors.

5. Acknowledgements

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