Ultra-Flexible Monolithic Three-Dimensional CMOS Devices and Circuits

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Abstract

This paper reviews advancements in flexible three-dimensional CMOS electronics, focusing on monolithic three-dimensional architecture that integrates vertically stacked carbon nanotube and indium gallium zinc oxide transistors. By utilizing shared gates and drains, and eliminating inter-tier vias, the design enhances routing efficiency, achieves 45% area reduction, and demonstrates exceptional flexibility. Circuits like ring oscillators and SRAMs exemplify high integration and functionality, highlighting their significance for complex flexible electronics.

Author Keywords

Flexible electronics, CMOS, Monolithic three-dimension, ring oscillator, static random-access memories.

1. Introduction

Recent developments in flexible electronics have opened new avenues for applications in wearable technology, intelligent robotics, and human-machine interactions. The integration of complementary metal-oxide semiconductors (CMOS) has notably accelerated the progress of flexible electronics, facilitating the incorporation of intricate functionalities. [1] There is a growing demand for flexible CMOS circuits in sectors such as healthcare, human-machine interfaces, and wearable devices, where these circuits must demonstrate high flexibility, dense integration, and exceptional electrical performance to support complex functionalities.

Flexible thin film transistors (TFTs) are the foundation devices to build up flexible CMOS circuits. To realize flexible CMOS circuits, researchers have proposed various possibilities of transistors.[2] For n-type transistors, amorphous indium gallium zinc oxide (a-IGZO) has gained prominence due to its low off-current characteristics. [3] Meanwhile, carbon nanotubes (CNTs) are recognized for their suitability in p-type transistors due to their inherent softness, excellent electrical properties, and scalability.[4][5] The combination of a-IGZO TFTs and CNT TFTs forms a robust foundation for flexible CMOS electronics.

Existing flexible CMOS circuits utilizing CNT and a-IGZO TFTs predominantly adopted traditional planar architectures, leading to low device density and complex fabrication processes due to material compatibility issues. A previous work adopted three-dimensional structure to achieve inverter, while they fabricated n-type transistor on one PI layer and p-type transistor on the other PI, and then connected the upper and lower devices via shadow mask printing. This induced limitation for both integration and performance. [6]

Monolithic three-dimensional (M3D) architectures, especially at the device level, offer a viable solution to the challenges of chip density, which arise beyond the 22-nm node by improving areal device density and reducing parasitic effects. However, M3D configurations encounter mechanical performance constraints due to inter-tier vias, which are often unable to endure significant mechanical stress during bending, thereby negatively impacting high-density circuits. Furthermore, the gate dielectric layer frequently restricts the development of circuits that necessitate both superior electrical performance and mechanical flexibility, as conventional high-k oxides and organic polymers may either fracture under stress or exhibit insufficient dielectric properties.

In addressing the aforementioned challenges, our recent researches have proposed and implements ultra-flexible M3D CMOS circuits characterized by a high level of integration and performance by vertical stacking CNT transistors and a-IGZO transistors. The design features a configuration, in which each pair of p-type CNT TFT located in the lower layer and n-type a-IGZO TFT in the upper layer share the common gate electrode and the common drain electrode. [7][8] This approach minimizes the need for inter-tier vias, thereby reducing routing complexity, transmission delay, and power consumption. Additionally, it streamlines the fabrication process while enhancing the mechanical performance and robustness of the circuits. A hybrid polyimide-Al_2O_3 (PI-Al_2O_3) layer serves as the gate dielectric for the realization of flexible circuits.[9] Two hybrid PI-Al_2O_3 layers are fabricated to function as dielectrics for the upper and lower TFTs, respectively. A variety of circuits, including inverters, NAND gates, NOR gates, high-stage ring oscillators (ROs), D latch cells and static random-access memories (SRAMs) have been designed and realized based on this platform.

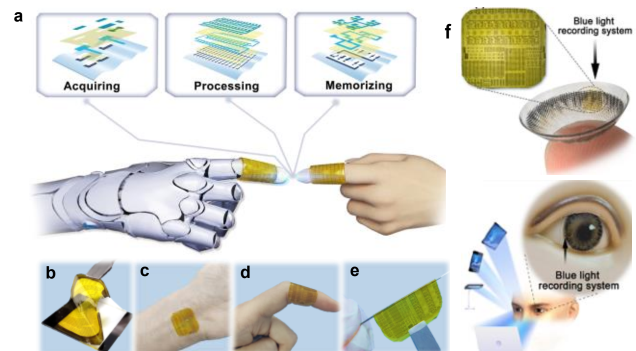

Figure 1. The fabricated flexible electronic systems. a) The fabricated flexible electronic system wound around both robotic and human fingers. Inset: The layout design of circuit blocks of the flexible system in this work, including acquiring, processing, and memorizing modules. b) Peeling of the ultra-flexible circuits. Attaching the circuits onto c) a human wrist, d) a finger, and e) an ultra-thin needle with the bending radius of 250 μm. f) System application for blue-light recording.[7]

2. System, architecture, process, and circuits

(a) The M3D flexible electronic platform and system

Figure 1a depicts a typical flexible electronic system, which are designed to conform to both robotic and human fingers. The system comprises a photonic transistor, a high-stage RO featuring 112 transistors, and a D latch, which are utilized for acquisition, processing, and memory functions, respectively, as illustrated in

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the inset of Figure 1a. The circuit array demonstrates significant mechanical flexibility (Figure 1b) and can be closely adhered to the human wrist, wrapped around a finger, or even applied to an ultra-thin needle, as shown in Figures 1c-e. Figure 1f shows a demonstration of blue-light recording system.

The fundamental component is the inverter consisting of a vertically stacked n-type a-IGZO transistor and a p-type CNT transistor, without the use of inter-tier vias. The structure and schematic representation of the inverter are presented in Figure 2a and 2b, respectively. Figure 2c provides a cross-sectional scanning electron microscopy (SEM) image of the inverter, illustrating the shared common gate and drain electrodes utilized by both the a-IGZO and CNT transistors. This M3D design of the inverter results in a 40% reduction in area, as indicated in Figure 2d. The essential fabrication steps, exemplified by the inverter's production, are outlined in Figure 2e.

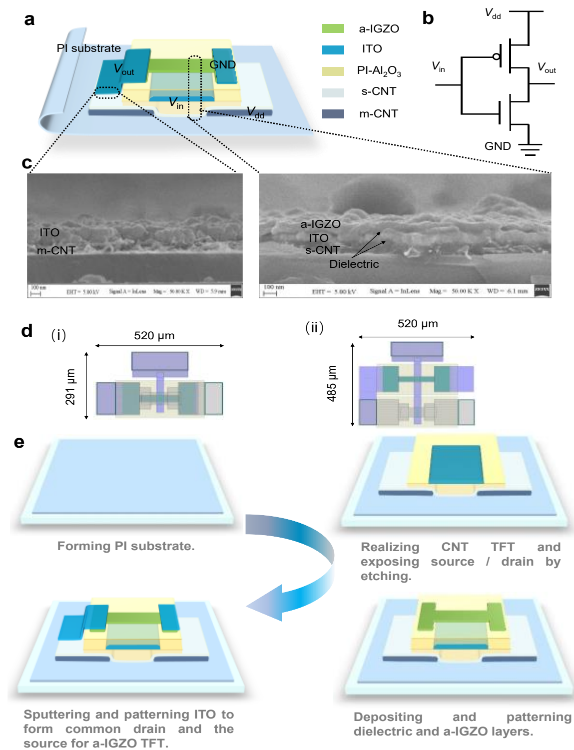

Figure 2. Design and architecture of the proposed inverter. a) Schematic diagram, b) circuit design, and c) SEM image of the inverter based on stacked CNT and a-IGZO TFTs vertically. d) Inverter areas based on (i) M3D and (ii) planar designs. e) Key fabrication process of fabricating the M3D inverter without inter tier via.[7]

(b) Characteristics of M3D CMOS circuits

Inverters: The M3D inverters were systematically characterized, as shown in Figure 3. The voltage transfer characteristics (VTC) at a supply voltage (V_{dd}) of 5 V demonstrate a noise margin of 78.8% at high voltage and 82.0% at low voltage (Figure 3a). The inverters withstand 6000 bending cycles at a 500 μm radius with minimal VTC degradation, indicating significant flexibility (Figure 3b). This flexibility arises from the use of intrinsically flexible components, a thin substrate, and the M3D design. At V_{dd} of 5 V, the inverters achieve a maximum gain of 191, a record for flexible CMOS inverters. They operate effectively across a voltage range of 1 to 11 V (Figure 3c), due to robust dielectric performance.[9] Dynamic working curves with a 12 ms cycle period are illustrated in Figure 3d.

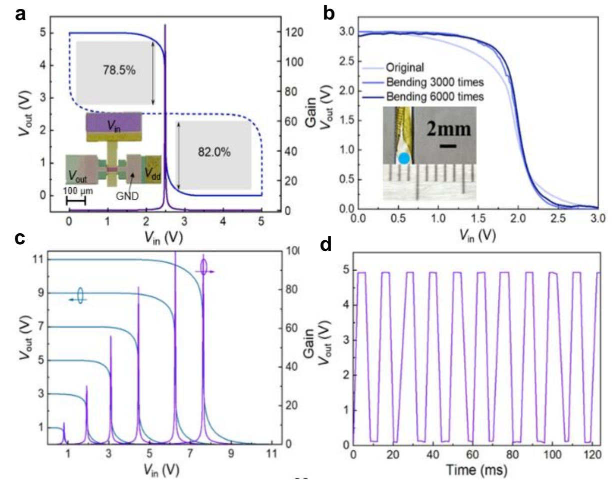

Figure 3. Characteristics of CMOS logic gates. a) Typical VTC of the proposed inverter. Inset: colored microscope image of the CMOS inverter. b) VTC over sequential bending test to curvature radius of 500 μm. Inset: photograph of bending test. c) VTC and gain of the inverter at Vdd ranging from 1 V to 11 V, with step of 2 V. d) Dynamic characteristics of the inverter. [7]

Logic Gates: NAND and NOR gates were also illustrated. Figures 4a-c present microscopic images of a NAND gate and a NOR gate, accompanied by their respective circuit diagrams and operational waveforms. A voltage of 0 V is designated as logic "0", while a voltage of 5 V is designated as logic "1". Both logic circuits exhibit accurate logical operations.

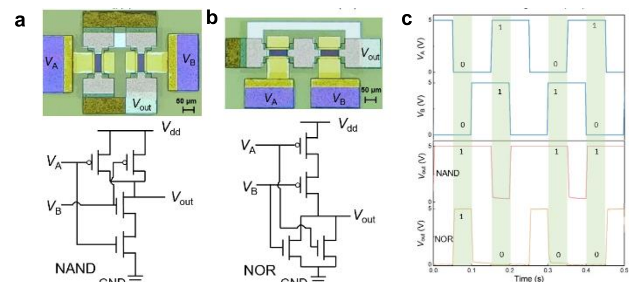

Figure 4. M3D NAND gate and gate. (a) Layout and schematic of NAND. b) Layout and schematic of NOR gate. c) Output waveforms of the NAND and NOR gates. [7]

ROs: ROs with various scale up to 55 stages were realized, and the schematic and photograph are shown in Figure 5a and 5b, respectively. It consists of 112 transistors and occupies an area of 9.56 mm^2, saving the area 45% compared with that by a planar design, showing higher integration density. The highest frequency is obtained from 3-stage RO, which is 312.5 kHz at V_{dd} of 11 V, as shown in Figure 5c. The 55-stage RO produces a square wave with frequency of 547 Hz, as shown in Figure 5d.

The frequency of RO ranging from 3 to 55 stages at V_{dd} of 5 V is displayed in Figure 5e. The lowest delay time is 530 ns with an average delay of 870 ns per stage for all the ROs with different stages. The oscillators can operate at a wide voltage range from 3 V to 11 V and exhibit high yield of the M3D platform. Especially, the 21-stage and 55-stage ROs keep outputting correct waveforms even after being bent at radius of 500 μm for 2000 and 50 cycles, respectively, as shown in Figure 5f and 5g.

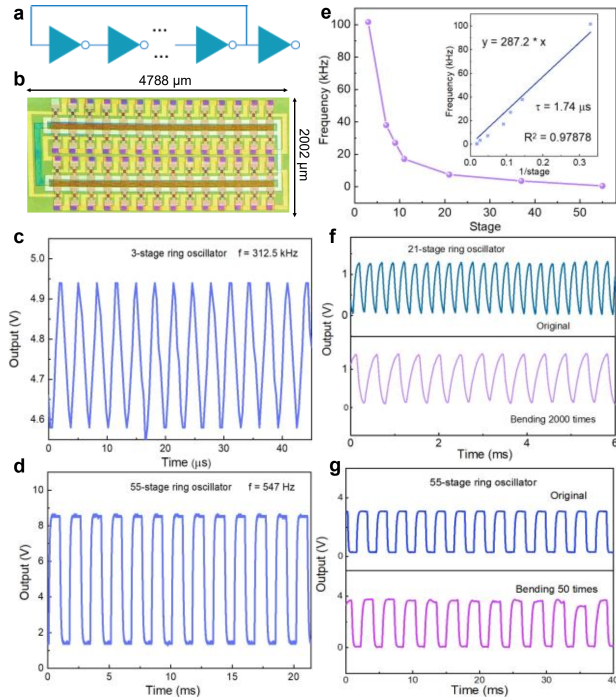

Figure 5. M3D ROs. b) Microscopic photograph of a 55-stage RO. Output waveforms of c) 3-stage and d) 55-stage ROs. e) Frequency characteristics of the oscillators with various stages. Inset: fitting curves of delay time. Output curves of f) 21-stage RO and g) 55-stage one over different bending cycles at curvature radius of 500 μm. [7]

D-latch: Figure 6a and b show the layout and schematic of D latch. For the D latch function, as shown in Figure 6c, output Q follows the input D when clock (CLK) is "1" while it holds the previous logic when the CLK is "0". The data is updated at CLK of "1" and held at CLK of "0", indicating the capability of data storing.

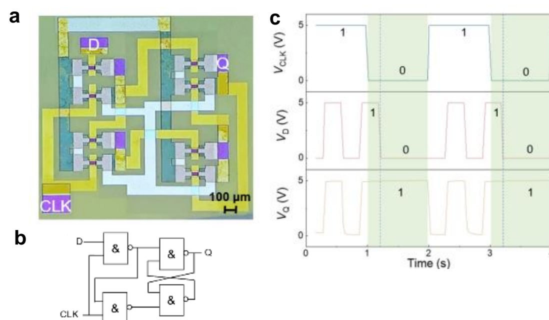

Figure 6. Demonstration of the D latch. a) Microscopic image. b) Circuit diagram. c) Output wave curves. [7]

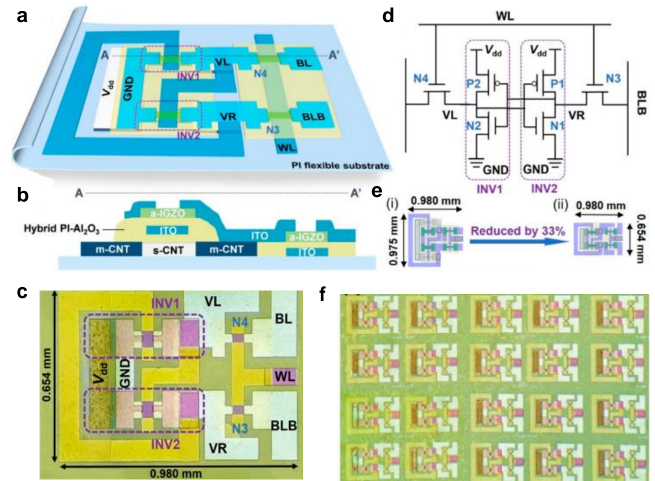

Figure 7. M3D SRAM. (a) Diagram illustration, (b) sectional view, (c) layout, and (d) circuit diagram of the M3D SRAM cell. (e) Layout comparison between (i) planar and (ii) M3D structure of the SRAM cell. (f) Large-scale array of the M3D SRAMs. [8]

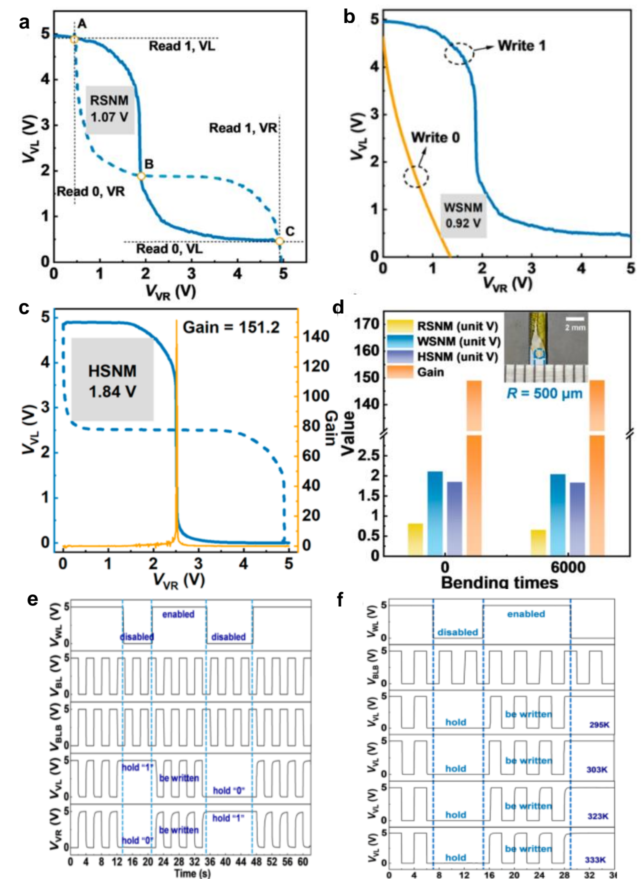

Figure 8. Characteristics of the flexible M3D SRAM. VTCs and extracted static noise margins during a) read and b) write operation. c) VTC and extracted HSNM and gain during hold operation. d) Extracted RSNM, WSNM, HSNM and gain in hold operation of the SRAM under different bending times. Dynamic response of the SRAM e) in write and hold operations, and f) under different temperatures. [8]

SRAM: An ultra-flexible and highly integrated SRAM with enhanced thermal stability has been developed utilizing the M3D CMOS design, as shown in Figure 7. Figure 7a-d show the diagram illustration, sectional view, layout, and circuit schematic of the M3D SRAM cell. Figure 7e shows a 33% reduction in 3D SRAM cell area compared with traditional planar designs. Figure 7f shows the large-scale array of SRAMs. As shown in Figure 8a-c, the SRAM exhibits the highest normalized hold noise margin, superior gain, and the lowest static power consumption among existing flexible SRAMs. From Figure 8d, the SRAMs show an exceptional mechanical flexibility during rigorous deformation processes Notably, the SRAM maintains stable dynamic performance (Figure 8e), and can function in high-temperature air environments (333 K), as shown in Figure 8f.

3. Conclusions

In this review, we have detailed our advancements in flexible integrated M3D CMOS electronics. The innovative M3D structure eliminates inter-tier vias by sharing both the gate electrodes and drain electrodes across different layers, enhancing integration density and performance. The demonstrated inverter achieves area saving by up to 45%, and a record gain of 191 while maintaining stable operation after 6000 bending cycles at a 500 μm radius, underscoring its superior flexibility among existing flexible M3D inverters. The flexibility is attributed to the use of intrinsically flexible materials, thin film designs, and the inter-tier-via-free architecture. We successfully integrated multi-stage circuits, including logic gates, ROs, D latches, and 6T-SRAMs, which exhibit reliable logic operation or data storage capabilities. The 55-stage RO demonstrated high integration density with a 45% area reduction, outputs a square waveform and showcases mechanical flexibility for large-scale circuits. The ultra-flexible SRAM has reduced the footprint by 33% and demonstrated excellent static and dynamic characteristics, including a normalized hold noise margin of 73.6% and a gain of 151.2, alongside minimal static power consumption. These designs reduce delay time by minimizing routing, and enhance circuit performance. We have also explored the system applications. Besides, the design also mitigates material compatibility issues between n- and p-type devices, broadening the options for flexible CMOS realization. Overall, the flexible M3D CMOS circuits exhibit outstanding flexibility, electronic performance, and integration potential, paving the way for future applications in wearable electronics, health monitoring, intelligent robotics, and human-machine interfaces.

4. Acknowledgements

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