Study of AMOLED Source Fast-Charge Simulation

Shuai Hou*, Chenghao Liao*, Guoqiang Wu*, Changman Kim*, Zhi Zhang*
***Chengdu BOE Optoelectronics Group Co., Ltd. Chengdu, China**

Abstract
This paper studies the design of a pre-charging circuit in source driver integrated circuits (ICs). We control the charging timing of the AMOLED module to achieve rapid charging effects. For the FHD+ resolution module operating at a 144Hz frame rate, the speed of the fast charging model is increased by 43%, while the load current is reduced by 8.5%. This innovative fast charging model effectively mitigates the color bias issue caused by insufficient source charging under heavy loads. Furthermore, the implementation of this fast charging model enables us to enhance the performance of a 165Hz display.

Author Keywords
AMOLED; Load model; Fast charging; Low power consumption

1. Introduction
With the continuous advancement of display technology, the market demand for high-quality display equipment is increasingly robust. AMOLED display devices, among the most sought-after display technologies, are now subject to stringent requirements for high resolution and high frame rates. To achieve a frame rate exceeding 144Hz for AMOLED screens produced under the existing LTPS process conditions, it is essential to address the issue of insufficient charging time for source signals[1]. Currently reported methods to enhance charging speed include: first, accelerating the source charging speed by increasing the source current[2, 3], however, this approach is not conducive to reducing power consumption. Second, the load of the AMOLED circuit can be reduced through the use of new processes and materials, thereby increasing the charge and discharge speed of the drive circuit[4]. Nevertheless, such methods significantly raise manufacturing costs. Consequently, finding a way to achieve rapid charging of source signals with low power consumption and minimal cost has become one of the most critical areas of research for high frame rate AMOLED display devices.

In this study, we conducted simulation experiments on the charging of source driver signals based on the AMOLED load model. We analyzed the panel's load, driving current, and the charging speed of the source signal. A control circuit was designed to manage the transition time of the source driver circuit between no-load and load conditions through simulation, enabling rapid charging and significantly reducing power consumption. By applying the findings from this research, we aim to develop low-power, cost-effective AMOLED display devices capable of achieving 165 Hz.

2. Experimental model
The p-mode field-effect transistor (TFT) is utilized to construct the driver circuit for AMOLED devices. Due to potential fluctuations in the threshold voltage (Vth) of the driver TFT caused by manufacturing variations, a 7T1C driver circuit is selected to compensate for Vth (Figure 1). During the actual charging process of the AMOLED source data, the equivalent resistance and parasitic capacitance in the fanout wiring, active wiring, and pixel TFT circuit must be considered. Consequently, we established the RC circuit model illustrated in Figure 2.

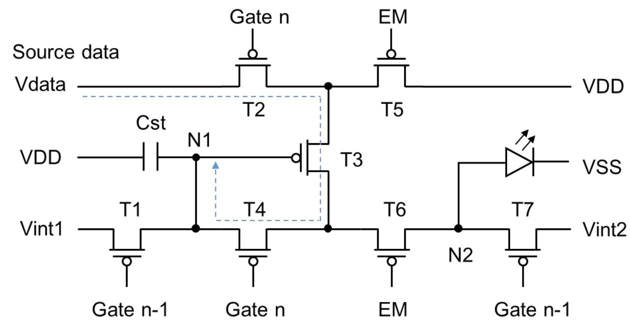

Figure 1. AMOLED 7T1C Drive circuit

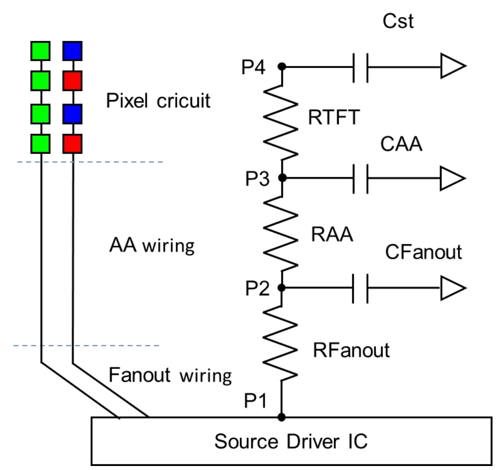

Figure 2. Source circuit equivalent RC model

The source drive voltage is delivered to the panel through the source pad. Initially, it traverses the panel fanout wiring (from P1 to P2), where the equivalent resistance is denoted as R_{Fanout} and the parasitic capacitance is C_{Fanout}. Subsequently, it enters the panel's active area (from P2 to P3), where the equivalent resistance of the source data line is R_{AA} and the parasitic capacitance is C_{AA}. Finally, after passing through the T2, T3, and T4 tubes (from P3 to P4), the source data voltage is stored in the pixel capacitor C_{st}, which is characterized by the equivalent resistance R_{TFT} and capacitance Cst. The FHD+ resolution AMOLED screen (1260 x 2800) was utilized to extract the equivalent RC loading parameters for the farthest pixel, as detailed in Table 1.

Table 1. Simulation parameters of source RC load

Item	P1-P2	P2-P3	P3-P4	Total	Unit
	Fanout	AA	TFT		
R	6.56	5.01	196.08	207.65	KΩ
C	5.84	30.66	0.02	36.52	pF

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To achieve uniform luminescence in AMOLED devices, it is essential to accurately store V_{data} in the Cst within a specified timeframe. However, with a resolution of 1260 x 2800 pixels and a frame rate of 144 Hz, the maximum theoretical charging time for a single line is only 2.48 µs. Considering the actual line resistance and parasitic capacitance, Cst often fails to reach the predetermined voltage due to the slow charging of the source signal. This results in deviations in the brightness and color coordinates of the display from standard values. This issue is particularly pronounced in low-brightness images, where the high V_{data} makes them susceptible to color inaccuracies caused by insufficient charging. Consequently, improving the charging speed of the source signal has become a significant technical challenge in the development of AMOLED panels.

3. Results and Analysis

3.1 Source charge characteristics

Due to the effects of wiring resistance and parasitic capacitance, the actual load at both the near and far ends of the panel varies. The test point on the panel can only evaluate the source curve at point P1. Set the screen refresh rate to 144Hz and refer to Figure 3 for the tested source curve. At 100% driving current, the rise time (Tr) and fall time (Tf) are 1.25 µs and 1.29 µs, respectively. The remaining stable charging time of the panel is only 0.8 µs. When the screen displays a one-line overload, color distortion may occur due to insufficient charging. To address the color distortion issue, a common approach is to increase the source bias current. Gradually increase the source bias from 100% to 150%, which will enhance the charging speed. When the source bias reaches 130%, the color distortion phenomenon begins to improve. However, with a 150% source bias, the source current has risen to 210%.

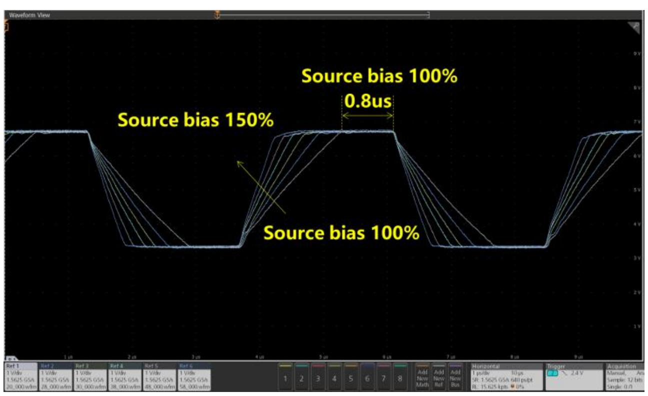


Figure 3. Source charge test curve

Table 2. Source settling time with different source bias

Source bias	Tr(µs)	Tf(µs)	I_S(µA)
100%	1.25	1.29	88.05
110%	0.99	1.03	101.67
120%	0.81	0.85	117.10
130%	0.71	0.73	137.42
140%	0.58	0.57	159.43
150%	0.52	0.47	184.93

In the context of high-resolution and high-frame-rate displays, inadequate charging may still occur even with maximum driving capacity. Utilizing the panel RC load model and the conventional source circuit, we utilize the V-T characteristic curve to assess the charging response of the panel source data, which ranges from 1V to 6.8V. The simulation results are illustrated in Figure 4. A discrepancy exists between the parameters extracted during panel loading and the actual conditions. By increasing the RC load parameters by 1.5 times, the simulation results align more closely with the actual test results.

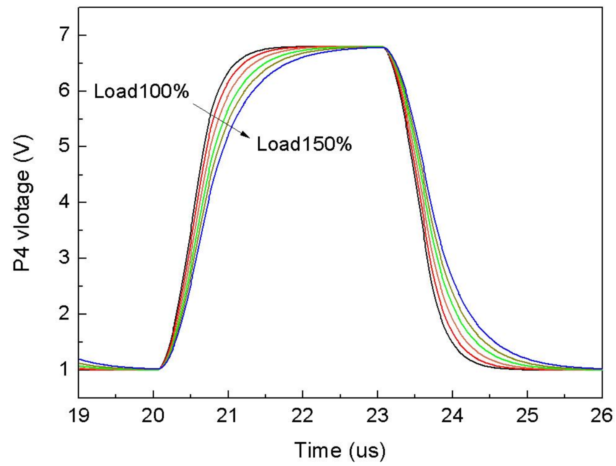


Figure 4. Source charge simulation curve

Table 3. Source settling time with different RC loading

Loading	Tr(µs)	Tf(µs)	I_S(µA)
100%	0.61	0.6	62.89
110%	0.71	0.7	67.52
120%	0.81	0.8	72.92
130%	0.92	0.91	78.29
140%	1.04	1.03	82.82
150%	1.17	1.16	87.81

3.2 Source fast charging model

To achieve a higher frame rate, it is essential to accelerate the source circuit to complete the charging and discharging of Cst. The challenge lies in achieving rapid charging while minimizing costs and power consumption. This paper presents results obtained from simulating a hybrid charging model that enhances source speed and reduces power consumption. As illustrated in Figure 5-a, the output terminal of the conventional source driver circuit is directly connected to the panel source line, meaning that the line load consistently represents the output load of the source amplifier (AMP). A control switch, M1 (PMOS), is added between the AMP and the source output pad, governed by the source control signal (S_C). When S_C is activated at a low voltage, the thin-film transistor M1 is enabled, allowing the source AMP to connect to the external panel load. Conversely, when the M1 TFT is off at a low voltage level, the source AMP only drives the internal load of the IC (C_{AMP}). The total charge transferred during the charging process, ΔQ, is equal to the sum of the IC and panel capacitance multiplied by the target voltage difference, Δ V (as shown in Formula 1). However, both the charging time and power consumption are influenced by the process voltage difference, indicating that a slower charging process will also result in higher power consumption.

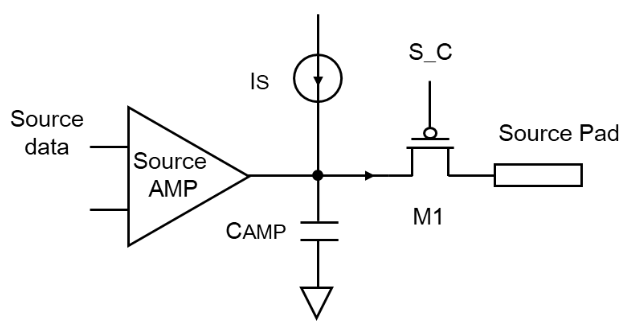
$$\Delta Q = (C_{IC} + C_{Panel}) \times \Delta V = \int idt \qquad (1)$$

The method aims to reduce line loss, improve the arrival time of the target voltage, and regulate the charging flow at an optimal level. As illustrated in Figure 5-b, when S_C signal is activated, the drive circuit is directly connected to the load, significantly impacting the charging process. S_C is designed to turn off the M1 TFT 200 ns before the actual output, allowing the source amplifier to initiate a voltage rise in advance under low load conditions and switch after reaching the target voltage. When S_C activates the M1 TFT, the source amplifier outputs directly to the panel at the target voltage, functioning as a constant current power supply. This composite charging process helps avoid the slow voltage rise of the source amplifier under external load conditions, thereby maximizing its output efficiency. Once the source amplifier completes the voltage preset, the actual charging process of the panel is executed according to the charging and discharging formulas with load (Formulas 2and 3)[5,6].

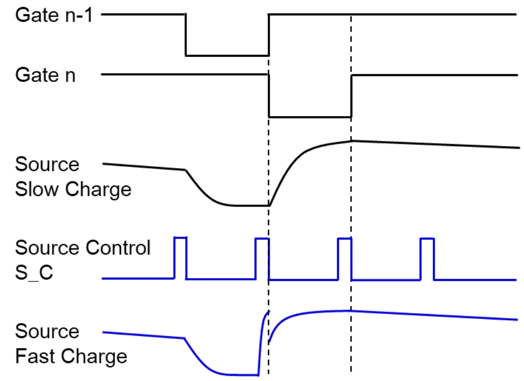
$$\text{Charge: } Q(t) = C\varepsilon(1 - e^{-t/RC}) \qquad (2)$$

$$\text{Discharge: } Q(t) = Q_0 e^{-t/RC} \qquad (3)$$

According to the previously mentioned source driver circuit and load control model, simulation experiments were conducted, with the blue lines representing the fast charging results in Figure 6. Based on the existing source amplifier circuit structure, a capacitance of 2 pF was implemented in the C_{AMP} system. After resetting Gate n-1, the establishment of point P1 and its subsequent voltage depend on the output current IS. The source amplifier is activated, but transistor M1 remains off. At this stage, the load on the source amplifier is minimal, allowing for the rapid establishment of the voltage at point P0. When S_C and Gate n simultaneously reach the falling edge, the transistors M1, T2, T3, and T4 are activated concurrently. Given that the potential at P0 has been established, the voltage transition from points P1 to P4 will exceed that of a conventional drive circuit.



(a) Source control circuit model



(b) Source fast-charge wave

Figure 5. Source fast-charge module

According to the fast charge simulation results (Figure 6), the P4 Tr/Tf values are 0.55/0.58 µs, and the IS current is 57.5 µA. The speed at which Cst charges to a stable level has increased by 43%. The IS records the average current within 3 µs after the source amplifier is activated. Theoretically, the total energy required under the same load remains constant. However, the fast charging structure, based on the previously mentioned source control scheme, occupies a relatively small proportion of the 3 µs due to its rapid establishment time. Consequently, the average power consumption is lower, resulting in an annual reduction of 8.5% in power usage. At a frame rate of 165 Hz, utilizing the fast charging model, Cst can still achieve a stable charging time of 1.21 µs. When combined with advancements in panel processing and improvements in the driving capability of the source circuit, the realization of a 165 Hz display is within reach.

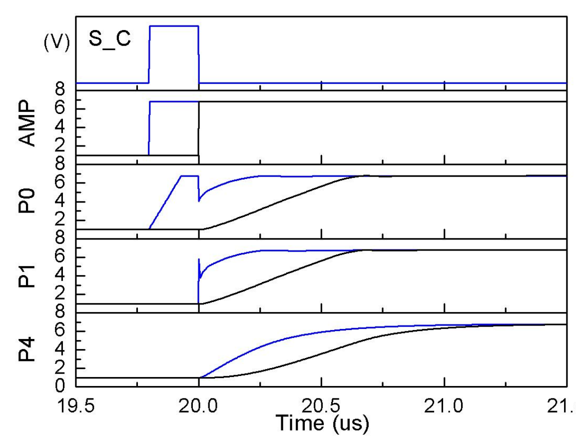


Figure 6. Source fast-charge simulation curve

The actual test results of the source signal at point P1 in the fast charging scheme are illustrated in Figure 7. After activating the source fast charge function (S_C on), the Tr/Tf values are 0.43/0.4 µs, which is significantly faster than the charging time under the 100% source bias condition. At this point, the stable time for fast charging is comparable to the charging time under the 130% source bias, with both being 1.4 µs. In comparison to the method that solely increases the driving current, the fast charging scheme demonstrates significantly improved performance.

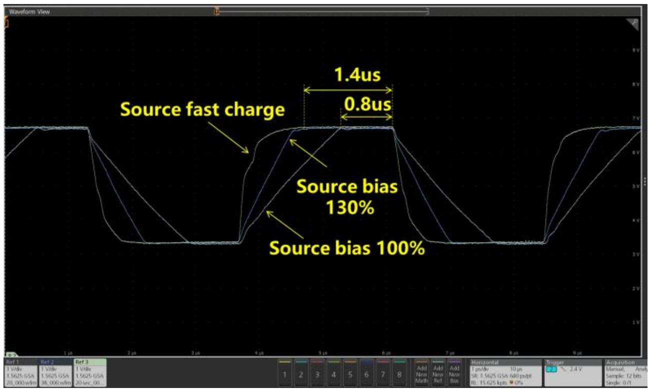


Figure 7. Source fast-charge test curve

As illustrated in Figure 8, when displaying the 1-horizon line image at 144 Hz, the image quality appears significantly redder due to insufficient charging. Although increasing the source bias to 130% has improved image quality, it is still a slight color shift. Furthermore, raising the refresh rate to 165 Hz, even with the source bias current increased to a maximum of 150%, does not provide adequate stable charging time, resulting in a persistently reddish image quality. However, when the fast-charge feature is utilized, we can enhance the source charging speed by over 43%, which significantly improves the image quality of overloaded images at both the 144 Hz and 165 Hz settings.

Figure 8. Overload effect for 1-horizon line image

4. Conclusions

According to the data obtained from the charging simulation experiment based on the AMOLED panel load model, the panel load is the primary factor influencing the charging speed and power consumption of the source. Increasing the source AMP driving force can accelerate the charging time; however, this also leads to a substantial increase in power consumption. For example, when the source AMP driving force is increased by 1.5 times, the charging speed rises by 37.5%, while power consumption surges to 210%. By controlling the pull-up time of the source driver circuit under both no-load and load conditions, we achieved an effective fast charging outcome for the source data. The charging speed increased by 43%, while power consumption was reduced by 8.5%. Additionally, the quality of images depicting heavy loads has significantly improved. Therefore, based on this fast charging model, we anticipate an increase in the frame rate from 144Hz to 165Hz.

5. References

1. Xingheng, et al. High-speed low-power voltage-programmed driving scheme for AMOLED displays. Journal of Semiconductors (2016).
2. Jeon, J. Y. , et al. A Direct Fast Feedback Current Driver Using an Inverting Amplifier for High-Quality AMOLED Displays. IEEE Transactions on Circuits & Systems II Express Briefs 59.7(2012):414-418.
3. Lee, Geon Ho , et al. P-45: A Fast Driving Circuit for AMOLED Displays Using Current Feedback. SID Symposium Digest of Technical Papers 37.1(2012):363-365.
4. Fan, Ching Lin , et al. LTPS-TFT pixel circuit compensating for TFT threshold voltage shift and IR-drop on the power line for AMOLED displays. Advances in Materials Science and Engineering 2012(2012).
5. Hsu, Chih Cheng , et al. Pixel circuit with external current source to achieve fast compensation for variations of LTPS TFTs for AMOLED displays. IEEE (2017).
6. Lu, Li , et al. A Fast Ramp-Voltage-Based Current Programming Driver for AMOLED Display. Circuits and Systems II: Express Briefs, IEEE Transactions on 66.7(2019):1129-1