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<https://doi.org/10.1002/jsid.2068>

Effective 10-bit OLED Driver IC with 11-bit DAC, Double Capacitor-Coupled Adder, and Offset Calibration for Enhanced Panel Driving

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Abstract

Proposed is an 11-bit source driver IC for high-resolution OLED displays, utilizing a Double Capacitor Coupled Adder (DCCA) for parallel sampling and driving. A Slow Rate Enhancement (SRE) circuit ensures fast response under minimal voltage differences, while Offset Calibration minimizes inter-channel voltage deviations. Experimental results show a 2.0 μ s line time, 9.9 V/ μ s slew rate, and a DVO of 2.43 mV, showcasing precision and efficiency.

Author Keywords

OLED driver IC; double capacitor-coupled adder; slew rate enhancement; offset calibration; source driver; deviation of voltage outputs

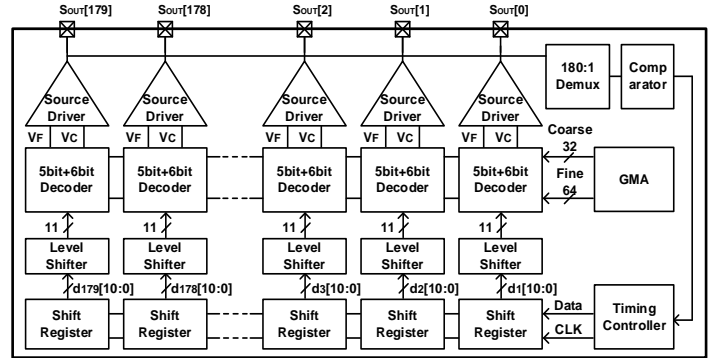


Figure 1 Block diagram of the proposed OLED driver IC

1. Introduction

With the recent advancements in Organic Light-emitting Diode(OLED) display driving technology, there is an increasing demand for high-performance driver ICs capable of accurately and stably driving panels at high resolutions and frame rates. In response to this demand, Umeda et al. were the first to propose an Liquid Crystal Display(LCD) driver with a Capacitor Coupled Adder, introducing an effective method for performing sampling and driving in analog signal processing[1]. Additionally, Huang et al. improved area efficiency by proposing a 12-bit structure that sums three voltages[2]. However, these designs require sequential sampling and driving within a 1-H interval, resulting in time constraints. Meanwhile, Jo et al. proposed a High-Gain Fast-Slew Circuit for high-resolution and high-frame-rate OLED displays, but this approach has a limitation in that the slew detector only activates when the input-output voltage difference exceeds the threshold voltage[3].

In recent studies, minimizing the DVO has emerged as a key criterion for evaluating driver IC performance. A low DVO indicates high inter-channel voltage uniformity, which is crucial for enhancing display image quality[4].

To overcome the limitations of prior designs, this paper proposes a structure that uses two capacitors to allow the sampling and driving phases to occur simultaneously, thereby improving temporal efficiency. Additionally, we present a SRE circuit capable of responding quickly even when input-output voltage differences are minimal, achieving the fast response speed and stability required for high-resolution display driving. To further improve performance, our design employs Offset Calibration, achieving a low DVO value and enhancing output uniformity across channels.

2. Proposed Driver IC

Figure 1 shows the block diagram of the proposed OLED driver IC. Although the IC is designed with 11-bit resolution, 1 bit is

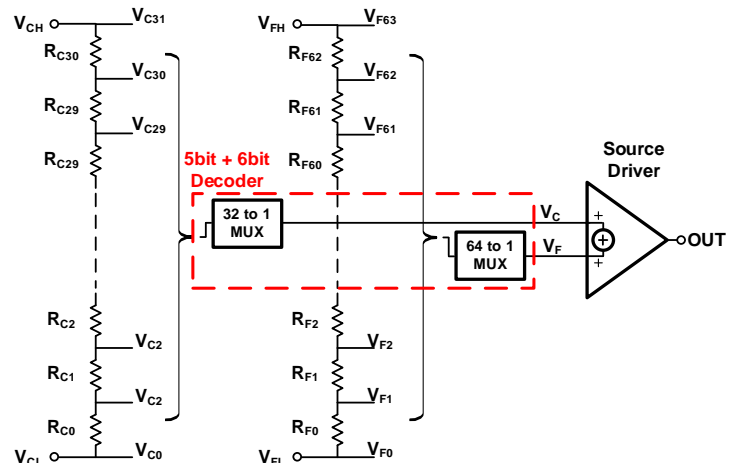


Figure 2. Block diagram of the 11bit R-Ladder DAC

allocated for offset calibration, providing an effective 10-bit performance. This calibration bit aligns the offset across channels, thereby enhancing the DVO.

Input data is sequentially received via the shift register and subsequently converted into coarse voltage(V_C) and fine voltage(V_F) through a 5-bit + 6-bit decoder. The generated V_C and V_F are then transmitted to the source driver, which outputs the final pixel driving voltage.

To ensure voltage uniformity across channels, the offset calibration process uses a comparator to detect channel discrepancies and sends calibration values to the Timing Controller (T-Con) to minimize these errors. This process significantly improves DVO, particularly in high-resolution panels.

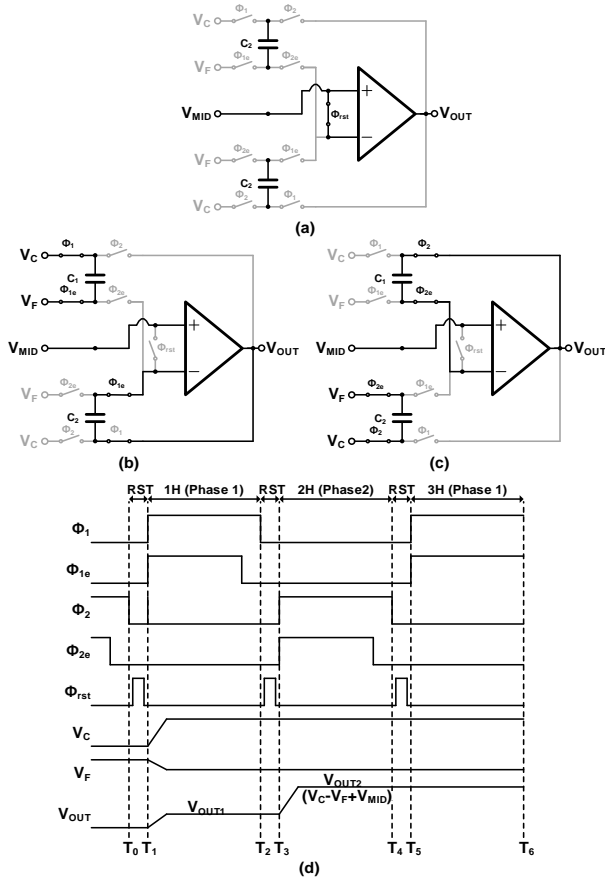


Figure 3. Operation of proposed double capacitor coupled adder (a) Reset mode (b) 1 H (c) 2 H (d) Timing diagram

3. Capacitor Coupled Adder

Figure 2 shows the block diagram of the proposed 11-bit R-Ladder DAC. This design uses two resistor strings to generate V_C and V_F , which are then summed to produce the final output. This approach enhances the precision of the resistor string-based DAC while improving area efficiency.

Figure 3 shows the operation of the proposed DCCA, displaying the circuit configuration in each mode alongside the timing diagram. In the Reset Mode, capacitors are initialized by the Φ_{rst} signal, while during the 1H phase, V_C and V_F are sampled across both terminals of C_1 . The delay between Φ_1 and Φ_{1e} is implemented to minimize the impact of the V_C on the fine voltage sampling. In the 2H phase, the output is generated based on the voltages sampled in 1H, while C_2 is simultaneously used for sampling. The output voltage at this stage can be expressed as follows:

$$V_{OUT} = V_C - V_F + V_{MID} \quad (1)$$

The proposed DCCA structure leverages two capacitors, allowing the full 1-H period to be utilized for both sampling and driving. This design achieves both temporal efficiency and high-speed response.

4. Amp Offset Calibration

Figure 4 illustrates the operating principle of the proposed offset calibration circuit. During this process, 6bit DEC sequentially delivers the voltages from the fine R-ladder to the

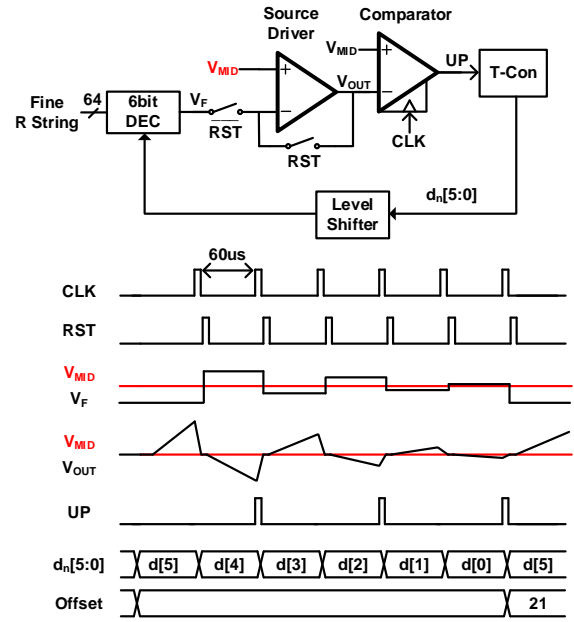


Figure 4. Principle of amp offset calibration

input of the comparator, allowing precise adjustment of the offset. During source driver calibration, it is kept in an open-loop state, allowing the output voltage V_{OUT} to increase or decrease depending on the values of V_{MID} and V_F . This design enhances the durability of the system against noise and kick-back effects from the comparator by amplifying the output of source driver. The Comparator detects the difference between V_{MID} and V_{OUT} and generates an UP signal accordingly. Following this, the reset(RST) signal disconnects V_F , and the amplifier transitions to a closed-loop state. At this point, V_{OUT} is determined as a voltage offset from V_{MID} . The UP generated by the comparator is transmitted to the T-Con, and through a 6-step binary search process, the optimal offset value is determined. The final offset value is stored in a register and is used to maintain uniform output voltage across all channels.

In the source offset calibration process, a 180:1 Demux connects 180 source channels to a single comparator, ensuring that a consistent comparator offset is applied across all channels. This design reduces output voltage deviation, and the calibrated offset values are periodically applied to each channel by the T-Con.

5. Slew Rate Enhancement

Figure 5 shows the circuit diagram of the SRE functionality implemented in the proposed source driver circuit. The SRE circuit is designed to respond quickly even to small differences between the input voltage(V_{IN}) and the output voltage(V_{OUT}). To achieve this, the Width/Length (W/L) ratios of the NMOS and PMOS transistors are adjusted according to their respective roles. The W/L ratios of MN1, MP1, MP2 and MP2 are set to 1:4, while those of MN3, MP3, MN4 and MP4 are set to 1:2, ensuring that MN1 and MP1 turn off easily even when there is a small voltage difference between the input and output. This design prevents current from flowing through MN5 and MP5, keeping MN6 and MP6 off, thus preventing current flow through ISRE in a static state.

Figure 6 illustrates the operation of the SRE when the input is rising. The W/L ratios of MN5, MP5, MN6, and MP6 are set to 1:8, allowing a maximum of eight times the current to flow

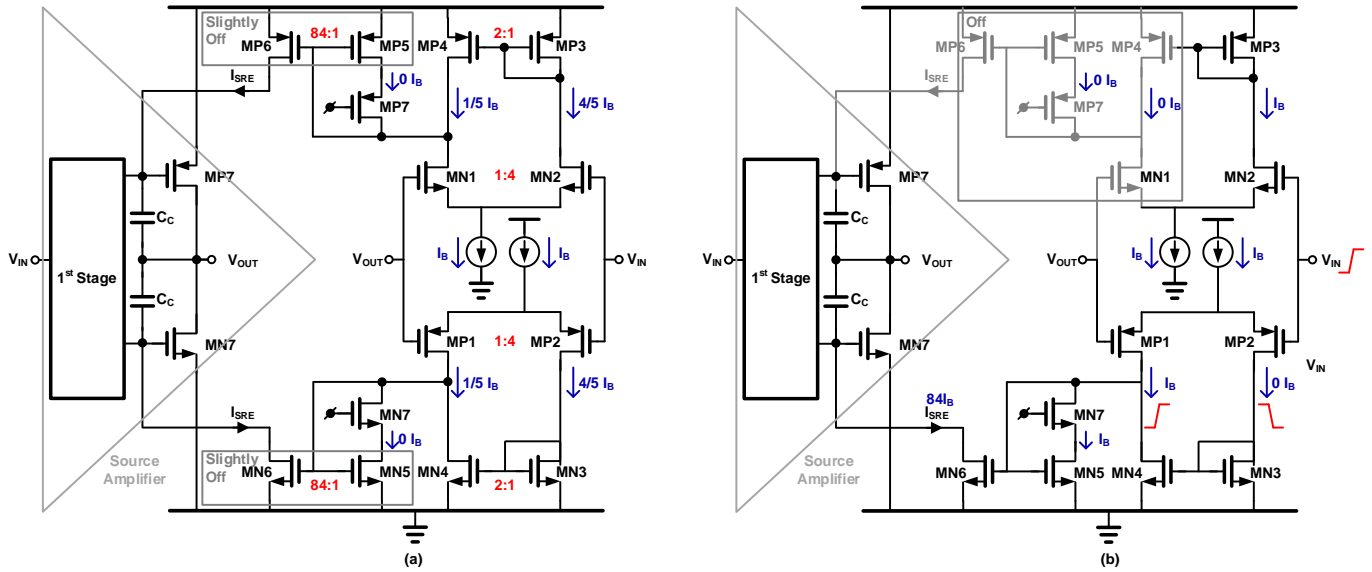


Figure 5. Schematic and principle of source driver with slew rate enhancement (a) Schematic (b) Principle



through I_{SRE} . Additionally, MN7 and MP7 are biased to prevent excessive current flow through I_{SRE} . This dynamic current scaling ensures that the amplifier stabilizes quickly.

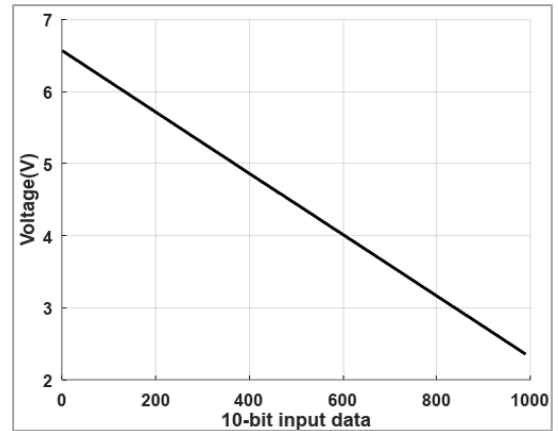
6. Measurement Results

Figures 6 to 9 present the measurement results for six channels of the proposed OLED driver IC, showcasing linearity, offset calibration, and output waveforms. Figure 6 shows a die photograph of the IC fabricated in a Chip-on-Film (COF) package, which was designed to improve integration and is optimized for high-resolution displays.

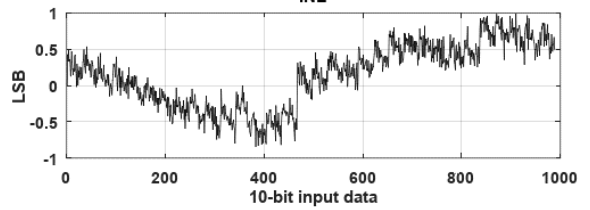
Figure 7 illustrates the linearity performance of the IC. Subfigure (a) shows the source driver's output characteristics corresponding to the 10-bit input data, confirming that the output maintains linearity across the entire input range. Subfigure (b) displays the INL and DNL performance, where both remain within ± 1 LSB and demonstrate monotonic behavior.

Figure 8 compares the results before and after offset calibration. The maximum deviation between channels was initially 12.99 mV, which was reduced to 2.43 mV after calibration.

Figure 9 shows the transient response and slew rate of the source driver. The output swing of the source driver reaches 3.27 V relative to the input signal. For a 10% to 90% transition, with I_B ranging from 100 nA to 200 nA, the rise time was measured to be between 264 ns and 128 ns. During this period, the slew rate ranged from 9.9 V/ μ s to 20.4 V/ μ s. Figures 6 to 9 present the measurement results for six channels of the proposed OLED



(a)



(b)

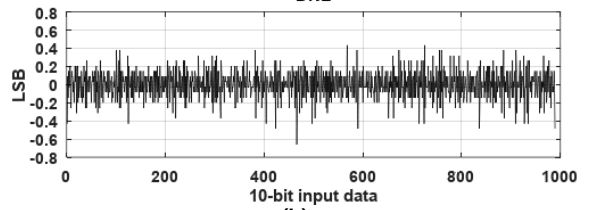


Figure 8. Measurement results with for channel proposed driver IC (a) Output characteristic (b) INL & DNL

driver IC, showcasing linearity, offset calibration, and output waveforms. Figure 6 shows a die photograph of the IC fabricated in a Chip-on-Film (COF) package, which was designed to improve integration and is optimized for high-resolution displays.

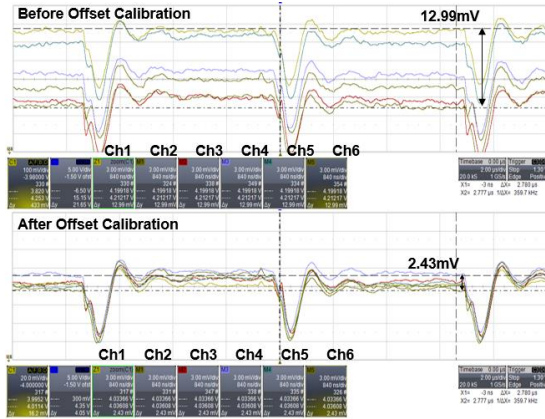


Figure 9. Measurement results before and after Offset Calibration

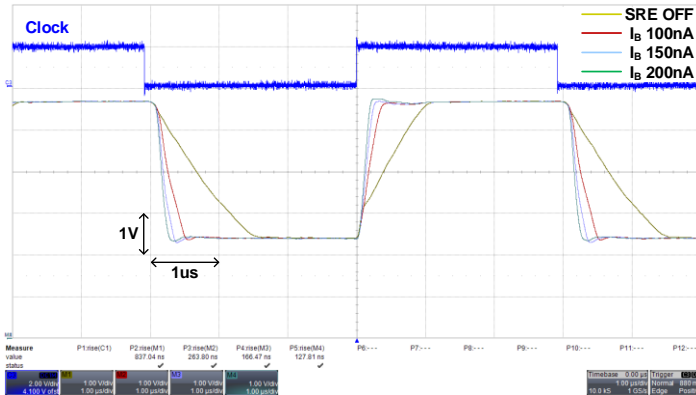


Figure 10. Output Swing of Source Driver

7. Conclusion

The proposed OLED Driver IC is designed with an 11-bit resolution architecture based on a 28nm process, achieving both high resolution and excellent area efficiency compared to conventional structures through the use of a DCCA. This IC provides high precision with an effective output performance corresponding to 10 bits, enabled by offset calibration.

As shown in Table 1, the proposed IC achieves a short line time of 2.0 μ s and a stable slew rate of 9.9 V/ μ s with a load capacitance of 46.6 pF. This represents the fastest slew rate relative to current consumption compared to previous studies. Additionally, after offset calibration, the maximum DVO is reduced to 2.43 mV, demonstrating superior uniformity compared to other studies.

In conclusion, the proposed OLED Driver IC meets high resolution, fast response time, low power consumption, and compact area requirements, making it a promising solution for next-generation high-performance OLED display driving applications.

Table 1. The performance summary of the proposed OLED driver IC with a comparison table

	This Work	JSID 2024 [3]	JSSC 2023[4]	VLSI 2021[5]	ISSCC 2024[6]
Process	28nm	28nm	130nm	180nm	65nm
Gray Scale	11 bit (5b+6b)	11b (7b+4b)	10 bit (10b + 0)	12 bit (7b+5b)	10 bit (10b + 0)
DAC Architecture	Double Capacitor Adder		SC-multiplier +LSB stack-up	Piecewise Linear	Global Slope-DAC
Line time	2.0 μ s	2.7 μ s	8.0 μ s	2.0 μ s	8.2 μ s
Slew Rate	9.9 V/ μ s @46.6pF	7.645V/ μ s @54pF	8.1V/ μ s @30pF	6.24 V/ μ s @80pF	4.7V/ μ s @30pF
Static Current (uA/ch)	1.28 uA	1.2uA	1.8 uA	2.0 uA	1.5 uA
Output Range (V)	2.56 ~ 6.36	3.0 ~ 6.8	0.3 ~ 4.5	0.1 ~ 4.9	0.3 ~ 4.7
DNL / INL (LSB)	0.66 / 0.98	0.48 / 0.50	0.39 / 0.9	0.43 / 0.95	0.49 / 0.85
Max. DVO	13mV / *2.43 mV	11 mV	4.82 mV	7.9 mV	10.0 mV
Area	4790 μ m ² (290.3 x 16.5)	N/A	2304 μ m ² (144 x 16)	5015 μ m ² (295 x 17)	2171 μ m ² (135.7 x 16)

*DVO after offset calibration

8. References

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