Challenges of Atomic-Layer-Deposited Oxide Semiconductor Channels beyond PVD: Material, Devices, and M3D Stacked Structures

Yoon-Seo Kim[1], Su-Hwan Choi[2], Hyejin Oh[1], Taewon Hwang[1], and Jin-Seong Park[1,2]
[1]Division of Materials Science and Engineering, Hanyang University, Seoul, Korea
[2]Division of Nanoscale Semiconductor Engineering, Hanyang University, Seoul, Korea

Abstract
This study explores ALD-based oxide semiconductors, highlighting in-situ composition control, atomic-scale ordering, and interface engineering. High-mobility (>100 cm²/V·s) IGZO and stable p-type SnO (<5 cm²/V·s) devices are achieved via optimized ALD processes. We demonstrate monolithic 3D-stacked complementary transistors and propose N_2O plasma for addressing mobility-stability trade-offs. ALD's pivotal role in scalable, high-performance active-matrix device fabrication is emphasized, showcasing its potential for mass production.

Author Keywords
Atomic Layer Deposition, Oxide Semiconductor, Thin Film Transistor, High field-effect mobility IGZO, Nitrogen doping, p-type SnO, Monolithic Stacked Complementary FET.

1. Introduction
Since the first demonstration of amorphous IGZO (In-Ga-Zn-O) by Hosono et al., oxide semiconductors have revolutionized the display industry, particularly in OLEDs, due to their moderate mobility, low off-current, and large-area uniformity [1]. IGZO thin-film transistors (TFTs) are ideal for high-resolution displays (>1000 ppi) owing to their superior short-channel immunity and 3D processability enabled by atomic layer deposition (ALD) [2]. For instance, vertically stacked IGZO TFTs have achieved resolutions of up to 1360 ppi [3].

However, challenges remain, particularly in addressing the mobility-reliability trade-off caused by oxygen vacancy defects, which enhance carrier concentration but degrade reliability under stress [4,5]. Crystalline oxide semiconductors have emerged as a promising solution by optimizing electrical properties through controlled crystallinity. Examples include top-gate self-aligned CAAC-IGZO TFTs achieving 1058 ppi [7] and ultra-high-density displays exceeding 5291 ppi through innovative design [8,9]. Yet, these approaches face limitations in free-form, low-temperature applications like automotive, wearable, and AR/VR displays.

Atomic layer deposition (ALD) offers transformative advantages for oxide semiconductor fabrication, crucial for advancing thin-film transistor (TFT) technology in Figure 1. Key benefits include: (1) precise in-situ composition control, enabling optimized electrical properties and homogeneous material quality; (2) vertical structure engineering, allowing multi-channel designs for enhanced mobility and reliability; (3) tailored chemical reaction dynamics, leveraging advanced precursors and reactants for superior film quality; and (4) improved insulator and interface engineering for device stability. These features address critical challenges like mobility-stability trade-offs, scalability, and uniformity, positioning ALD as a pivotal process for next-generation high-performance and high-density devices. ALD offers precise thickness control, tunable cation ratios, and superior 3D processability [10,11]. In this study, we developed pseudo-single-crystal (PSC) IGZO by modulating oxygen plasma power, achieving tailored atomic ordering and electrical properties [12]. ALD conditions were also optimized for SnO crystallinity, enabling monolithic stacked complementary field-effect transistors (CFETs) with IGZO and SnO [13,14]. This work provides key insights into high-pixel-density oxide semiconductors for future monolithic stacked display technologies (Figure 2).

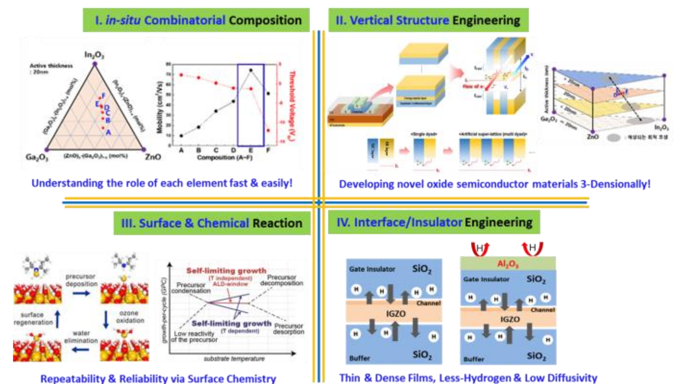

Figure 1. Four Values of ALD Oxide Semiconductor Channels and the associated TFT application.

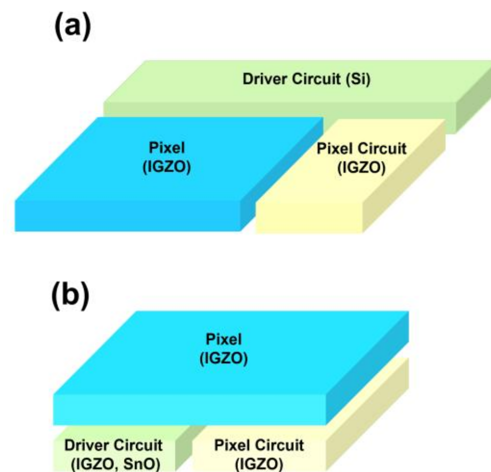

Figure 2. Panel design for (a) proposed high pixel density [8] and (b) M3D stacked.

2. Atomically Ordered (AO) IGZO via ALD
The crystallization of IGZO from an amorphous to a CAAC

ISSN 0097-996X/25/5602-0946-$1.00 © 2025

structure typically requires additional processes, such as post-annealing at temperatures above 700 °C or catalytic metal layer-induced crystallization [15,16]. However, these methods are unsuitable for monolithic stacked structures in future displays. To address this, the ALD process was optimized by modulating the cation ratio and reactant oxidation energy to achieve a single crystal-like structure.

Figure 3 demonstrates the successful formation of atomically ordered (AO)-IGZO at an optimized sub-cycle ratio of In:Ga:Zn = 12:1:1. The electrical properties of AO-IGZO channel TFTs vary with oxygen (O_2) plasma reactant power, as shown in Figures 2(b) and 2(c). Table 1 summarizes the key electrical parameters—field-effect mobility (μFE), threshold voltage (Vth), subthreshold swing (S.S.), and hysteresis—for ten devices.

Notably, the IGZO TFT fabricated at 70 W plasma power exhibits high mobility and a low S.S. but shows a slightly negative Vth shift due to carbon and hydrogen-related defects caused by the lower plasma power. Conversely, plasma powers above 300 W degrade mobility due to damage to the PSC structure. The optimized condition, achieved at 100 W plasma power, produces AO-IGZO with superior electrical properties (μFE = 114.31 cm²/V·s, Vth = −0.44 V, S.S. = 89.79 mV/decade) and minimal impurity-related defects.

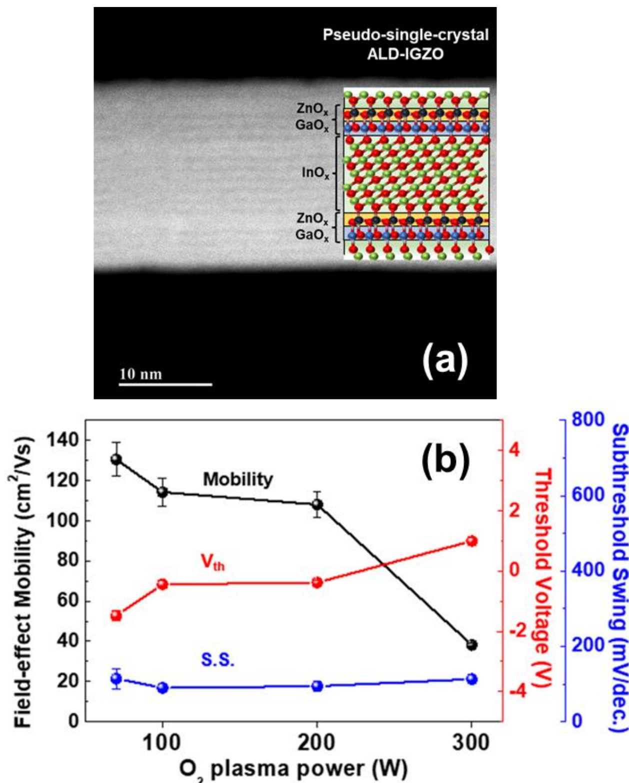

Figure 3. (a) Cross-sectional image of the transmission electron microscope (TEM) image and schematic of atomic-ordering of PSC-IGZO structure. (b) electrical properties comparison according to the O_2 plasma power

As shown in Figure 4, AO-IGZO channel TFTs deposited at 100 W also demonstrate excellent positive bias temperature stress (PBTS) reliability, with only a 0.53 V positive shift under PBTS conditions (95 °C, 2 MV/cm stress, 1 hour). This superior reliability stems from the AO structure's resistance to oxygen vacancy-related defects, which typically degrade device performance.

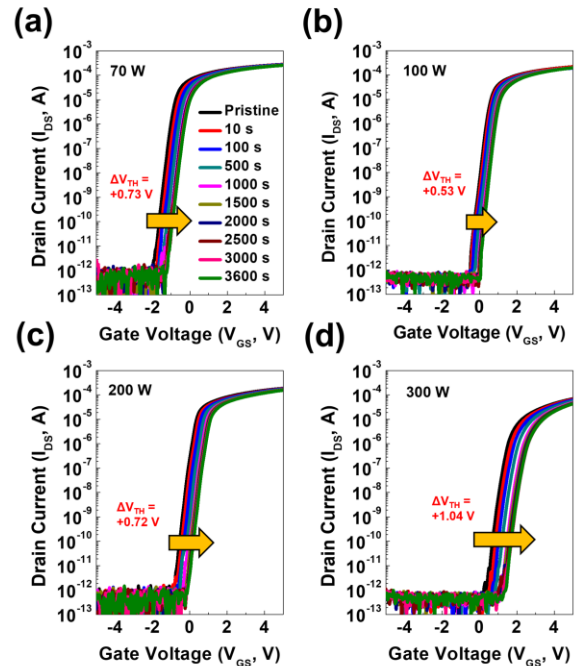

Figure 4. Positive bias temperature stability of PEALD-IGZO in different plasma power.

3. Precursor Discrete Feeding Method for SnO

The SnO p-type semiconductor exhibits a 2D crystalline structure with (001) planes aligned along the c-axis. Recent ALD studies highlight process optimization for improved surface coverage. The discrete feeding method (DFM), which divides the pulse and purge steps in a single ALD cycle, enhances surface coverage and throughput. DFM has been shown to increase growth per cycle (GPC) and reduce defect states during initial growth.

Our study focuses on DFM’s potential to improve crystallinity. Enhanced surface coverage within a single ALD cycle promotes lateral growth, improving the 2D crystalline structure (Figure 5). The DFM approach successfully improved GPC and the crystalline state of SnO, leading to better electrical properties in p-type SnO TFTs. Specifically, field-effect mobility increased to 1.86 cm²/V·s, and the subthreshold swing (S.S.) decreased to 110 mV/decade, attributed to reduced grain boundary defects.

Additionally, DFM-deposited SnO TFTs demonstrated superior negative bias temperature stress (NBTS) reliability, with a 0.11 V shift under NBTS conditions (60 °C, 2 MV/cm stress, 1 hour), as shown in Figure 6. These results underscore DFM’s effectiveness in enhancing both crystallinity and device performance.

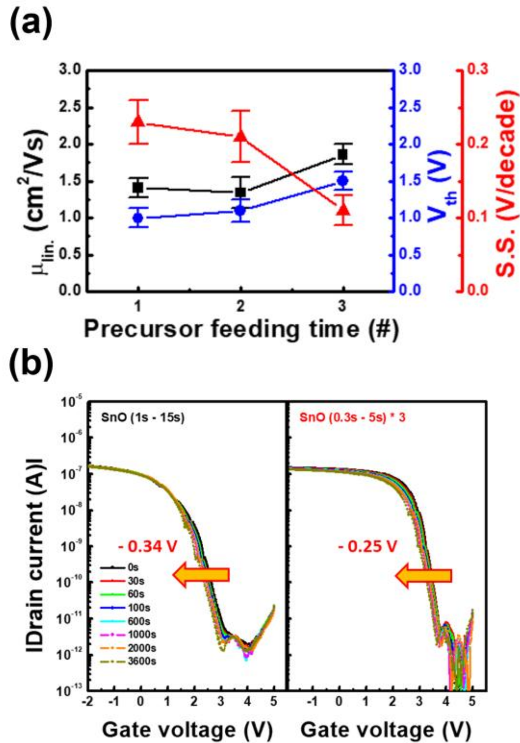

Figure 5. (a) electrical properties of TFTs according to the number of precursors feeding time. (b) NBTS reliability results of conventional and DFM deposited SnO TFTs

4. Monolithic Vertically Stacked CFET

The monolithic vertically stacked complementary FET (CFET) comprising IGZO and SnO TFTs was successfully fabricated using the ALD method for the channel materials. Figure 6(a) illustrates the CFET schematic and process flow chart. To minimize hydrogen diffusion during TFT fabrication and post-annealing, thermal ALD with ozone as a reactant was employed for the Al_2O_3 interlayer dielectric. Following the fabrication of the p-type SnO TFT, rapid thermal annealing (RTA) was performed at 300 °C for 5 minutes in an N_2 ambient to activate the p-type SnO TFT.

Thermal ALD-deposited Al_2O_3 was employed as a passivation layer for SnO TFTs to prevent oxidation of SnO to SnO_2 during the CFET fabrication and stacking processes. Figures 6(b) and 6(c) illustrate the voltage transfer characteristics (VTCs) and voltage gain of the all-oxide ALD vertically stacked CFET as a function of input voltage (Vin), respectively.

The VTCs of the CFET, measured at supply voltages (VDD) ranging from 2 to 10 V, demonstrate clear rail-to-rail inverter output curves, with a maximum voltage gain of 44.7 V/V achieved at VDD = 10 V. Figure 6(d) presents the noise margin and transition voltage extracted from the output voltage (Vout) as a function of Vin. The transition voltage, defined as the point where Vin equals Vout, exhibited a positive shift with increasing VDD. At VDD = 10 V, the CFET achieved a noise margin of 87.5% and a transition voltage of 1.25 V, indicating robust and reliable performance.

5. Impact

In this study, we highlight the transformative potential of the ALD method for achieving precise atomic-scale control and superior electrical properties in IGZO and SnO, enabling advanced monolithic stacked display applications. By optimizing oxygen plasma power, AO-IGZO was developed, exhibiting exceptional electrical performance (field-effect mobility = 114.31 cm²/V·s, Vth = −0.44 V, S.S. = 89.79 mV/decade) and reliability (0.53 V positive shift under PBTS at 95 °C and 2 MV/cm for 1 hour). The tunability of atomic ordering and properties underpins its suitability for scalable applications.

Additionally, the ALD precursor feeding method enhanced the crystallinity and p-type electrical performance of SnO (field-effect mobility = 1.86 cm²/V· s, Vth = 1.5 V, S.S. = 110 mV/decade) while improving reliability (0.11 V negative shift under NBTS at 60 °C and 2 MV/cm for 1 hour). Furthermore, the successful fabrication of a vertically stacked CFET demonstrated a voltage gain of 44.7 V/V and a noise margin of 87.5% at a 10 V supply voltage. These findings emphasize ALD's critical role in advancing scalable, high-performance device architectures for future display technologies.

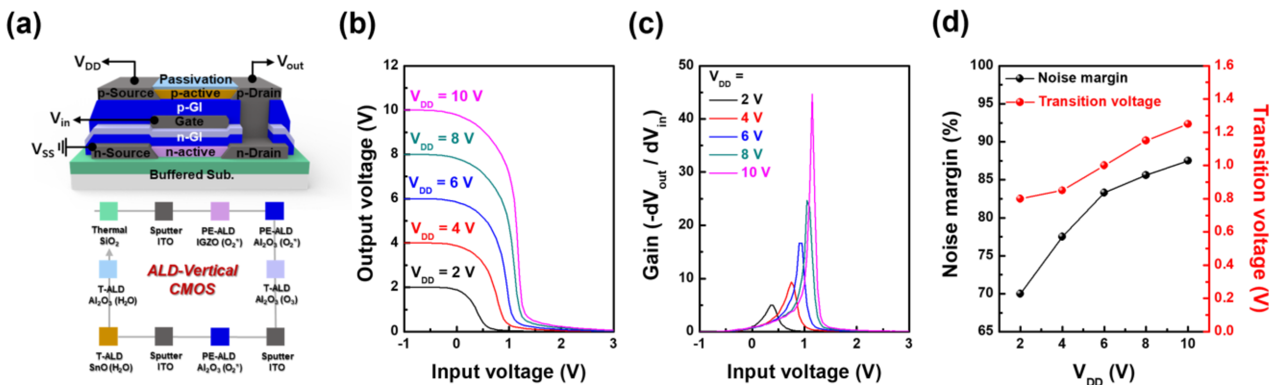

Figure 7. (a) Schematic illustration of vertically stacked CMOS inverter and fabrication process. (b) VTCs and (c) voltage gain of vertical CMOS inverter as a function of Vin with increasing V_{DD}. (d) Noise margin and transition voltage versus V_{DD}.

Acknowledgements

This research was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (No. RS-2023-00260527). This work was also supported by the industry technology R&D program (20017382 and 20006400) funded By the Ministry of Trade, Industry & Energy (MOTIE, Korea).

6. References

[1] Kim HM, Kim DG, Kim YS, Kim M, Park JS. Atomic layer deposition for nanoscale oxide semiconductor thin film transistors: review and outlook. International Journal of Extreme Manufacturing. 2023 Feb 3;5(1):012006.

[2] Si M, Lin Z, Chen Z, Sun X, Wang H, Ye PD. Scaled indium oxide transistors fabricated using atomic layer deposition. Nature Electronics. 2022 Feb 21;5(3):164–70.

[3] Lee S, Chen Y, Kim J, Jang J. Vertically integrated, double stack oxide TFT layers for high-resolution AMOLED backplane. Journal of the Society for Information Display. 2020 May 4;28(6):469–75.

[4] de Jamblinne de Meux A, Bhoolokam A, Pourtois G, Genoe J, Heremans P. Oxygen vacancies effects in a-IGZO: Formation mechanisms, hysteresis, and negative bias stress effects. physica status solidi (a). 2017 Mar 2;214(6):1600889.

[5] Kim T, Choi CH, Hur JS, Ha D, Kuh BJ, Kim Y, et al. Progress, Challenges, and Opportunities in Oxide Semiconductor Devices: A Key Building Block for Applications Ranging from Display Backplanes to 3D Integrated Semiconductor Chips. Advanced Materials. 2022 Jul 21;2204663.

[6] Choi SH, Ryu SH, Kim DG, Jae-Hyeok Kwag, Yeon C, Jung J, et al. *c*-Axis Aligned 3 nm Thick In_2O_3 Crystal Using New Liquid DBADMIn Precursor for Highly Scaled FET Beyond the Mobility–Stability Trade-off. Nano Letters. 2024 Jan 17;24(4):1324–31.

[7] Masataka Shiokawa, Kouhei Toyotaka, Masashi Tsubuku, Sugimoto K, Nakashima M, Matsuda S, et al. P-26: A 1058 ppi 8K4K OLED Display using a Top-Gate Self-Aligned CAAC Oxide Semiconductor FET. SID Symposium Digest of Technical Papers. 2016 May 1;47(1):1209–12.

[8] Shishido H, Shuichi Katsui, Kobayashi H, Nakagawa T, Tamatsukuri Y, Shogo Uesaka, et al. 21-1: *Invited Paper:* 5291-ppi Microdisplay Using CAAC-IGZO FET with Channel Length of 60 nm. Sid's Digest Of Technical Papers. 2020 Aug 1;51(1):293–6.

[9] Shuichi Katsui, Kobayashi H, Nakagawa T, Tamatsukuri Y, Shishido H, Shogo Uesaka, et al. A 5291-ppi organic light-emitting diode display using field-effect transistors including a c-axis aligned crystalline oxide semiconductor. Journal of the Society for Information Display. 2019 Jun 26;27(8):497–506.

[10] Johnson RW, Hultqvist A, Bent SF. A brief review of atomic layer deposition: from fundamentals to applications. Materials Today. 2014 Jun;17(5):236–46.

[11] George SM. Atomic Layer Deposition: An Overview. Chemical Reviews. 2010 Jan 13;110(1):111–31.

[12] Kim Y, Oh H, Kim J, Lim JH, Park J. Approaches for 3D Integration Using Plasma-Enhanced Atomic-Layer-Deposited Atomically-Ordered InGaZnO Transistors with Ultra-High Mobility. Small Methods. 2023 Jun 28;7(10).

[13] Kim HM, Lee WB, Koo H, Kim SY, Park JS. Controlled 2D growth approach *via* atomic layer deposition for improved stability and performance in flexible SnO thin-film transistors. Journal of Materials Chemistry C. 2024 Jan 1;12(23):8390–7.

[14] Kim DG, Choi SH, Lee WB, Jeong GM, Koh J, Lee S, et al. Highly Robust Atomic Layer Deposition-Indium Gallium Zinc Oxide Thin-Film Transistors with Hybrid Gate Insulator Fabricated via Two-Step Atomic Layer Process for High-Density Integrated All-Oxide Vertical Complementary Metal-Oxide-Semiconductor Applications. Small Structures. 2023 Nov 21;5(2).

[15] Han H, Jang S, Kim D, Kim T, Cho H, Shin H, et al. Memory Characteristics of Thin Film Transistor with Catalytic Metal Layer Induced Crystallized Indium-Gallium-Zinc-Oxide (IGZO) Channel. Electronics. 2021 Dec 24;11(1):53.

[16] Jeong H, Kim YS, Jeong SG, Park J. Impact of Annealing Temperature on Atomic Layer Deposited In–Ga–Zn–O Thin-Film Transistors. ACS Applied Electronic Materials. 2022 Mar 1;4(3):1343–50.