A Novel Fabrication Process for Enhancing the Reliability of IGZO Thin Film Transistor

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Abstract

This study presents the impact of IGZO/GI interface contamination and carrier fluctuations within IGZO due to the fabrication process of indium gallium zinc oxide (IGZO) thin-film transistors (TFTs) with a top-gate structure. To address these challenges and improve device reliability, a novel island-shaped gate-insulated (I-GI) structure, passivated with a silicon oxide (SiO_x) thin film, is proposed. Experimental results show that the I-GI structure significantly enhances both electrical stability and reliability compared to the conventional reference structure. The newly developed design demonstrates substantial improvements in device stability under various operational conditions. These results confirm that the I-GI structure effectively reduces front-channel contamination while preserving the carrier concentration within the IGZO layer, ensuring consistent and reliable device performance without fluctuations during the fabrication process.

Author Keywords

Oxide TFT; IGZO; Island gate insulator; Silicon oxide thin film; Coplanar;

1. Introduction

Oxide semiconductor devices are increasingly used as thin-film transistors (TFTs) in various displays, including those in watches, mobile phones, and televisions, owing to their high electron mobility, low off-current, and consistent performance. Additionally, with the growing demand for high-end display panels, there has been active research into high-mobility oxide semiconductors and the development of highly reliable oxide semiconductors. [1-4] Nevertheless, despite these numerous advantages, oxide semiconductors remain a limited alternative to low-temperature polycrystalline silicon (LTPS) devices due to their sensitivity to hydrogen and oxygen. These elements can function as donors and charge compensators in the IGZO layer, thereby influencing the properties of TFTs. While oxide semiconductors, such as IGZO, offer several performance advantages, their susceptibility to environmental factors presents significant challenges in achieving long-term reliability in TFT applications. [5-7]

This study investigates the impact of contamination at the interface between the IGZO channel layer and the GI interface during the TFT fabrication process. To address this issue, a novel structure was proposed and implemented to prevent contamination at the IGZO/GI interface. The study analyzes the resulting changes in the electrical properties and behavior of the TFT devices while investigating fundamental improvements in device performance.

2. Methods

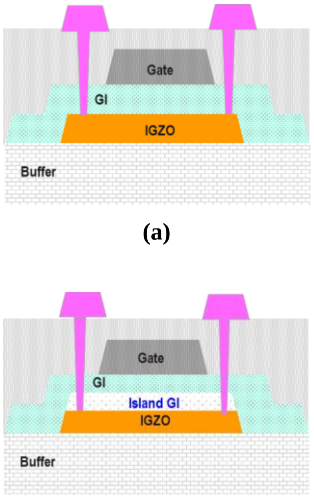
2.1 Hypothesis and Experimental Method

As previously mentioned, oxide semiconductors are highly sensitive to hydrogen and oxygen, which can induce carrier concentration fluctuations within the IGZO layer. Consequently, minimizing their ingress during the fabrication process and preserving the as-deposited state of the IGZO thin film are critical for maintaining stable TFT characteristics. [8,9] In this context, we hypothesize that post-deposition patterning processes disrupt this balance by increasing hydrogen ingress and oxygen vacancy formation, while also altering device characteristics due to contamination at the IGZO/GI interface.

To test this hypothesis, we conducted the following verification experiments. First, we fabricated I-GI structure TFTs designed to mitigate interface contamination and evaluated their characteristics without annealing processes. Additionally, we modified the GI deposition conditions to promote an increase in carrier concentration within the IGZO layer and observed the resulting changes in the device's threshold voltage (Vth) characteristics. Finally, device reliability was evaluated under conditions with a clean IGZO/GI interface, enabling a comprehensive assessment of the impact of interface contamination on device performance and stability.

2.2 New TFT Structure and Fabrication Process

To investigate the impact of contamination at the IGZO/GI interface, two types of TFTs were fabricated. The first was a conventional top-gate coplanar structure, while the second was an island-shaped gate-insulated (I-GI) structure, passivated with a silicon dioxide (SiO_x) thin film after IGZO deposition. The structure of the fabricated TFTs is shown in Figure 1.



(a)

(b)

Figure 1. Presents different structures for thin-film transistors (TFTs): (a) shows the reference structure for top-gate coplanar TFT; (b) illustrates an island-shaped gate-insulated (I-GI) structure TFT.

The I-GI layer, formed from a 10 nm-thick SiO_x thin film, was deposited using a conventional plasma-enhanced chemical vapor deposition (PECVD) process. To minimize potential confounding factors unrelated to structural differences from the reference device, the PECVD parameters used for the deposition of the I-GI layer were kept identical to those employed for the reference TFT's gate insulator.

The I-GI structure was fabricated in the following sequence. After depositing the IGZO thin film, the I-GI layer was applied, followed by photolithography using the active layer photomask. To achieve consistent device characteristics during the etching process for pattern formation, it is crucial to form a proper taper. At this stage, the etch selectivity ratio between the I-GI layer, the SiO_x thin film, and the IGZO layer was carefully adjusted to ensure the proper taper. Fig. 2 (a) presents the Transmission Electron Microscope (TEM) cross-sectional analysis results.

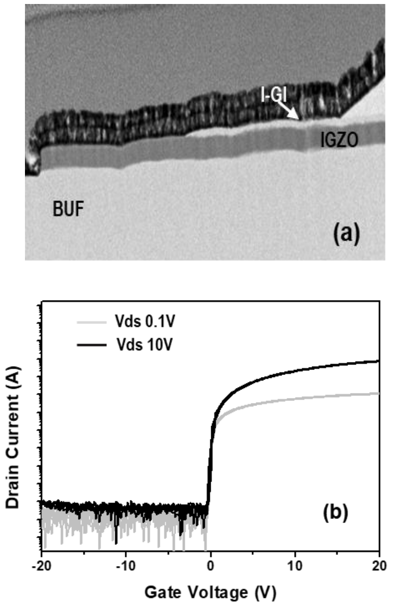


Figure 2. (a) TEM cross-sectional Image of channel region and (b) Transfer Characteristics of island-shaped gate-insulated (I-GI) TFT.

Subsequently, the main GI layer, with a thickness of 140 nm, was deposited under the same conditions as the I-GI layer. The remaining process steps were then identical to those of the control group device, ensuring consistency and minimizing variation in TFT characteristics due to factors other than structural differences. Fig. 2 (b) shows the transfer curve characteristics of the I-GI structure TFT fabricated by the described process.

3. Results

3.1 Impact of I-GI Structure on Vth Stability

Here, to examine the changes in device characteristics, the annealing process was excluded for both device structures. The annealing process in IGZO TFTs is a critical compensation procedure, commonly used for hydrogen degassing and defect curing. As shown in Fig. 3, for the reference device without annealing process, the threshold voltage shifts negatively, and the variation increases. In contrast, the I-GI structure device exhibits stable and uniform Vth characteristics.

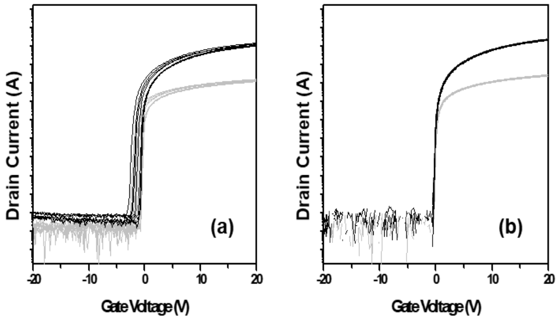


Figure 3. Transfer curves of (a) reference TFT, (b) I-GI TFT without annealing process.

The transfer characteristics reveal that the Vth variation occurs due to an increase in carrier concentration within the IGZO layer during the fabrication process. Furthermore, it can be observed that excluding the annealing process makes it difficult to control the increase in hydrogen and oxygen vacancies within the IGZO, which are induced during fabrication. In contrast, the results in Fig. 3(b) demonstrate that these fluctuations are effectively suppressed by the I-GI structure. These results indicate that the I-GI structure can effectively control variations in carrier concentration within the IGZO layer.

Next, we increased the SiH_4 gas flow during the GI deposition to promote the influx of hydrogen radicals into the IGZO layer, thereby artificially altering the carrier concentration. We then observed the resulting variations in Vth characteristics for each TFT structure under these conditions, as shown in Fig.4.

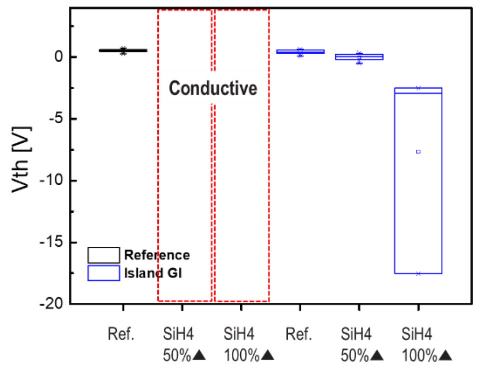


Figure 4. Variation in Vth characteristics with fluctuations in SiH_4 gas flow during GI deposition.

As a result, in the I-GI structure, despite the increase in SiH_4 gas flow, the shift in Vth towards a more negative value (indicating an increase in carrier concentration in the active layer) was less pronounced compared to the reference structure. As with the previous results, this suggests that the I-GI structure is more effective in maintaining carrier concentration within the active channel layer, thereby enhancing the stability of the initial device characteristics. Furthermore, it demonstrates that the I-GI structure facilitates the fabrication of devices that exhibit greater robustness against variations introduced during the fabrication process.

3.2 Reliability Improvement

Based on the previous evaluations, which confirmed that device variations are induced by processes following IGZO deposition, we assessed whether the I-GI structure improves device reliability. Fig. 6. presents the reliability results for positive bias temperature stress (PBTS) and negative bias illumination stress (NBTiS) for both structures. The PBTS conditions were 100°C, Vgs = 30V, Vds = 0V, and 1 hour of stress. The PBTS results show a significant improvement in the I-GI structure's PBTS characteristics compared to the reference device. This improvement is attributed to the ingress of excess oxygen into the IGZO layer during the compensation process, which is hypothesized to serve as a carrier trap site at shallow levels, leading to the degradation of the PBTS characteristics in the reference device.[10] Additionally, the implementation of the I-GI structure demonstrates effective control of defects at the GI interface.

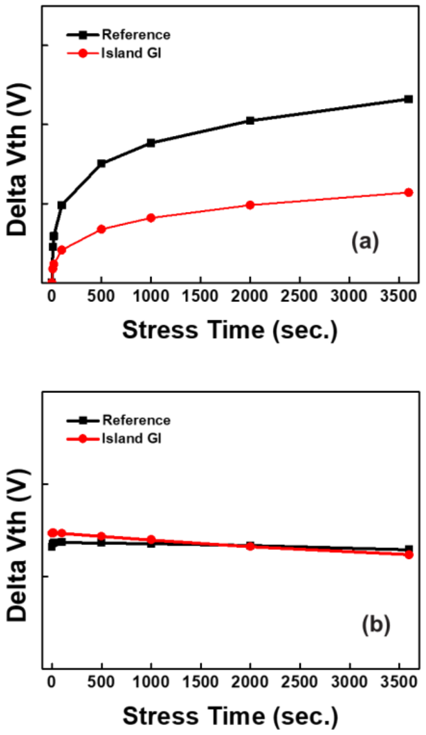


Figure 6. Compare the reference and I-GI TFT with delta Vth after (a) PBTS and (b) NBTiS conditions.

Conversely, hydrogen within IGZO serves both as a donor, generating carriers, and as a defect passivation by forming OH bonds, which reduces deep-level defects. As confirmed by the previous experimental results, an appropriate amount of hydrogen influx improves PBTS characteristics through defect passivation. However, excessive hydrogen influx acts as a donor, leading to fluctuations in the initial threshold voltage (Vth) and degrading the NBTiS characteristics. Therefore, to accurately assess the improvement in reliability, it is essential to evaluate both PBTS and NBTiS characteristics, as shown in Fig. 6 (b). The NBTiS conditions were 60°C, Vgs = -30V, 4500nits, and 1 hour of stress. The results demonstrate that the NBTiS characteristics of both the I-GI and reference devices are comparable, further confirming that the I-GI structure effectively maintains an optimal balance of hydrogen and oxygen within the IGZO layer.

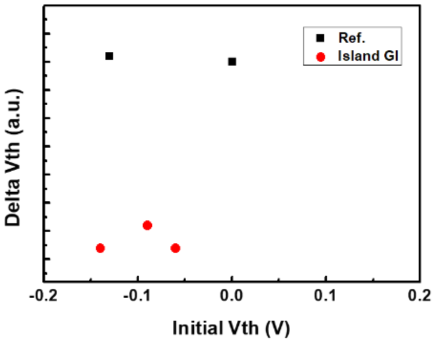


Figure 7. Delta Vth of the reference and I-GI structures under current stress.

Finally, a current Stress (CS) evaluation was conducted to examine the differences in the IGZO/GI interface characteristics between the two structures. The CS evaluation was conducted for 12 hours under the conditions of 60°C, Vds 5V, and a current of 200nA.

As shown in Fig. 7, while both structures exhibited similar initial Vth characteristics, the I-GI structure demonstrated a significant improvement in CS characteristics. This demonstrates that the I-GI structure not only suppresses carrier fluctuations caused by the influx of hydrogen/oxygen but also shows resilience against carbon and organic contamination during the photolithography, wet etching, and stripping processes.

4. Conclusion

In this paper the impact of IGZO/GI interface contamination and carrier fluctuations within IGZO during the fabrication process of oxide semiconductor thin-film transistors was investigated. The experimental results demonstrated that the I-GI structure exhibited significantly improved stability in both electrical characteristics and reliability compared to the conventional reference structure. Passivating the IGZO layer with the SiO_x thin film proved effective in controlling the ingress of hydrogen and oxygen during subsequent processing, maintaining the carrier concentration within the IGZO layer in its as-deposited state and minimizing fluctuations in Vth. The results of this study suggest that the passivated IGZO layer in the I-GI structure offers a promising solution for improving the long-term stability and performance of oxide TFTs, thereby contributing to the advancement of high-reliability, high-mobility oxide semiconductors.

5. References

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