# Stacked Vertical Oxide TFTs for Ultra-High Resolution Display

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## Abstract

***AR/VR devices demand ultra-high-resolution displays to accommodate a wide field of view (FOV) and high pixels per degree (PPD). Stacked vertical channel TFTs, which combine vertical channel TFTs with a stacked structure, offer a backplane solution that meets these requirements. By optimizing the structure and process integration, the device characteristics of stacked vertical channel TFTs were well controlled. Using this technology, a pixel design supporting 3500 PPI with a 4T1C configuration was developed.***

## Author Keywords

vertical channel TFTs; stacked TFTs; oxide TFTs; ultra-high resolution display; AR/VR display.

## 1. Introduction

Recently, AR/VR devices designed for metaverse applications have garnered significant attention. One of the key components of these devices is the display panel, as its specifications are closely tied to the image quality of AR/VR experiences. Critical factors such as field of view (FOV) and screen door effects depend on the display's performance. It is generally understood that a 100-degree FOV is necessary to fully cover the user's vision, while 60 pixels per degree (PPD) are required to deliver clear imagery equivalent to 20/20 vision [1].

A combination of a large FOV and high PPD necessitates an ultra-high-resolution display panel. For instance, achieving a 100-degree FOV and 60 PPD requires a 6K resolution display panel. However, the display size must be minimized to ensure a compact form factor and lightweight design for AR/VR devices. Typically, the diagonal size of an AR display panel is less than 1 inch, while that of a VR display panel ranges from 1 to 2 inches. To meet the general goals of AR/VR displays—large FOV, high PPD, and small size—a display panel with extremely high pixel density is essential.

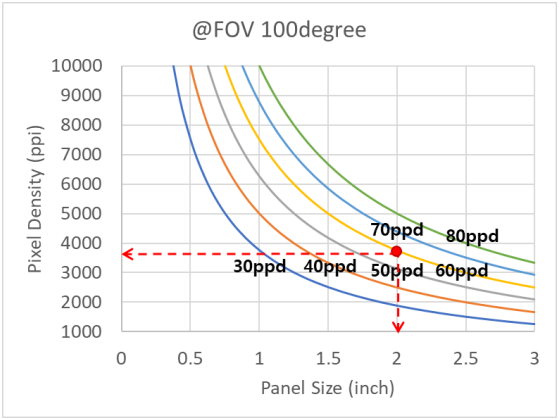


**Figure 1.** The relationship between pixel density and panel size for various PPDs, under the constraint of a 100-degree field of view (FOV).

For example, as shown in Fig. 1, achieving a 100-degree FOV, 60 PPD, and a 2-inch diagonal size requires a display panel with an exceptionally high pixel density of 3500 PPI.

In this paper, we propose a novel structure for a TFT backplane designed to achieve 3500 PPI, incorporating a compensating pixel circuit using a 4T1C configuration. Additionally, we will discuss the technical challenges associated with this innovative structure.

## 2. Non-planar TFTs for ultra high-resolution Display

Typically, the channel direction of TFTs is parallel to the substrate of the display panel, and only a single channel layer is present. Such structures are referred to as planar TFTs, which include bottom-gate BCE (back-channel etch) structures and top-gate SA (self-aligned) structures. In these designs, increasing the density of TFTs inevitably requires reducing the critical dimensions, including the channel length. However, this approach is constrained by the technical limits of lithography tools, which impose restrictions on the achievable pixel density in planar backplane structures.

Non-planar TFTs can overcome these technical limitations, enabling the fabrication of ultra-high-density display panels. One approach to non-planar TFTs is the adoption of vertical channel structures [2]. Vertical channel TFTs significantly reduce the footprint of TFTs, as the channel region occupies almost no surface area. Another approach involves stacking TFTs on top of each other [3]. Ideally, stacking TFTs *n*-times can reduce the total area to one-*n*th of its original size.

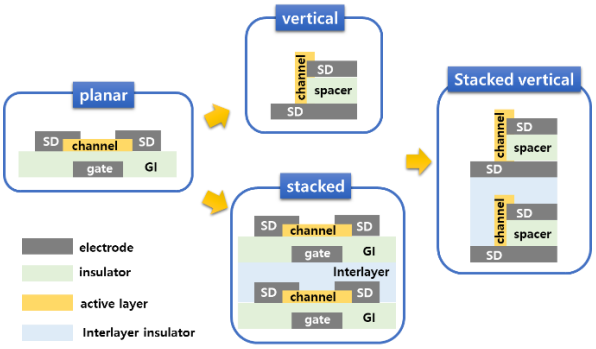


**Figure 2.** The concept of a non-planar TFT structure.

These two approaches can be combined to maximize the footprint reduction in non-planar TFTs [4]. Stacked vertical TFTs may be the most efficient structure for providing backplanes for ultra-high-density displays. However, the complexity of the structure and the process coupling between each layer of TFTs must be carefully optimized.


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## 3. Development of stackable vertical channel TFTs

The essential components of vertical channel TFTs include the vertical channel between the bottom and top source-drain electrodes, and the gate stack (comprising the gate insulator and gate electrode) that covers the vertical channel. However, there are several variations of vertical channel TFTs. These structures can be categorized based on the number of masks used, as shown in Fig. 3.

In a 3-mask process, only the bottom and top source-drain masks, along with the gate mask, are required to fabricate vertical channel TFTs. The gate insulator and active layer are defined by the gate mask. While the 3-mask process is relatively simple, the large overlap between the gate electrode and the active layer can lead to high parasitic capacitance, and gate leakage currents may occur due to the overlap.

The 4-mask process mitigates gate leakage currents by introducing patterning of the active layer before depositing the gate insulator. A key challenge in the 4-mask process is the patterning of both the active layer and the gate electrode layer. Since these layers are deposited on a step geometry, residual material remains after the dry etching process.

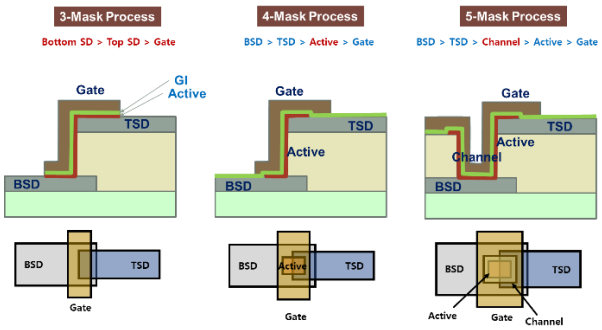


**Figure 3.** The types of vertical channel TFTs based on the number of masks used in the fabrication process.

The introduction of a hole-type pattern (shown as the ‘channel’ region in Fig. 3) can address this issue, as patterning of the active layer and gate electrode can be performed on the flat regions.

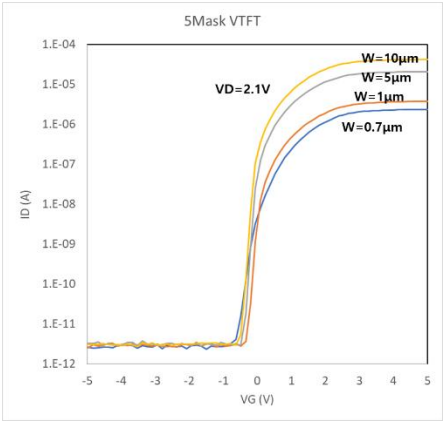


**Figure 4.** The typical transfer characteristics of vertical channel TFTs fabricated using a 5-mask process.

Another advantage of the 5-mask process is the absence of a global step geometry in the structure. This feature is crucial for process integration in stacked vertical TFTs.

The typical transfer characteristics of vertical channel TFTs fabricated using the 5-mask process are shown in Fig. 4. TiW metal was used for the source-drain layer, while an ALD-deposited IGZO layer was used for the channel. The gate electrode was made from a PEALD-deposited alumina layer and TiW metal. The threshold voltages and leakage currents were well controlled for TFTs with various widths and a channel length of 0.3 μm.

## 4. Stacked vertical channel TFTs

As a proof of concept for stacked vertical channel TFTs, a simple 2T-1C type AMOLED pixel array was fabricated, as shown in Fig. 5 [4].

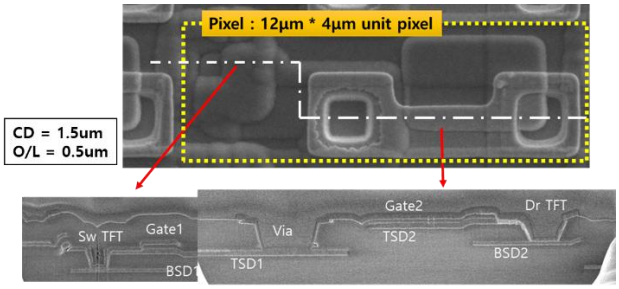


**Figure 5.** The cross-sectional SEM images of a 2T-1C pixel composed of stacked TFTs.

The pitch of the pixel array was 12 μm by 4 μm, corresponding to a pixel density of 2000 PPI. The 5-mask process vertical TFTs were successfully integrated into the stacked structure.

One of the key considerations in the stacking process is optimizing the thermal procedure for the bottom and top vertical TFTs. Given the very short channel length of vertical channel TFTs, the channel area can easily transform into a conductive layer due to the influence of external dopants. Therefore, the thermal budget for the top vertical TFTs must be reduced to prevent the diffusion of dopants into the active layer of the bottom vertical TFTs. However, lowering the process temperature may negatively affect the quality of the dielectric layer. The film quality of the dielectric layer between the top and bottom source-drain electrodes is crucial, as it interfaces with the back-channel of the active layer..

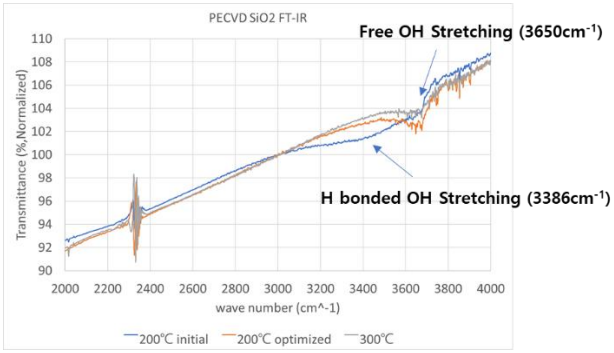


**Figure 6.** The optimization of the SiO2 dielectric layer deposited at a low temperature of 200°C.

The film quality of the SiO2 dielectric layer, deposited at low temperature, was improved through the optimization of deposition conditions. As shown in Fig. 6, the characteristics of the OH bond in SiO2 films for the optimized low-temperature deposition were similar to those of films deposited at typical temperatures.

The characteristics of the fabricated stacked vertical TFTs are shown in Fig. 7. Despite the different thermal budgets (300°C for the bottom vertical TFT and 200°C for the top vertical TFT), the threshold voltages of each vertical TFT showed a nearly identical distribution.

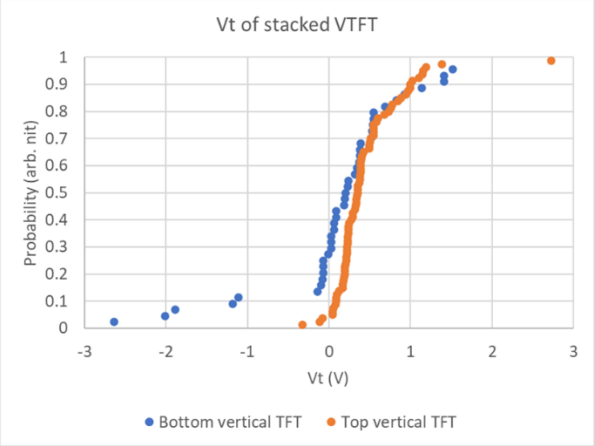


**Figure 7.** The comparison of the characteristics between the bottom vertical TFT and the top vertical TFT.

To achieve an ultra-high-resolution display with stacked vertical channel TFTs, a 3500 PPI AMOLED pixel array with compensating pixel circuits has been developed.

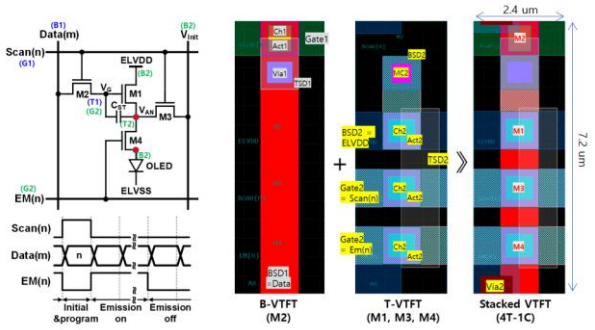


**Figure 8.** The schematic of the 4T1C pixel circuit, along with the timing diagram and layers of stacked vertical TFTs.

Due to the very small footprint of vertical channel TFTs and the stacking of TFTs, the 4T1C pixel circuits are designed with a pixel pitch of 7.2 µm by 2.4 µm, corresponding to a pixel density of 3500 PPI, as shown in Fig. 8. In Fig. 8, M2 is designed as the bottom vertical TFT, while M1, M3, and M4 are designed as top vertical TFTs to optimize wiring efficiency.

The 3D images of the designed stacked vertical TFTs are shown in Fig. 9. The electrodes corresponding to scan, data, ELVDD, EM, and Vinit can be identified. The red cylinder represents the channel region, composed of the active layer, gate insulator, and gate layer inside the hole structure. Vias connecting the top and bottom vertical TFTs are also depicted as grey cylinders.

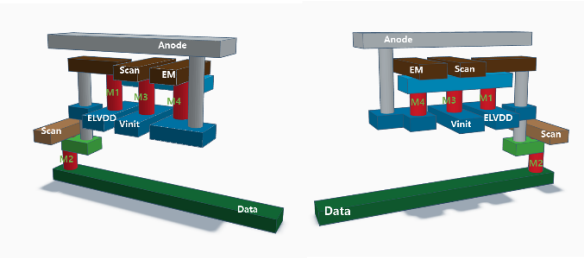


**Figure 9.** The 3D images of the 4T1C pixel design from two different viewpoints.

A 3500 PPI pixel array with stacked vertical TFTs was fabricated, as shown in Fig. 10. The detailed fabrication results and pixel characteristics will be presented at DW 2025.

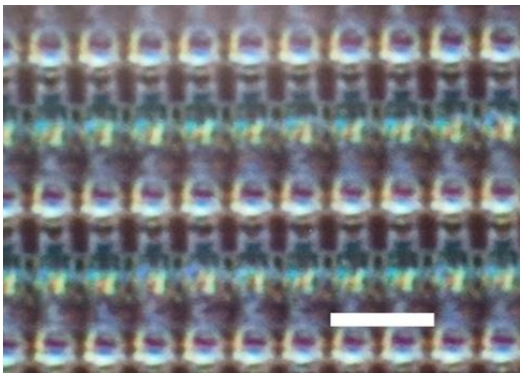

**Figure 10.** Top-view image of the fabricated 3500 PPI pixel array. The scale bar in the image represents 5 µm.

## 5. Conclusions

The non-planar TFT structure, including vertical channel TFTs and stacked TFTs, represents a breakthrough for achieving high pixel density. Stacked vertical TFT structures are presented as a novel backplane solution to realize ultra-high-resolution displays in a compact area. The 5-mask process vertical TFT and optimized thermal budget process integration address the technical challenges associated with stacked vertical TFTs. A 2000 PPI 2T1C pixel array has been fabricated, demonstrating the concept of stacked vertical TFTs. As part of the development for ultra-high-resolution displays, a 3500 PPI 4T1C pixel array has been designed, and the fabrication results will be presented.

## 6. Acknowledgements

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## 7. References

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