Ultra-High Output Current of Oxide Vertical TFTs Using a-IGZO by Sputter

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Abstract

The vertical channel structure thin film transistors (V-TFTs) have caused the widespread attention to achieve high output current and small footprint simultaneously. To establish the vertical channel architecture, it is critical to control dry etch process of spacer between source and drain layer. In this work, the taper angle of spacer shows approximately 70 to 85° by optimizing the photo and dry process, which is the base layer of the semiconductor channel. By adopting the plasma treatment, the device equivalent mobility is above 80 cm2/Vs with channel length 0.5um. Besides, the △Vth under the positive bias stress of 20V and negative bias temperature illumination stress of -20V for 1 h is +0.49V and -1.69V, respectively. The 4inch 90 x 100 (x RGB) mini-LED display driven by a-IGZO V-TFTs has demonstrated.

Keywords

Vertical channel; Sub-micro length; high on-state current; low leakage

1. Introduction

The ultra-high-resolution display is in demand as virtual reality (VR) and augmented reality (AR) displays, and hologram display become much more widespread [1]. Low power consumption is a necessity for extended reality applications such as the Internet of Things (IoT) and mobile applications. Low operation voltage is crucial for low power operation, as power consumption is inversely proportional to the square of the operation voltage. For such active matrix displays driven by thin-film transistors (TFTs), the most effective way to reduce power consumption is to increase the output current. In conventional planar TFTs with a metal-insulator-metal (MIS) structure, the effective ways to reduce the operation voltage include decreasing the thickness of the gate insulator and using a high dielectric-constant material. Both strategies increase the induced charge in the channel by the gate voltage, resulting in a decrease of the threshold voltage of the TFT and enabling low voltage operation [2].

The vertical oxide thin-film transistor (V-TFT) is an innovative structure that offers unique advantages over conventional planar TFT structures involved with high current and small footprint simultaneously. V-TFTs are independent of the requirements for high-precision photolithography, and the channel length can be precisely controlled by adjusting the thickness of the deposited film (spacer layer), allowing for sub-1 μm channel lengths [3]. This independence reduces significant costs associated with high-precision photolithography.

Recent developments in V-TFT technology have focused on optimizing the structural design, selecting appropriate gate dielectric layer materials, and optimizing the active layer [4-7]. For example, Oh et al. have conducted multiple research works on V-TFT prepared with IGZO as the active layer, including depositing two different types of IGZO films in the vertical sidewall by adjusting the super cycle ratio of atomic layer deposition (ALD) to change the In, Ga, and Zn elements in IGZO, forming a double active layer [7]. This approach has significantly reduced the threshold voltage drift of the double active layer compared with that of the single active layer.

Until now, there are very few reports about the output current improvement and display backplane driving towards V-TFT architecture in large size substrate. In this device preparation, not only a-IGZO is deposited by the sputter rather than ALD, but also other materials and equipment are commonly employed in the fabrication of display backplanes. Moreover, the improvements on profile of vertical sidewall and the output on-state current of device have conducted to obtain superior electrical properties. Finally, the transfer and driving backplane characteristics of V-TFTs also have been systematically discussed.

2. Experiment and Method

In this work, the a-IGZO V-TFTs were conducted on a Gen 4.5 glass substrate. The fabrication process is as follows. Firstly, the source electrode was deposited by sputtering and patterned on substrate. Next, 500 nm plasma enhanced chemical vapor deposition (PECVD) SiO_2 was deposited as inter-layer dielectric (ILD) between source and drain electrode. By adopting magnetron sputter and photolithograph fabricated as the drain electrode. Subsequently, the vertical sidewall is defined down to the source electrode by using the drain electrode pattern as the self-algin etching of ILD layer. Afterward, the a-IGZO was deposited by magnetron sputtering using a ceramic target (In: Ga: Zn = 1:1:1 mol%) at room temperature as active area. The active area was patterned using wet etching. A gate insulating layer (GI) is deposited by PECVD and a gate electrode is formed through sputtering and photolithography. Passivation (PV) layer was formed, which is employed as a protection layer to prevent the diffusion of H2O and O2 molecules to active layer. Finally, the pixel electrode was sputtered and patterned. Based on this, the IGZO V-TFT with the channel length 0.5um has been prepared, which the schematic diagram is shown in Figure 1. Keithley 4200-SCS semiconductor parameter analyzer was used to measure device electrical properties in the dark under ambient condition.

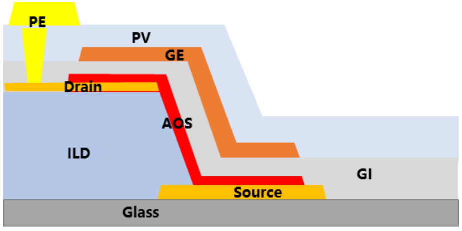

Figure 1. The schematic diagram of a-IGZO TFTs with vertical channel structure

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3. Results and Discussion

3.1 Optimization of ILD dry etch process

As the most important process of vertical structure, ILD etching to form vertical sidewalls is exceptionally critical. Most importantly, it not only determines the channel length, but also its uniformity across the G4.5 substrate. The taper shape of ILD sidewall and profile of V-TFT are illuminated by a scanning electron microscope (SEM), as shown in the Figure 2. The photo resistance (PR) setback at the interface of PR and ILD is more pronounced from the Figure 2(a). What's worse, the taper angle shows about 60 degree，which seems not steep and leads to the inferior uniformity of channel length. Consequently, the final profile of V-TFT as shown in the Figure 2(b). The channel of device shows a double step resulting from the bisection angle of ILD etching profile.

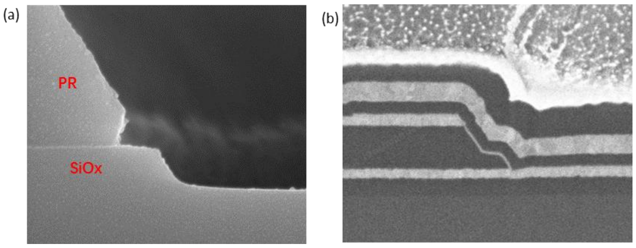


Figure 2. SEM cross-section profile of(a) ILD/PR and (b) a-IGZO V-TFT.

Further, the dry etching selective ratio of PR to SiOx also needs to optimize to obtain the steep sidewall of ILD. However, during the dry etching process, the PR pattern profiles may inevitably become rougher, and the line edge roughness of the PR pattern may be easily transferred to the surface of the ILD sidewall, which is the back channel interface of V-TFT. Besides, the roughness of the sidewall is more difficult to quantify by atomic force microscope (AFM), etc., because the region is vertical and its area is small. To ensure the steep profile of sidewall, the photo and dry etching process of ILD, focused on improving the PR taper and etching selective ratio, has optimized. Moreover, the sidewall surface treatment also has conducted after dry-etching. Figure 3 illustrates the cross-section profile of the V-TFT after the process improvement. The taper of sidewall is approximately 70 to 85° with the channel length 0.5um.

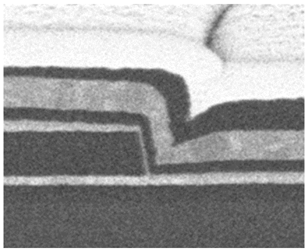


Figure 3. SEM cross-section image of reforming profile of a-IGZO V-TFT.

3.2 The electric characteries of V-TFT

Transfer curves and on-state current of device which were measured at different sites of test element groups on Gen. 4.5 glass is shown in Figure 4(a) and Figure 4(b) respectively. Figure 4(a) shows good subthreshold region characteristic (0.2±0.3V) and low off-state leakage current (10^{-13}~10^{-14}A). In the V-TFT, the magnitude of the off-state current depends on the density of the defect state in the back channel, which is related to the dry etching of the sidewall region and the deposition of the active layer [5]. As a result, the low leakage current illustrates that the relative smooth interface of sidewall region, which is attributed to the high etching process and treatment. The mobility of the above V-TFT device is about 7cm^2/Vs, which is higher than the reported work [8]. However, Figure 4(b) shows the uneven on-state current distribution on the different sites of the glass. For ultra-short channel devices such as V-TFT, the effect of contact resistance on current increases significantly as the channel length becomes shorter. The relatively low on-state current at most of the points is mainly due to the higher contact resistance in the source/drain region. Therefore, the output current of V-TFT needs to improve further to maximize the profit of submicron channel length involved with decreasing the contact resistance.

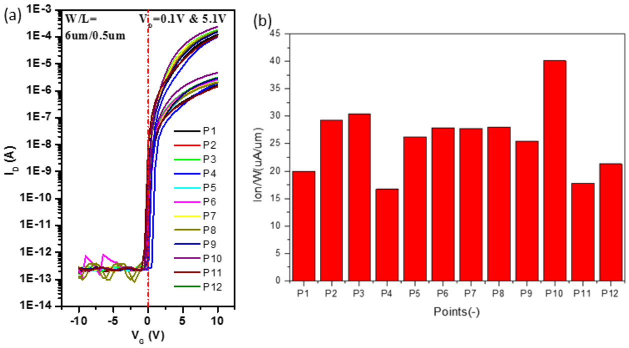


Figure 4. (a) Transfer characteristics and (b) the normalized on-state current of the conventional a-IGZO VTFTs.

3.3 On-state current improvement of V-TFT

To improve the on-state current of V-TFT, the contact area of source/drain and active layer has prepared by plasma treatment, which could remarkably decrease the contact resistance. Thus, an novel architecture of V-TFT has conducted to further improve the mobility to achieve the comparable level to top-gate self-aligned structure. The proposed V-TFT structure is shown in Figure 5 (a) and Figure 5 (b) illustrates the transfer curves measured at different sites on Gen. 4.5 glass and respectively. The renewed a-IGZO V-TFTs represent the mobility of around 10 cm^2/Vs with normalized current 44uA/um (Ion/W) and threshold voltage -0.30V±0.20V. It is underlined that the normalized current increases about 70% compared to the results showed in Figure 4(b)，which is about 7 times of the TGSA. In other words, from the magnitude of the output current of a-IGZO VTFT, the equivalent mobility of the device eventually reaches more than 80 cm^2/Vs. To evaluate TFT reliability, Figure 6 shows the shift of transfer curve for the a-IGZO V-TFTs under PBTS and NBTiS, respectively. Minor positive Vth shift (0.49 V) indicates that less electrons are trapped in the interface and gate insulator. The NBTIS is measured under Vg=-20 V at 60 ˚C for 1 hours with 4500 nits white light, which ΔVth is only -1.69 V.

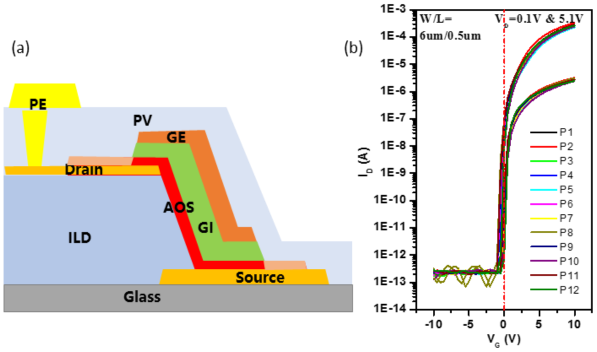


Figure 5. (a) The proposed novel architecture and (b) transfer characteristics of the novel a-IGZO VTFTs.

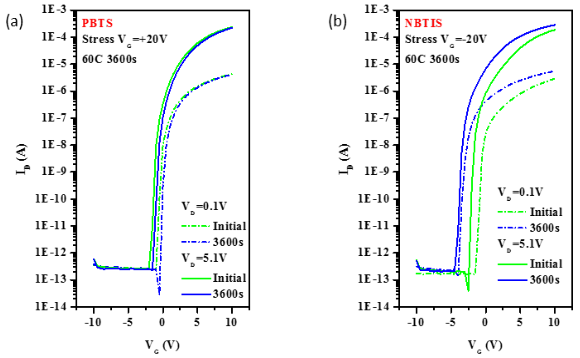
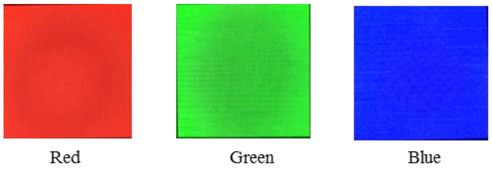


Figure 6. (a) The PBTS reliability (at dark after 3600s stress test at 60 ℃ when the Vg=+20 V) and (b) NBTIS reliability (at 4500nits after 3600s stress test at 60 ℃ when the Vg= -20 V) of the V-TFTs

Finally, the 4inch 90 (x gate) x 100 (x RGB) Mini-LED panel, which is driven by a-IGZO VTFTs with 3T1C pixel circuit, has been lighted successfully. Figure 7 shows the lighting result of three screens of red, green and blue respectively and the good illuminance uniformity.



Red Green Blue

Figure 7. Module lighting results of 4inch Mini-LED panel driven by a-IGZO VTFTs**.**

4. Conclusion

To achieve high equivalent mobility for high resolution display, we realized the feasibility of a submicron channel length in the vertical channel architecture with a-IGZO semiconductor deposited by sputter. In this structure, the sidewall profile of ILD has reformed to guarantee the uniformity of channel length and the quality of back-channel interface. Moreover, we improved the effective contact resistance among the semiconductor and source/drain by plasma treatment to maximize the output current. The transfer performance of V-TFT eventually achieve the desirable level, which equivalent mobility is over 80 cm^2/Vs and the mean Vth is -0.3V±0.20V. Vth shifts of only 0.49 and -1.69 V are attained with respect to 3600 s PBTS and NBTIS. Finally, the 4inch Mini-LED panel driven by V-TFTs shows the good illumination uniformity. In a word, we believe that the vertical channel structure would be a promising backplane for the product application to ultra-high-resolution display.

5. Acknowledgements

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6. References

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