Trifold OLED Display Fabricated Through Low-Temperature Process Using Short-Channel Top-Gate Self-Aligned Field-Effect Transistor with Crystal IO

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Abstract
We developed a low-temperature process for a top-gate self-aligned FET with L = 2 μm including a crystal indium oxide active layer, and achieved a field-effect mobility of 50 cm^2/Vs. Using this technology, we successfully fabricated the world's first trifold OLED display using crystal indium oxide.

Author Keywords
InO_x; Crystal Indium Oxide (Crystal IO); High mobility; Low-temperature process; Short channel; Foldable OLED display

1. Introduction
Recently, there have been various demands for displays with low power consumption, high resolution, large screen size, foldability, light weight, and high impact resistance. In view of this, backplane technologies using low-temperature polysilicon (LTPS), an oxide semiconductor (OS), and a low-temperature polycrystalline silicon and oxide (LTPO) have been developed. A flexible organic light-emitting diode (OLED) display is a technology that achieves foldability, light weight, and high impact resistance. We have developed flexible displays such as trifold displays and side-roll panels using *c*-axis aligned crystal indium gallium zinc oxide (CAAC-IGZO) for their active layers [1-4]. As the backplanes for commercialized flexible display panels, a laser lift-off technology using a polyimide (PI) separation layer has recently been employed. In the case where the PI separation layer is used, the process temperature of a field-effect transistor (FET) array must be lower than or equal to 450 °C; thus, the LTPS faces challenges such as initial threshold voltage (Vth) variations and deterioration in on-state characteristics and gate bias temperature (BT) reliability [5].

FETs containing OSs, in particular, IGZO, have excellent characteristics even when fabricated through a low-temperature process at 450 °C or lower. Thus, they are applicable to substrates with a wide range of sizes from G6 to G10 and are compatible with flexible devices. Since they have extremely low off-state currents [6] and short channel lengths, application to a wide range of mass-produced products such as smartwatches, smartphones, tablets, and TVs has been progressed. Moreover, they have an advantage of making the driving of pixel circuits simple because of no hysteresis influence. However, IGZO(111) which is generally used has a problem of low mobility as compared with LTPS. In order to solve the problem, LTPO [7], which combines the high mobility and reliability of the LTPS with the low off-state current of the OS, has been proposed and products including the LTPO have been commercialized. Nevertheless, the LTPO has drawbacks including a complicated process, a large number of steps, and high cost. Moreover, the process temperature of the LTPO is as high as that of the LTPS; thus, the LTPO is not compatible with flexible devices [8].

High-mobility OS materials, especially polycrystalline InO_x:H in which hydrogen is added during sputter deposition, have been researched and developed to effectively solve this problem. However, many previous studies reported the FETs having long channel lengths, normally-on characteristics, and insufficient reliability despite having high field-effect mobility [9-11]. When an FET containing InO_x:H achieves a low-temperature process, short channel, high field-effect mobility, normally-off characteristics, and high reliability, it can be a better alternative to LTPS or LTPO as the backplane technology applicable to flexible devices.

In view of this, drawing on our past knowledge and experience [12-19], we have developed a low-temperature process for a top-gate self-aligned (TGSA) FET using InO_x:H, which is deposited by sputtering, for an active layer; this process is applicable to large-sized glass substrates. We evaluated the electrical characteristics and gate BT reliability of the FET, and actually fabricated a trifold OLED display using the process.

2. Crystallinity of InO_x:H and TGSA FET Process
InO_x films with and without addition of hydrogen are deposited with a sputtering apparatus for G3.5-sized substrates. Figure 1 presents X-ray diffraction (XRD) analysis results of the InO_x films before baking and after baking at 150 °C and 400 °C. The films without addition of hydrogen are already crystalized after the deposition, whereas the films with addition of 5 % of hydrogen are not crystalized after the deposition. After baking at 150 °C or higher, a plurality of peaks indicating crystallinity are observed, which indicates that InO_x:H is polycrystallized. We call such crystallized InO_x:H a crystal indium oxide (IO).

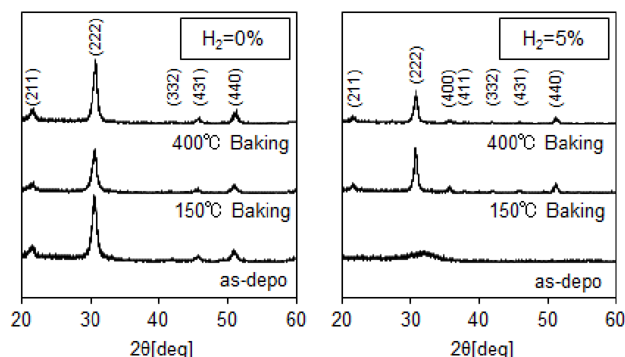

Figure 1. XRD analysis results (InO_x:H = 20 nm, sputter deposition)

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Figure 2 shows a schematic cross-sectional view of the fabricated TGSA FET including a crystal IO active layer. A separation layer is formed over a G3.5-sized glass substrate, and a bottom gate is formed thereover to offer a dual-gate structure. A bottom gate insulator (GI) film is deposited thereover with a plasma-enhanced chemical vapor deposition (PECVD) apparatus, the InO_x:H is deposited with a sputtering apparatus, the InO_x:H active layer is formed, and baking treatment at 400 °C is performed. After that, a top GI film is deposited with the PECVD apparatus, and then a top gate is deposited with the sputtering apparatus. After that, the top GI film is etched in a self-aligned manner with the top gate, and a passivation layer is deposited with the PECVD apparatus, whereby source and drain (S/D) regions of the active layer have n^+ type. After that, S/D contact holes are opened to form S/D wirings, and finally, a planarization layer is formed. The number of masks in this TGSA FET process is smaller than that in the LTPS FET process by approximately one and smaller than that in the LTPO FET process by approximately four. Thus, the TGSA FET process is simple and has cost advantages.

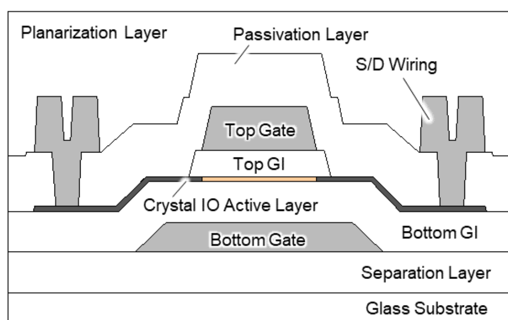
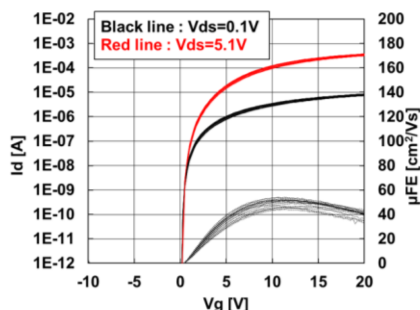


Figure 2. Schematic cross-sectional view of TGSA FET

3. Electrical Characteristics of Crystal IO TGSA FET

Figure 3 shows the drain current-gate voltage (Id-Vg) characteristics of the fabricated dual-gate TGSA FET with W/L = 3/2 µm. The bottom gate of the FET is electrically connected to the top gate. Even with a short channel length L of 2 µm, excellent Id-Vg characteristics with small variation are obtained. Vth is normally-off, and a linear field-effect mobility of 50 cm^2/Vs is achieved at a drain-source voltage (Vds) of 0.1 V. Note that the combined capacitance of the top GI and the bottom GI is used for the calculation of the field-effect mobility.



		Average	3σ
µFE [cm^2/Vs]	Vds=0.1V	50.0	8.9
Vth [V]	Vds=0.1V	0.46	0.08

Figure 3. Id-Vg characteristics (measured at 20 points in G3.5-sized substrate)

Figure 4 compares the Id-Vg characteristics of the fabricated crystal IO TGSA FET, a commercialized IGZO TGSA FET, and commercialized LTPS FETs. It is apparent from Fig. 4 that the fabricated crystal IO TGSA FET has a much higher on-state current than the commercialized LTPS FETs, while having an extremely low off-state current that is a feature of the OS.

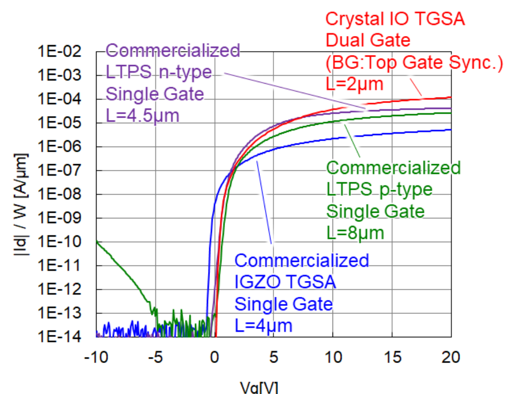


Figure 4. Comparison of on-state current (Vds = 5.1 V, Vgs = –10 V to 20 V. Id is normalized by channel width W. Positive and negative of Vgs of LTPS p-type FET are inverted.)

Figure 5 shows the results of positive bias temperature stress (PBTS) and negative bias temperature stress (NBTS) tests on the fabricated crystal IO TGSA FET and the commercialized IGZO TGSA FET. The PBTS and NBTS test results of the crystal IO TGSA FET are equivalent to those of the commercialized IGZO TGSA FET, and both FETs have excellent characteristics with almost no variations.

Thus, crystal IO TGSA FETs are probably widely applicable to driver circuits, pixel circuits, and other circuits of displays.

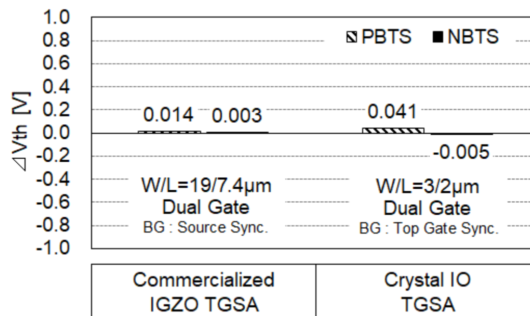


Figure 5. Gate BT test (Stress condition: Vg = ±2 MV/cm, Dark, 60 °C, 3600 sec)

Figure 6(a) shows comparison of the Id-Vg characteristics between before and after separation of the FET array from the glass substrate. There is no significant difference in Id-Vg characteristics between before and after the separation, which reveals that the FETs are hardly affected by the separation process. Figures 6(b) and 6(c) show comparison of the Id-Vg characteristics before and after inward and outward bending tests each performed on the FETs 100,000 times with a curvature radius R of 2 mm, and variations in Id-Vg characteristics are not observed after the bending tests performed in each bending direction 100,000 times. In a crystal IO including polycrystals,

the conditions of the crystal grain boundary are maintained even after the bending, indicating that the bending does not affect the characteristics.

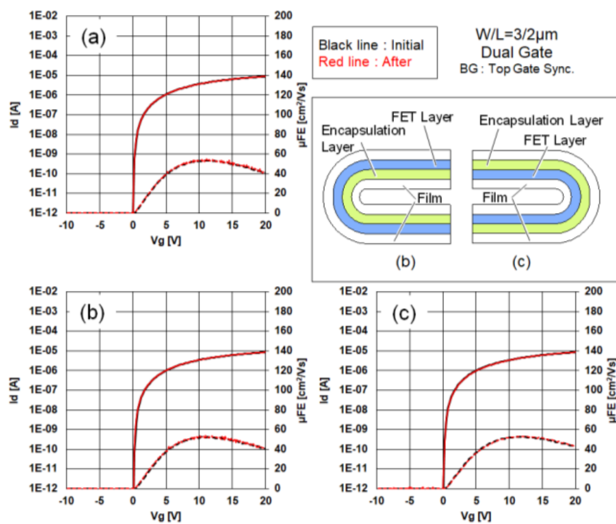


Figure 6. Id-Vg characteristics (a) before and after FET array separation, (b) before and after FET inward bending, and (c) before and after FET outward bending

(Vds = 0.1 V, Vgs = –10 V to +20 V)

Generally, LTPS is considered to have hysteresis problems. Thus, pixel circuits of OLED displays require an increase in the number of devices and input of complex signals to reduce the influence of hysteresis. Figure 7 shows hysteresis evaluation results of an LTPS p-type FET typically used for OLED displays, and the crystal IO TGSA FET. The crystal IO TGSA FET has Id-Vg curves almost overlapping with each other and has almost no hysteresis, which are advantageous for the circuit operation of OLED displays.

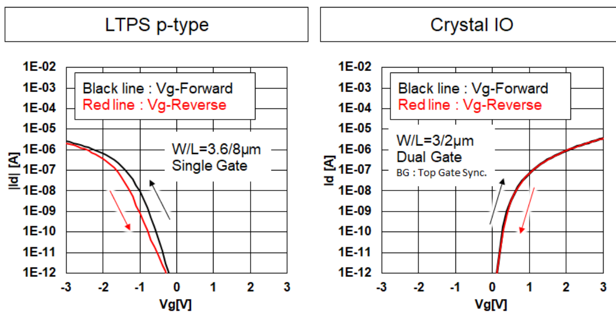


Figure 7. Hysteresis evaluation by Id-Vg measurement (Vds = 6 V, Vgs = –10 V to +10 V (Vg range is enlarged))

4. Trifold OLED Display

We fabricated a medium-sized trifold OLED display employing the crystal IO TGSA FET in the backplane for use as a tablet. Its specifications and pixel circuit are shown in Table 1 and Fig. 8, respectively. This pixel circuit can offer high luminance by boosting a data potential, but a threshold value is compensated using the back gate of a driving transistor M2 [20]. In a pixel circuit having an internal threshold compensation function, the sampling time and accuracy of the threshold value are important. The sampling time and accuracy of the threshold value were compared by simulation between the case where IGZO was used in the backplane and the case where the crystal IO was used in the backplane. The simulation results show that saturation does not occur until 20 μs in the case of using IGZO, whereas saturation occurs in approximately 10 μs in the case of using the crystal IO. This reveals that the threshold value of the crystal IO FET having higher mobility is obtained more accurately in a shorter time than that of the IGZO FET.

Table 1. Specifications of trifold OLED display

	Specifications
Screen diagonal	8.56 inches
Resolution	1200 × RGB × 1920
Pixel size	96.0 μm × 96.0 μm
Pixel density	265 ppi
Aperture ratio	17.4 %
Pixel circuit	6Tr3C
Coloring method	Side-by-side
Emission type	Top emission
Source driver	Chip on panel
Demultiplexer	Integrated
Scan driver	Integrated

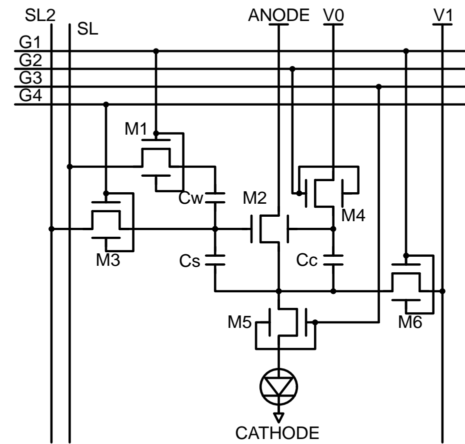


Figure 8. Pixel circuit diagram

Figure 9 shows the display results of the fabricated display panel. An image with excellent quality was displayed and the drivers operated correctly even when the display panel was folded.

Assuming the same luminance, a potential difference between the anode and the cathode in the case of the crystal IO active layer is reduced to 80 % of that in the case of the IGZO active layer. In other words, power consumption is also reduced to 80 %. Heat generation is an issue for flexible substrates. Lower power consumption results in smaller heat generation, which means that the crystal IO is highly compatible with flexible substrates.

Figure 9. Display result of trifold OLED display

Table 2 lists the features of the crystal IO. The crystal IO has advantages of an IGZO and LTPS or LTPO, and thus offers a panel with superior specifications.

Table 2. Comparison of features between FETs

		LTPS	IGZO	LTPO	Crystal IO
	Channel length	L ≥ 3μm	L ≥ 2μm	L ≥ 3μm (LTPS)	L ≥ 2μm
FET characteristics	Mobility [cm^2/Vs]	≤ 100 (n-type)	10	≤ 60 (p-type)	50 – 100
	Reliability	Excellent	Good	Excellent (LTPS)	Good
	On-state current	High	Low	High (LTPS)	Ultrahigh
	Off-state current	High	Ultralow	Ultralow (IGZO)	Ultralow
Productivity	Substrate size	G6	G8.5	G6	G8.5
	Processing temperature	≤ 550℃	≤ 400℃	≤ 550℃	≤ 400℃
	Number of masks *Compared with LTPS	-	-1	+3	-1
Panel specifications	Power consumption	Good	Excellent	Excellent	Excellent
	Narrow bezel	Excellent	Poor	Excellent	Excellent
	High frame rate driving	Excellent	Poor	Excellent	Excellent
	Low frame rate driving	Poor	Excellent	Good	Excellent

5. Conclusion

The TGSA FET with L = 2 μm including the crystal IO active layer is fabricated through a low-temperature process at 400 °C in a line for a G3.5-sized substrate. The fabricated TGSA FET has a field-effect mobility of 50 cm^2/Vs and normally-off characteristics with small variations. In addition, the TGSA FET has a high gate BT resistance and stable characteristics even after a glass substrate separation process and bending, thereby offering the trifold OLED display that displays an image with high quality.

The use of a high-mobility crystal IO TGSA FET in the OLED backplane enables low-power consumption, narrower bezel due to downsizing of driver circuits, and higher frame rate. This backplane technology is easily applicable to flexible devices and large-sized substrates such as G8-sized substrates, and can thus be a better alternative to LTPS and LTPO that has bright prospects for the future.

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