Video Transport Topologies for Ultra-High Resolution Automotive Displays

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Abstract

Ultra-high resolution automotive displays require a tremendous amount of video data. There is some industry concern about the ability of SerDes links to transport this data. This presentation provides a high-level overview of various existing topologies and emerging technologies which will support the necessary bandwidths.

Author Keywords

SerDes, resolution, DSC, compression

1. Introduction

As an example, a 24MPx (Megapixel)/30bpp (bits per pixel)/60 fps (frames per second) pillar-to-pillar display requires approximately 50Gbps of video payload data. In contrast, a 3840x2160, 24bpp, 60fps "4K" display is only 8.3Mpx and requires just 14Gbps. Displays which bring the consumer experience into the vehicle can demand much higher refresh rates of 90fps to beyond 144fps. This linearly increases the video data payload.

In automotive display systems utilizing SerDes, there are three primary bandwidth choke points: the ECU SOC-to-serializer, serializer-to-deserializer, and deserializer-to-TCON (or other endpoint device).

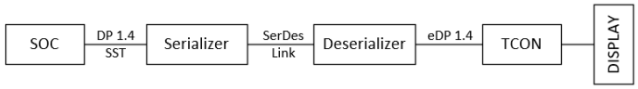

Figure 1: A representative SerDes IVI system with DP interfaces to a SerDes bridge.

Figure 1 depicts a system with the DP/eDP interfaces commonly used in high-bandwidth IVI (In-Vehicle Infotainment) systems. The DP/eDP 1.4 interfaces are limited to 25.92Gbps payload. The automotive Serializer-Deserializer (SerDes) links currently in production are limited to approximately 10Gbps payload, so the SerDes bridge is the constraining element.

While 30bpp color is slowly gaining popularity, 24bpp is much more common at this time. The calculations in this paper are done with 24bpp color, 10Gbps link payload, and 10% default blanking for consistency, unless otherwise specified. The analysis is focused on the signal chain from the SOC DP port to the deserializer eDP output and does not consider the capabilities of the SOC or TCON.

2. Baseline: Single SerDes Link

An uncompressed 10Gbps SerDes link supports approximately 6.3Mpx displays, with 415MHz PCLK (pixel clock). This topology is represented in Figure 1. The constraint is the SerDes link. This topology has been in production for many years.

3. Dual SerDes Links

By using two SerDes links between the serializer and deserializer, the capacity can be doubled to 12.6MPx, with 830MHz PCLK. The advantage of this architecture is that compression is not needed to achieve the higher payload, with the disadvantage that an additional cable and its related connectors are needed. The constraint is the SerDes links. This topology has been in production for many years.

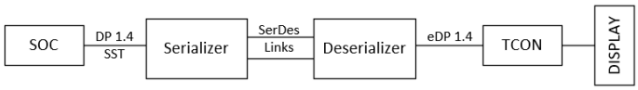

Figure 2: Dual-link topology without compression.

4. Single SerDes Link with Compression, Decompression in Deserializer

VESA DSC (Display Stream Compression) provides visually lossless compression of 3:1 for 24bpp color and 3.75:1 for 30bpp color. For a given PCLK, the SerDes link bandwidth is the same for 24bpp and 30bpp compressed video. Performing decompression in the deserializer enables the signal path to support 16.4Mpx/1080MHz PCLK. The constraint is the eDP interface. This topology has been in production for about five years.

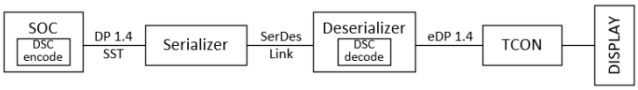

Figure 3: Single link topology with compression, decompression in deserializer.

5. Single SerDes Link with Compression, Decompression in TCON

TCONs are under development which provide DSC decompression. If decompression is performed in the TCON the eDP interface is removed as the constraint. Bandwidth increases to 19Mpx/1250MHz, constrained by the SerDes link bandwidth. Initial design evaluations are planned in 2025.

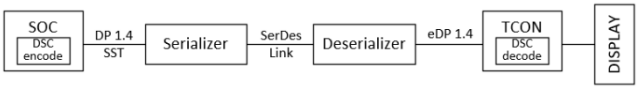

Figure 4: Single link topology with compression, decompression in TCON.

6. Compressed MSTs for Left and Right Display Panel Segments Using a Cingle SerDes link

TCONs supporting decompression will likely not be in widespread use for several years. Additionally, routing this much bandwidth from a single TCON to the display panels is still challenging. Using two TCONs will still be preferred in many systems.

An existing architecture which addresses these issues is to use separate MSTs for the left and right segments of the display. The MSTs are individually compressed by the SOC. Alternatively, a compressed superframe may be used. In its most economical implementation, the 30Gbps compressed bandwidth of the SerDes link is comprised of two 15Gbps streams. A single SerDes link carries the full bandwidth of the display, with the first deserializer outputting half of the video data and a daisy-chained deserializer outputting the other half. In this configuration, 19MPx/1250MHz PCLK can be delivered to the display. A synchronization mechanism can be used to align the two video sub-streams. This topology is bench validated and is in customer system verification.

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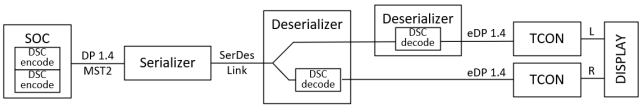

Figure 5: Two MST topology with compression, one SerDes link, decompression in deserializers.

7. Compressed MSTs for Left and Right Display Panel Segments Using Two SerDes links

Another existing architecture uses separate MSTs for the left and right segments of the display, each being routed using a separate SerDes link. The MSTs are individually compressed by the SOC. Alternatively, a compressed superframe may be used. Each SerDes link carries up to 30Gbps of compressed data. Each is connected to a deserializer which decompresses the video and drives a TCON via eDP. A synchronization mechanism can be used to align the two video sub-streams. The eDP 1.4a interfaces constrain the PCLK to 1080MHz each, so a total display of up to 33Mpx/2160MHz PCLK can be supported. This topology is bench validated and is in customer system verification.

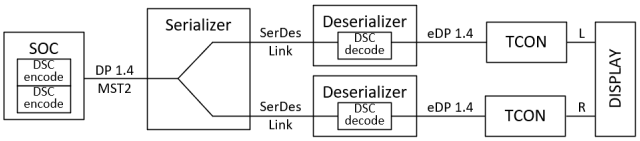

Figure 6: Two MST topology with compression, two SerDes links, decoders in deserializers

8. DP 1.4 with Higher Bandwidth SerDes

SerDes links under development with 13Gbps or 20Gbps payload capacity naturally increase the supported display resolution. A single link without compression, as shown in Figure 1, supports 8.3MPx/540MHz and 12.6Mpx/830MHz, respectively.

A 13Gbps link with DSC configured as shown in Figure 3 will support 25Mpx/1625MHz.

A 20Gbps link with DSC configured as shown in Figure 4 will support 38Mpx/2500MHz.

With two MST and two links used, as shown in Figure 6, the maximum payload is constrained by the DP 1.4 SOC/serializer interface to 49Mpx/3240MHz PCLK.

9. DP 2.x SOC-to-Serializer Interfaces

SOCs with DP2.x ports are planned to sample this year. SerDes vendors will eventually support DP2.x with matching interfaces There are two primary advantages to DP 2.1 in the automotive display environment:

1. It enables more displays to be supported by each SOC DP port, thus reducing the number of ports required.
2. It enables support of significantly higher resolution displays without and with compression.

4-lane DP2.x payload bandwidths for uncompressed video using UHBR10, UHBR13.5, and UHBR20 are 38.7Gbps, 52.2Gbps, and 77.4Gbps respectively.

It will be theoretically possible to transport the full payload of UHBR20 using four 20Gpbs payload SerDes links.

Compressed, two-link topologies as shown in Figure 6 will no longer be constrained by the SOC-Serializer interface bandwidth. 20Gbps SerDes links will support 76Mpx/5000MHz displays.

10. Summary and Conclusion

Table 1 provides a summary of the maximum display resolutions supported by each of the presented topologies and technologies. Existing solutions which are either in production or are bench-proven and in OEM system evaluations can support displays of up to 33Mpx/2160MHz PCLK. Over the next few years, the capability will more than double to 76MPx/5000MHz.

Table 1. Architecture Capability Summary

Topology	Max Res (Mpx)	Max PCLK (MHz)
Baseline: no compression, single SerDes link	6.3	415
No compression, dual SerDes links	12.6	830
Compression, single SerDes link, decompression in deserializer	16	1080
Compression, single SerDes link, decompression in TCON	19	1250
Compressed MSTs for left and right display panels using a single SerDes link	19	1250
Compressed MSTs for left and right display panels using two SerDes links	33	2160
Single 13/20Gbps link with compression	25 /38	1625 /2500
Dual 13/20Gbps links with compression	49	3240
DP 2.x SOC interface, compression, dual 13/20Gbps links	49 /76	3250 /5000

Note: SOC and/or TCON video processing capabilities might limit the higher resolutions.

11. Other Considerations

HDCP (High-bandwidth Digital Content Protection): Many cockpit displays require HDCP. All of the described architectures can support HDCP.

DP AE (DisplayPort Automotive Extensions) FuSa (Functional Safety): The VESA DP AE provides standardized FuSa protection using CRCs (Cyclical Redundancy Checks) transported in an SDP (Secondary Data Packet) transmitted synchronous with every video frame during the vertical blanking time. In addition to a frame CRC, CRCs are provided for ROIs (Regions of Interest), typically used for warning telltales.

The DP AE provides end-to-end FuSa from the DP Source Device (typically the ECU SOC) to the DP Sink Device (TCON or SerDes bridge composite device) for both uncompressed and compressed data.

DP AE Security: Security may become a requirement in display systems. It is supported by VESA DP AE Profile 2 (control plane) and Profile 3 (data plane).

12. Acknowledgements

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13. References

All work presented was performed by the author and/or his colleagues.