Large Scale Glass Substrate for High Performance Computing Application

Satoru Kuramochi
Dai Nippon Printing Co., Ltd, Chiba, Japan
E-mail: kuramochi-s2@mai.dnp.co.jp

Abstract

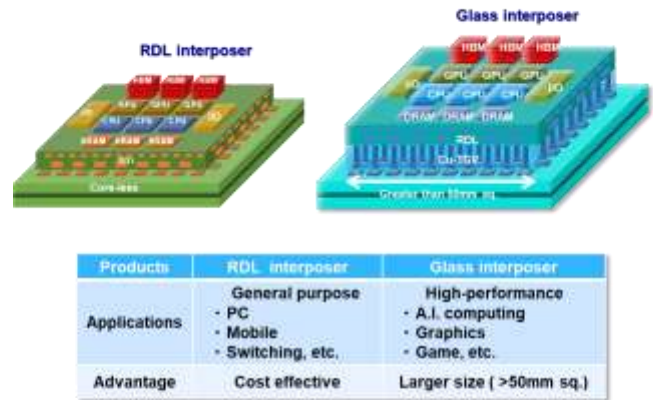
As the industry moves toward High Performance Computing (HPC) for huge data transmission with low power consumption. The requirements for PKG structure have become more challenging. The major engineering requirements for HPC application are high-density, high-speed data transmission, low loss, precision manufacturing with low-cost process. High pin count needs large area package with high mechanical stability and low warpage.
This paper presents the demonstration of RDL interposer and Glass Core Substrate with large panel size format. In case of Glass core substrate process, three metalized processes were compared process capability, reliability and high-speed transmission characteristics. Filled with Cu method is found out low resistance, high transmission rate and high-power density. In the thermal stress simulation, the heat characteristics and thermal mechanical stress analysis for two types of via shapes, straight and X-shape, were analyzed, which indicated that straight vias were advantageous for suppressing heat generation, while X-shape was for mitigating thermal stress. The reliability test result obtains stable resistance data because of combination of double-sided polymer dielectrics. The double-sided polymer dielectrics owing stress buffer of glass and cupper CTE difference. The Filled with Cu method demonstrated with large panel size format max 510x515mm with 6layers build-up.

Author Keywords

HPC, high-speed data transmission, high reliability, Glass core substrate,

1. Introduction

In recent years, as data centers have grown larger and the utilization of AI has advanced, there is increasing expectation for semiconductor products that can handle increasing data transmission and high-speed signal transmission. Thus, new structures such as chiplets and heterogeneous integration packaging have been proposed. On the other hand, with the miniaturization, lightweight, and increased functionality of electronic devices, there is a growing demand for high density and high integration. As the industry increasingly adopts High HPC for large-scale data transmission while minimizing power consumption, the demands on Package structure have become more complex and challenging. The major engineering requirements for HPC application are high-density, high speed data transmission, low loss, precision manufacturing and low cost. In response to these challenges, we have developed low-loss RDL and glass core technologies. Fig. 1 shows images and characteristics of RDL interposer and glass interposer (GIP) as examples of ultra high-density substrates.



Products	RDL interposer	Glass interposer
Applications	General purpose · PC · Mobile · Switching, etc.	High-performance · A.I. computing · Graphics · Game, etc.
Advantage	Cost effective	Larger size (>50mm sq.)

Figure 1. Ultra high-density substrate

2. RDL Interposers

A. Concept of development

Fig. 2 shows target specification and feature of RDL Interposer for high performance computing.

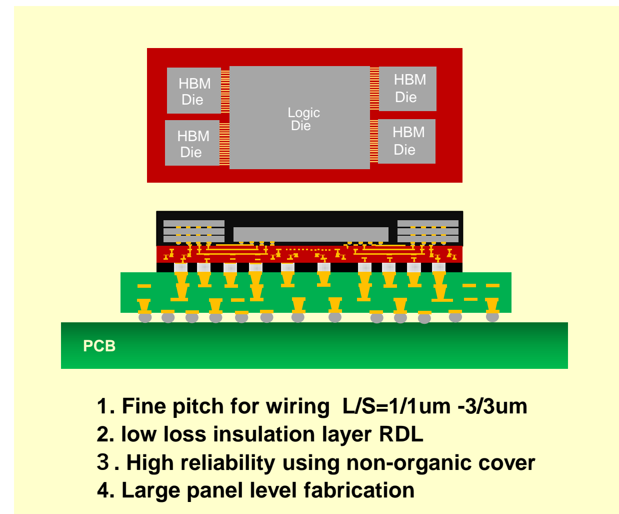


Figure 2 . Schematic structure and feature of RDL Interposer

ISSN 0097-996X/25/5602-1113-$1.00 © 2025

B. Demonstration of fabrication with 300mmx400mm panel

Process flow of RDL layers. At first, seed layer formation on lower steps on the insulation layer. (a)

Secondary, Photo resist formation and open the wiring area with developer. Thirdly, electro-plating applied open area of photo resist. (c) After resist striped(d), seed layer metal was etched. (e) And then inorganic layer deposit on the Cu trace(f). It is original process for high reliability of the RDL layer. After insulation layer formation, inorganic layer was dry-etched through opening area of insulation layer. Finally micro bumps formation on the top layer.[1] Fig. 3 shows demonstration result of fine wiring layers on 300x400mm Glass panel format. 2-µm pitch Cu trace fabricated on the large glass.

High aspect ratio wiring obtained electro-plating with semi-additive process. Fig. 4(a) shows high aspect ratio wiring. Aspect ratio of wiring was about 3 on L/S=1/1µm.

Fig. 4(b) show L/S=1/1µm trace with protective layer. Inorganic layer enhance highly reliability on the narrow pitch under 2µm. [2)3)]

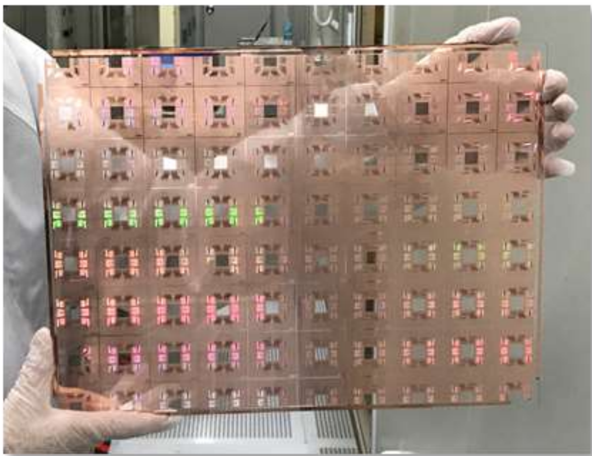
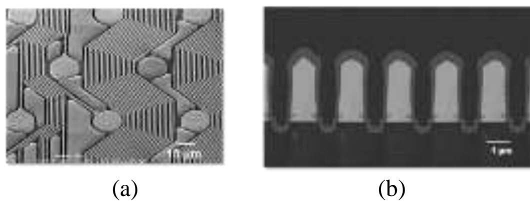


Figure. 3 Fine wiring layers on 300x400mm Glass panel format.



(a) (b)

Figure. 4 (a) L/S=1/1µm trace, (b)trace profile with protective layer.

Insulation layer materials is important role of RDL properties. Insulation layer materials needed small size micro via, Low stress for reduction warping and low loss tangent for high-speed signal transmission.

We demonstrate coplanar waveguide (CPW) transmission line with fine wiring layers. TEG fabricated on core glass to measure high frequency characteristics. Fig.5 shows real measurement result of fine wiring consist of CPW structure with 5mm length. Insertion loss has large value with fine wiring pitch due to the conductive loss will be large. As the L/S becomes finer than 2/2µm, there is a tendency for the Cross-sectional Area to decrease, which results in an increase in insertion loss and deterioration of Eye Diagram (Fig.6). Therefore, it is crucial to focus on the high-aspect-ratio formation of the Transmission Line.

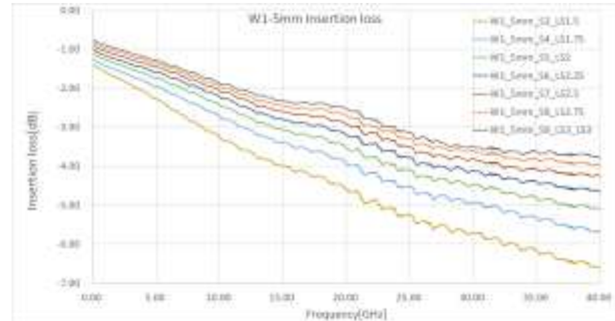


Figure. 5 Measurement result of fine wiring consist with CPW structure.

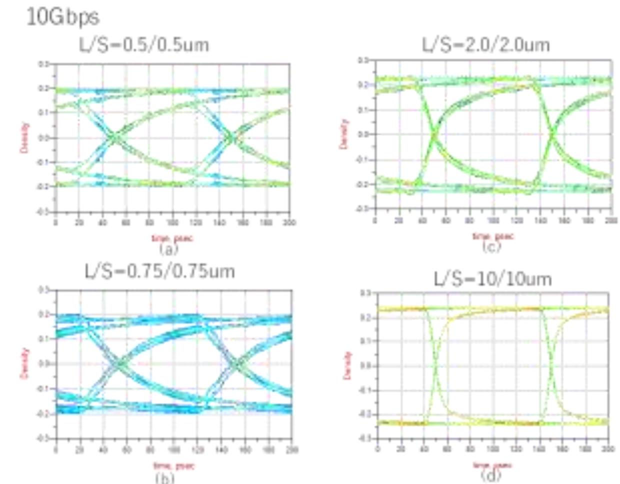


Figure.6 Eye diagram simulation result of CPW on RDL.

3. Glass core substrate

A Concept of development

Fig. 7 shows target specification and feature of glass Interposer for high performance computing. Fig. 8 shows process flow of Glass interposer. First of all, TGVs of 80µm in diameter and 200µm in pitch were formed on 400µm thick alkali-free glass. Ti/Cu seed layer deposition. Then the via was deposited with Cu by conformal electroplating. Thick dielectric polymer layer was laminated on the wafer as RDL passivation film. Redistribution lines were patterned with photo resist. Cu RDL line of 5 µm thickness was deposited by Cu electroplating followed by photo resist and Cu seed layer removal. The conformal plating method has great advantage of process time of plating. After depositing the seed layer, plasma ashing was done from the both sides of the wafer to improve the hydrophilic property of the surface of Cu seed layer.

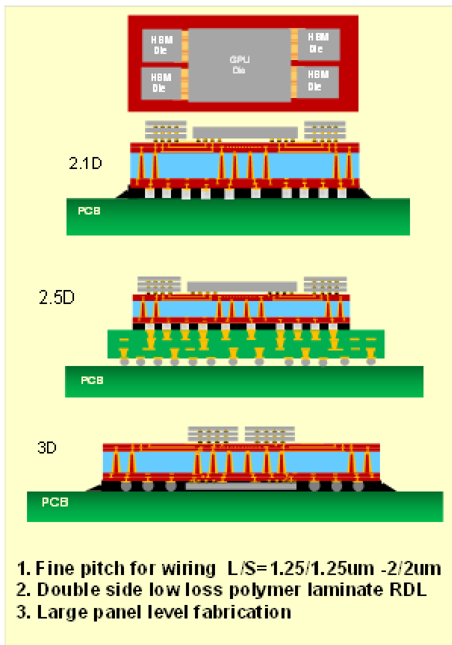


Figure. 7 Schematic structure of Glass based substrate

Fig.9 showcases a filled via with dimensions of 510x515 mm, while Fig. 10 exhibits a partially filled Cu method on a 300x400mm panel.

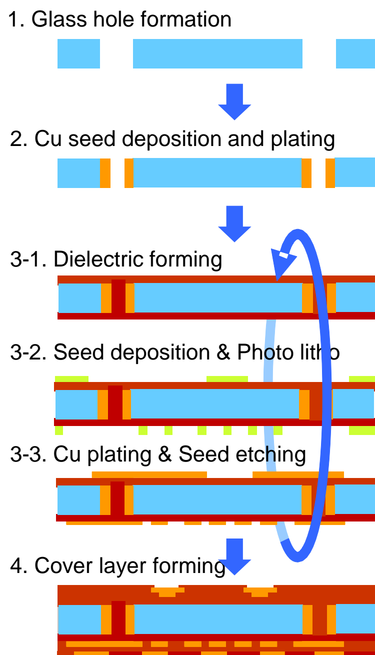


Figure. 8 process flow of Glass interposer

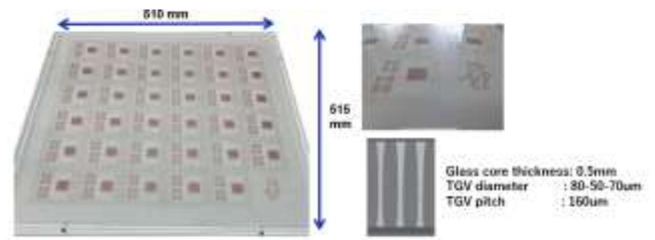


Figure.9 Filled with Cu Via method

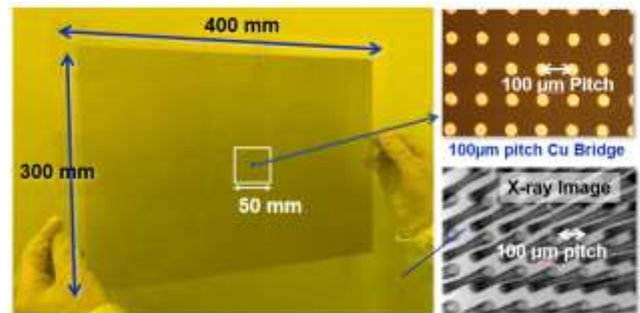


Figure.10 Partially filled with Cu method

A. *Reliability of glass interposer*

We conducted reliability tests on each of the three types of TGV. Fig.11 shows result of Thermal cycle test (TCT) for conformal type. Test condition is temperature cycles from -40°C to 85°C with a dwell time of 30 min at each temperature. No significant resistance changes were observed during the test, even after conducting 1000 cycles.

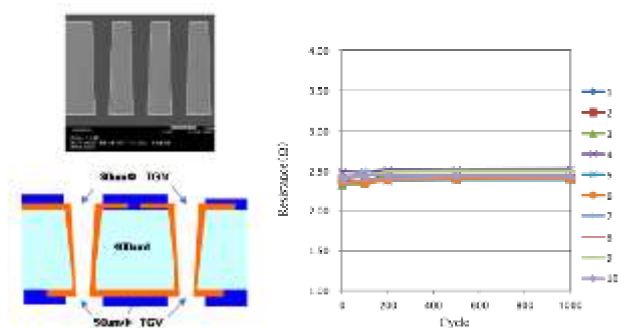


Figure.11 Thermal cycle test result of conformal type TGV

Next, Figure 12 shows Thermal cycle test vehicle with Filled type TGV. Figure 13 shows the results of filled type TCT. The conditions for this TCT were a cycle of -55℃ to 150℃. As with the conformal type, no significant resistance change was observed even after 500 cycles.

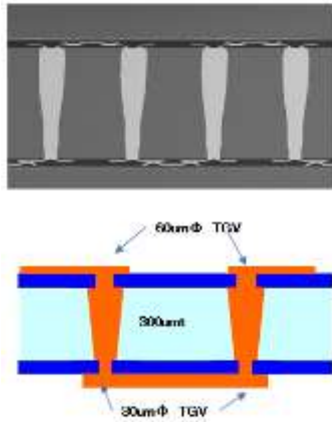


Figure.12 Thermal cycle test vehicle with Filled type TGV

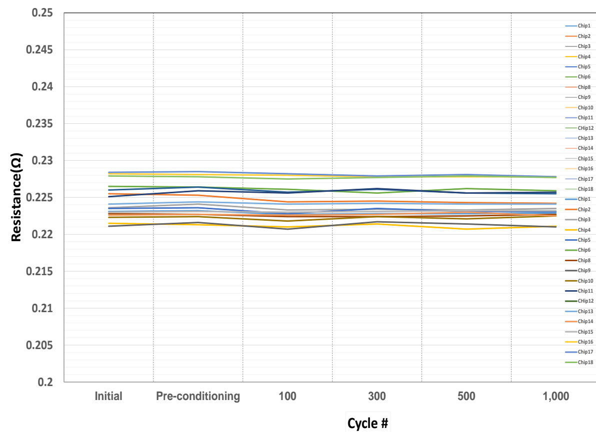


Figure.13 Thermal cycle test result of Filled type TGV

C. RDL on Glass core substrate

We present the results of our RDL 2/2 μ m on glass core substrate. This glass package size is 130X130mm, and the TGV are fully filled with Cu. We have successfully fabricated it without encountering any issues in the overall dimensions of 300×400mm shown in Fig,14.

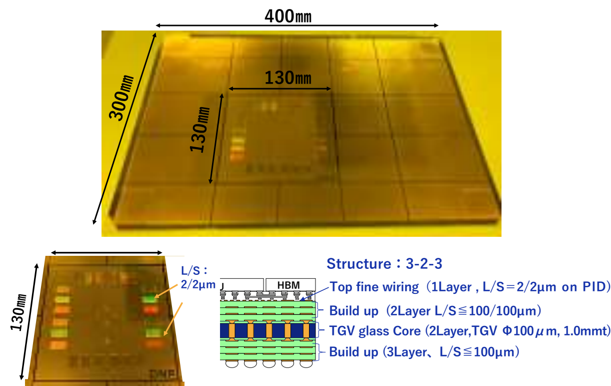


Figure.14 300X400mm RDL on glass core panels

4.Conclution

To achieve Ultra-High density RDL, it is necessary to miniaturize the wiring (L/S=1/1) and the vias (Bottom diameter 3um). We conducted the necessary verification for Ultra-High density RDL on a panel size of 300 × 400 ㎜. We also demonstrated the multilayering and conducted a demonstration of a 5-layer RDL. Additionally, although not mentioned in this paper, we announced that high reliability can be achieved by protecting the fine wiring with inorganic dielectric. [6] The measurement results of the insertion loss (S21) of the fine wiring and the simulation results of the eye pattern show that as miniaturization progresses, the high-frequency characteristics deteriorate. To solve this issue, it is necessary to increase the thickness of the wiring to reduce the resistance of the conductor. Therefore, we have achieved a high aspect ratio (A/R=3) by adopting a semi-

As for TGV, we have developed three types (conformal, field, partial filled) and have revealed that each type achieves low insertion loss (good high-frequency characteristics) based on the measured results. Furthermore, by conducting Thermal Cycling Test for the three types, high reliability has also been demonstrated.

We present the results of our RDL 2/2 μ m on glass core substrate. This glass package size is 130X130mm, and the TGV are fully filled with Cu. We have successfully fabricated it without encountering any issues in the overall dimensions of 300×400mm.

5.Reference

[1] Hiroshi Kudo et al., "A chracterized redistribution layer atchitecture for Advanced Packaging technology" Proceeding of 66th Electronic Components and Technology Conference, (2016), pp. 2063-2067.

[2] Takamasa Takano et al., "Submicron-scale Cu RDL Pattering Based on Semi-additive Process for Heterogeneous Integration" Proceeding of 69th Electronic Components and Technology Conference, (2019), pp. 94-100.

[3] Hiroshi Kudo et al., "Panel-Based Large scale interposer Fabricatied using 2-μm pitch semi additive process for chiplet-based integration" Proceeding of 72th Electronic Components and Technology Conference, (2022), pp. 836-844.

[4] Hiroshi Kudo et al., "Signal Integrity of 2-μm-Pitch RDL Interposer for High-Performance Signal Processing in Chiplet-Based System" Proceeding of 73th Electronic Components and Technology Conference, (2023), pp. 531-536.

[5] Hiroshi Kudo et al., "A chracterized redistribution layer atchitecture for Advanced Packaging technology" Proceeding of 66th Electronic Components and Technology Conference, 2021, pp. 1829-1833