High-Current LTPS-TFT Backplane Structure for 136-in. UHD Seamless Tiling MicroLED Displays

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Abstract

We developed the novel TFT backplane structure on glass for 136'' UHD Seamless Tiling Micro-LED Displays. The high current TFT backplane based on the combination of patterned active layer and high-k gate insulator has solved many issues such as degradation of device characteristics due to the self-heating and channel width limit in fixed pixel area for Micro-LED Displays

Author Keywords

Micro-LED, Tiling Display, Polycrystalline silicon thin-film transistor (poly-Si TFTs), Low Temperature Polycrystalline silicon thin-film transistor (LTPS TFT), High current TFT, High dielectric constant (high k), Self-heating effect, Excimer laser annealing (ELA)

1. Objectives and Background

Micro-LED is the light source that is expected to become the main player in future displays, following the OLED [1]. Although Micro-LED is being developed for various applications such as for watch, VR, and AR, it is an attractive choice for use in commercial displays, such as movie screens and outdoor displays due to its high brightness and good reliability. In particular, it is in the spotlight as the light source of tiling displays, which can be expanded in size indefinitely. Low temperature Polycrystalline silicon thin-film transistors (LTPS TFTs) is a main candidate for the backplane to drive micro-LED displays [2].

There are two aspects to consider when developing TFT backplane for commercial micro-LED displays. The first aspect is the driving current. Since poly-Si TFT backplanes have been developed mainly for mobile displays, driving current of light source is as low as about nano-ampere (nA) in full-white. However, the driving TFT (D-TFT) of pixel circuits for the micro-LED must supply high currents in the range of tens to hundreds micro-amperes (uA) stably as shown in Figure 1. The second is their reliability. While mobile displays are usually for personal use, large screen micro-LED displays are often used for commercial purposes. Because they require long term reliability, TFT backplanes for the micro-LED must also be more robust.

The easiest way to increase the driving current of a device is increasing the channel width. However, channel width cannot be increased indefinitely in a limited pixel area. Furthermore, if width is lengthened, there is a problem of deterioration of the device characteristics due to the self-heating effect [3][4]. As on-current (I_{on}) increases, off-current (I_{off}) also increases, so the method to control I_{off} is needed.

Therefore, we tried to find the solution for mass production of TFT backplanes and successfully developed the 136'' UHD Seamless Tiling Micro-LED Displays. In this work, the new concept of the LTPS TFT structure based on the combination of TFT structures and processes was introduced.

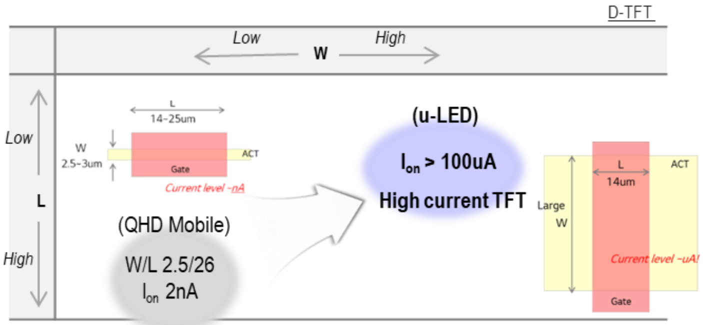

Figure 1. Comparison of driving current of Driving-TFT (D-TFT) in full-white mode by types of display

2. Results

A. Patterned Active

If the channel width is increased for driving capability as shown in Figure 1, heat dissipation inside the channel becomes difficult, which may cause the component to degrade. The well-known method is to divide active in the channel direction as shown in Figure 2(b). This structure can prevent the deterioration of TFT characteristics by dissipating the heat generated in the high field to the surroundings [5]. As the active layer is divided into many parts, the reliability improves, but the area occupied by the TFT inevitably increases due to the increased distance between unit active channels. Accordingly, the new structure was developed that can secure the maximum current while facilitating heat dissipation within the allowed pixel area.

As shown the top view image in Figure 2(c), the channel shape of the new structure is different from the conventional one, by patterns placed in active layer. The active of conventional device at the bottom of gate electrode is completely divided, but some are connected and divided in the new structure. In this case, the active area is divided into Area A, which is channel, and Area B as shown on Figure 3.

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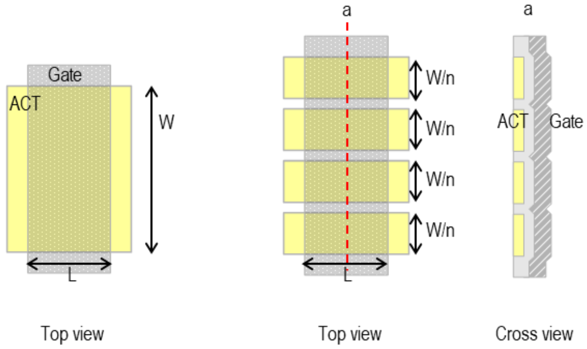
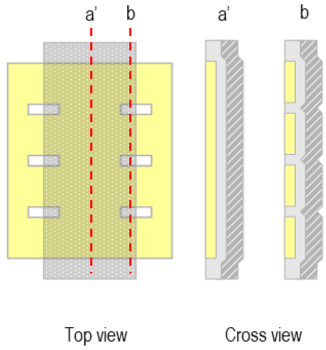


(a) TFT-a (b) TFT-b



(c) TFT-c

Figure 2. Comparison of TFT structure in the conventional (a and b) and new structure (c)

(n : number of Active block)

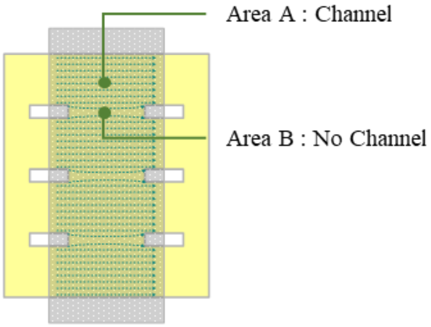
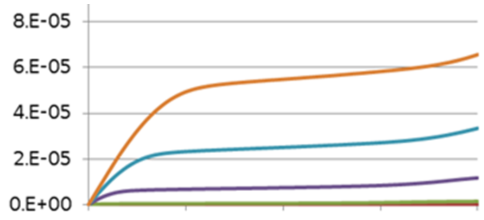
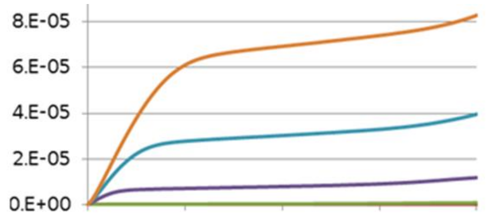


Figure 3. Active characteristics of new structure (TFT-c)

This structure has two advantages. First, the current loss rate can be minimized compared to the conventional one because its active is connected. As you can be seen from output curves of the two devices, which are TFT-b and TFT-c, in Figure 4, the current level of the new one was higher even though it had similar threshold voltage and mobility.



(a) Conventional TFT



(b) TFT with the patterned ACT

Figure 4. Comparison of output curve in the conventional TFT (a) and new structure TFT (b)

Second, thermal stability can be secured. Figure 5 shows the on-current (I_{on}) and the V_{th} change (dV_{th}) due to high drain current stress (HDCS) of TFT-b and TFT-c with respect to TFT-a. In the case of TFT-b, which divided the active layer, dV_{th} due to HDCS was greatly reduced compared to TFT-a, but I_{on} was similar or slightly reduced. However, dV_{th} of TFT-c was similar to that of TFT-b, even though I_{on} increased by more than 20%. These results show that TFT-c has a structure that can efficiently secure I_{on} while controlling degradation due to heat. As shown as Figure 3, the current of TFT-c mainly flows in the main channel, heat is generated in Area A and released to Area B.

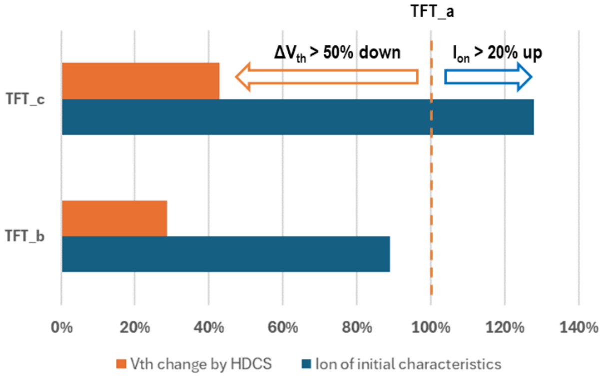
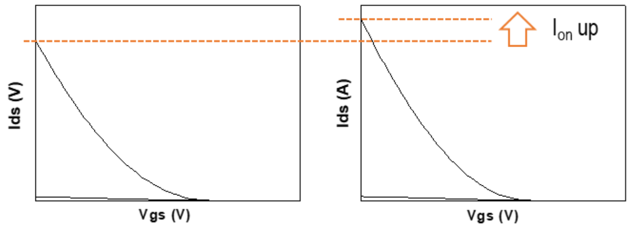


Figure 5. The on current (I_{on}) and the V_{th} change (dV_{th}) due to high drain current stress (HDCS) of TFT-b and TFT-c with respect to TFT-a.

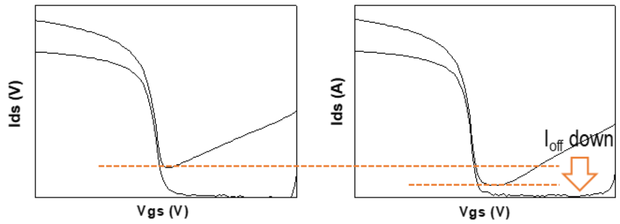
B. High k Gate Insulator

In a given pixel area, one of the most effective ways to increase the current level of driving-TFT (D-TFT) is to increase the dielectric constant of gate insulator (GI). The GI of LTPS TFT is usually silicon oxide (SiO_2), but we were able to develop high-k GI by combining SiO_2 and silicon nitride (SiN_x). As shown the comparison of on-current (I_{on}) in Figure 6, I_{on} of D-TFT was increased by more than 15% by using high-k GI.



(a) (b)

Figure 6. Comparison of I_{on} in the conventional SiO_2 GI TFT (a) and high-k GI TFT (b)



(a) (b)

Figure 7. Comparison of D-TFT Transfer curve in the conventional SiO_2 GI TFT (a) and high-k GI TFT (b)

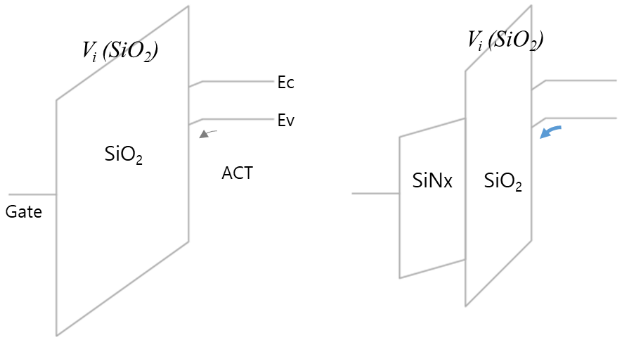
Another important point is that off-current (I_{off}) has been dramatically reduced as you can see in Figure 7.

Voltage of insulator (V_i) varies depending on the dielectric constant of the insulator, as in (1).

$$V_i = \frac{-Qs\ d}{\varepsilon_i} = \frac{-Qs}{C_i} \qquad (1)$$

Figure 8 shows the MOS energy band diagram in the conventional SiO_2 GI and high-k GI. When SiN_x is introduced to GI, V_i is bisected for each layer while the overall Vi is fixed when the gate voltage is applied. As higher field is distributed to SiO_2 compared to SiN_x, which has a high dielectric constant, the degree of bending of active layer in contact with SiO_2 increases, which leads to a decrease in I_{off}.

Finally, the development of robust GI led to a reduction of the breakdown voltage (BV) by more than 30%. This enabled the development of the TFT backplane, which is robust to electrostatic failures.



(a) (b)

Figure 8. Comparison of MOS energy band diagram in the conventional SiO_2 GI (a) and high-k GI (b)

3. Impact

We have developed the novel TFT backplane for 136'' Seamless Tiling Micro-LED Displays with a resolution of UHD (3840x2160) and a pixel pitch of 0.78. Figure 9 shows the MicroLED display that was unveiled at ISE 2025 last February. This TFT structure can realize the maximum current within a given pixel area while various device degradation. It is expected that this result can be expanded and deployed in various displays with high current and high reliability.

Figure 9. The image of 136'' Seamless Tiling Micro-LED Displays with a resolution of UHD (3840x2160) and a pixel pitch of 0.78

4. References

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