High-Speed Driving Pixel Circuit for Medium-Sized NanoLED Displays Based on Oxide TFTs

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Abstract

We have developed a new pixel circuit designed for self-emissive displays. This circuit enables high-speed operation through features such as the separation of Vth compensation and data writing period, 2H-open driving, and low-load charging. Utilizing this circuit, we prototyped a nanoLED display for a 16-inch UHD+ notebook and successfully demonstrated the effectiveness of the pixel circuit.

Author Keywords

Pixel circuit for internal compensation, High-speed driving, nanoLED display, Medium-sized display, Top-gate IGZO TFT

1. Background

In recent years, OLED technology has been widely adopted for self-emissive displays across various applications. Notably, most smartphone displays now utilize OLED technology, and its adoption is also expanding in medium-sized displays for notebooks and automotive applications. For mobile to medium-sized self-emissive displays, internal compensation techniques are commonly employed to compensate for the threshold voltage of the driving transistors within the pixel. Traditionally, the 7T1C circuit has served as the standard configuration for internal compensation, and hybrid processes combining LTPS and oxide TFTs have been proposed based on this circuit architecture, with many products currently utilizing these technologies [1][2].

However, this pixel circuit faces two significant challenges. First, the hybrid process involving the combination of LTPS and oxide TFTs tends to increase manufacturing complexity and costs. Second, conventional 7T1C pixel circuits, or circuits based on them, require that both threshold voltage compensation and data writing be completed simultaneously, which limits their capability for high-speed operation.

This paper proposes a new pixel circuit designed to overcome these challenges. This circuit is composed solely of oxide TFTs, enabling high-speed operation even in medium-sized displays intended for notebooks and automotive applications, where bus line loads are typically high. This approach allows for a reduction in costs while achieving high display quality compared to displays manufactured using hybrid processes. Furthermore, we will also introduce the development of a notebook display that utilizes next-generation light-emitting devices, specifically nanoLEDs (quantum dot LEDs).

2. A New pixel circuit for high-speed driving

2.1. Proposed pixel circuit

The proposed pixel circuit is illustrated in Figure 1. This circuit is composed of seven TFTs and two capacitors (7T2C). All components are constructed using N-channel IGZO-TFTs. The driving TFT is designated as T4, while T5 and T6 are responsible for controlling the current flowing to the light-emitting element. As will be detailed later, T2 functions as a switch to maintain the gate potential of the driving TFT during threshold voltage compensation, while the operation of T1 and T3 facilitates the writing of the data voltage Vdata to the pixel circuit. Additionally, T7 is utilized to initialize the anode potential of the light-emitting element.

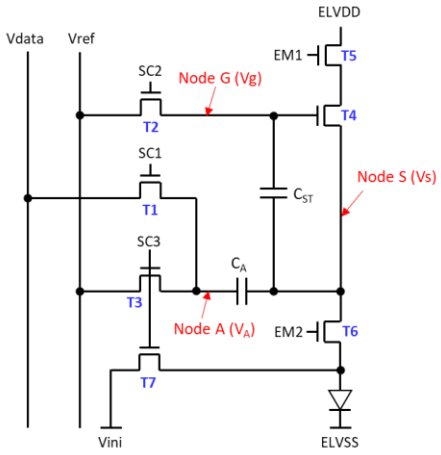

Figure 1. Proposed pixel circuit

2.2. Driving architecture

The driving method for this pixel circuit will be elucidated using Figures 2 and 3.

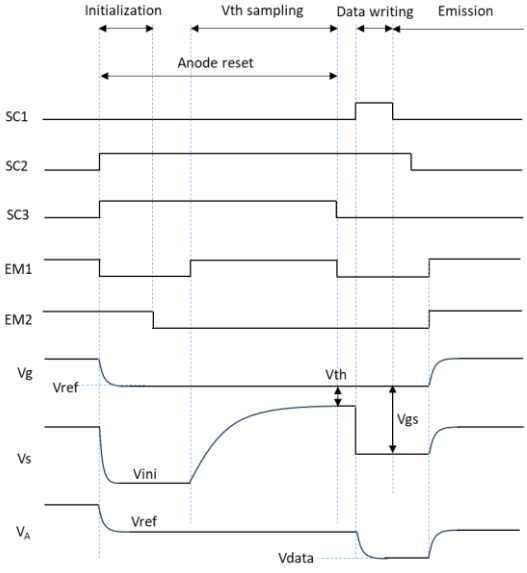

Figure 2. Timing diagram

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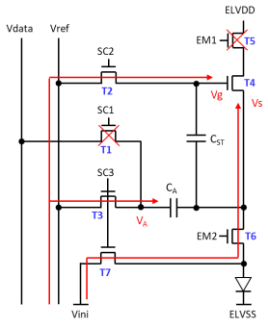


Figure 3(a). Initialization

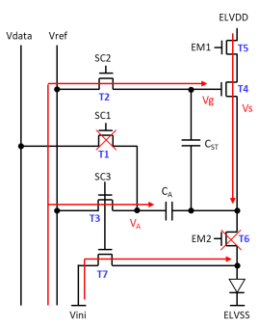


Figure 3(b). Vth sampling

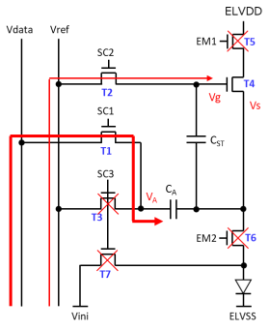


Figure 3(c). Data writing

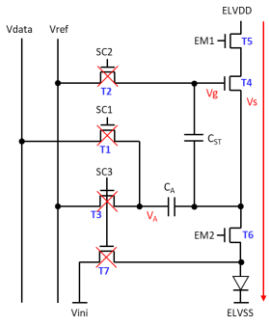


Figure 3(d). Emission

Figure 2 presents the driving timing diagram for the proposed pixel circuit, while Figure 3 illustrates the charging and discharging states during each operational phase depicted in Figure 2. As shown in Figure 2, the pixel circuit is driven by five control signals.

Initialization

Initially, the potential of the driving TFT is initialized (Figure 3(a)). By setting SC2, SC3, and EM2 to high, TFTs T2, T3, T6, and T7 are turned on, allowing node G to be charged to Vref through T2 and node S to be charged to Vini via T6 and T7. Simultaneously, the anode potential of the light-emitting element is reset to Vini through T7. Node A is charged to Vref via T3.

$$Vg = V_A = Vref$$
$$Vs = Vini$$

Vth Sampling

Next, the threshold voltage Vth of the driving TFT T4 is sampled (Figure 3(b)). Node G and node A are maintained at Vref through T2 and T3. With EM2 set to low, T6 is turned off, electrically isolating node S from the light-emitting element. Additionally, when EM1 is set to high, current flows from ELVDD to node S through T4 and T5. At this point, node S is charged until Vs = Vref - Vth, thereby allowing for the sampling of the threshold voltage Vth. The anode potential of the light-emitting element remains reset to Vini.

$$Vg = V_A = Vref$$
$$Vs = Vg - Vth = Vref - Vth$$

Data Writing

Subsequently, the data voltage is written to the pixel circuit (Figure 3(c)). Node G continues to be maintained at Vref. EM1, EM2, and SC3 are set to low, resulting in T3, T5, T6, and T7 being turned off. When SC1 is set to high, T1 is activated, charging node A with the data voltage Vdata. Consequently, node A transitions from its previously charged state of Vref to Vdata. During this process, node S is influenced by the potential variation of node A through C_A. Therefore, the potential state at this moment can be expressed as follows:

$$Vg = Vref$$
$$V_A = Vdata$$
$$Vs = Vref - Vth + \frac{C_A}{C_{ST} + C_A}(Vdata - Vref)$$

From the above equations, the gate-source voltage (Vgs) of the driving TFT T4 and the on-current (Ion) of T4 can be expressed as follows:

$$Vgs = \frac{C_A}{C_{ST}+C_A}(Vref - Vdata) + Vth$$
$$Ion = \frac{W}{2L}\mu C_{ox}(Vgs - Vth)^2$$
$$= \frac{W}{2L}\mu C_{ox}\left(\frac{C_A}{C_{ST}+C_A}(Vref - Vdata)\right)^2$$

As indicated by the equations, the term related to Vth is eliminated from the expression for Ion. This mechanism enables Vth compensation, allowing for the stable supply of on-current to the light-emitting element, independent of variations in Vth.

3. High speed driving

The proposed pixel circuit enables faster operation compared to the conventional circuit. Figures 4 and 5 will be used to elucidate the high-speed driving performance of the proposed pixel circuit.

3.1. Separation of Vth Sampling and Data Writing

As shown in Figure 2, the new circuit separates the timing for Vth sampling and data writing. To achieve high-speed operation, it is essential to shorten the data writing time. In this pixel circuit, the data writing time and Vth sampling time can be configured independently. This allows for the data writing time to be reduced while still maintaining a sufficiently long Vth sampling time. Consequently, high precision in Vth compensation can be preserved even during high-speed operation.

3.2. 2H-open driving

The pixel charging process in the proposed circuit is also illustrated in Figure 4. The gate signal SC1 remains open for two horizontal periods. In this circuit, it is sufficient to perform pixel charging before the completion of one horizontal period required to write the desired data voltage. During this process, the inclusion of another data voltage, such as that from the previous row, does not affect the final pixel charging outcome. Therefore, the gate signal SC1 can remain open for, for example, two horizontal periods.

This flexibility allows the time needed to open the gate signal SC1 (t_open) to be excluded from the pixel charging duration. Consequently, the pixel charging time (t_pix) can be expressed as follows:

$$t\_pix = 1H - (t\_vd + t\_close)$$

Particularly for displays aimed at node PC applications, which are typically landscape-oriented, the load on the gate bus lines tends to be significant. As a result, (t_open) is likely to increase. To drive such displays at high speed, it is crucial to eliminate the contribution of (t_open), making support for 2H-open driving extremely important.

In summary, by employing the proposed pixel circuit, sufficient pixel charging duration can be maintained even during high-speed operation, where the one horizontal period (1H) is shortened, thereby ensuring stable operation.

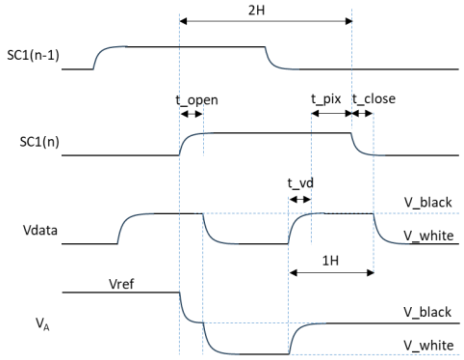


Figure 4. Driving waveform in pixel charging period

3.3. Low loading pixel charge

The charging path during data writing for the proposed circuit is illustrated with red lines in Figure 5. In the proposed circuit, the effective pixel load for charging is significantly reduced since pixel charging occurs with C_A and C_{ST} connected in series. For instance, when C_A = 160fF and C_{ST} = 85fF, pixel charging can be performed against the equivalent series capacitance of 55fF. This configuration allows the pixel load to be minimized, thereby shortening the pixel charging time.

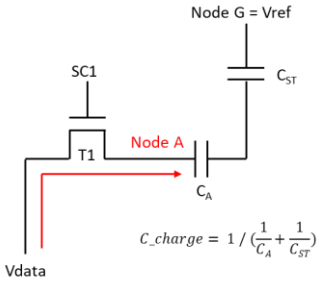


Figure 5. Data writing to pixel capacitor

3.4. Simulation result

The proposed pixel circuit is advantageous for high-speed operation due to these three characteristics. The results of simulations conducted to evaluate high-speed driving performance are presented in Figure 6. This figure illustrates the black current during black image, relative to the 1H period. The pixel circuit, driving timing and surrounding load are based on a 16-inch UHD+ (3840 x 2400) display.

When driving UHD+ at 60 Hz (with 1H = 6.8usec.)), the black current is normalized to 1. The figure shows the relative magnitude of the black current when the refresh rate is increased to 120 Hz and 240 Hz. Here, a comparison is made between the proposed circuit and the conventional 7T1C circuit [2].

As illustrated in Figure 6, in the conventional circuit (red line), the reduction in 1H time leads to insufficient pixel charging, resulting in an increase in black current and a significant decrease in contrast. In contrast, the proposed pixel circuit (blue line) maintains the same black current at 240 Hz as observed during 60 Hz operation.

By adopting the proposed circuit, it is possible to sustain high-quality display performance even during high-speed operation.

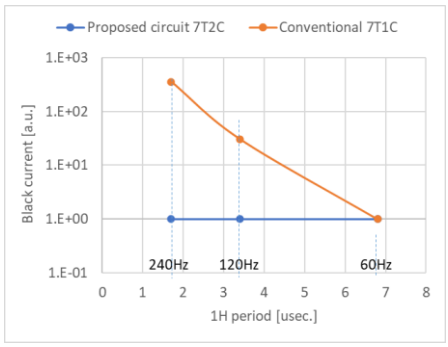


Figure 6. Simulation result of black current

3.5. Low refresh rate driving

Furthermore, this circuit is entirely composed of IGZO-TFTs, allowing for the realization of low-frequency operation. The waveform for the idle frame during low-frequency operation is illustrated in Figure 7. In this state, SC1 and SC2 are maintained in a low state. SC3, EM1, and EM2 perform operations similar to those in the writing frame depicted in Figure 2. By activating SC3, the anode potential of the light-emitting element is reset as needed, thereby stabilizing the emission state. During this time, by placing the driver IC in a standby mode, a reduction in power consumption can be achieved.

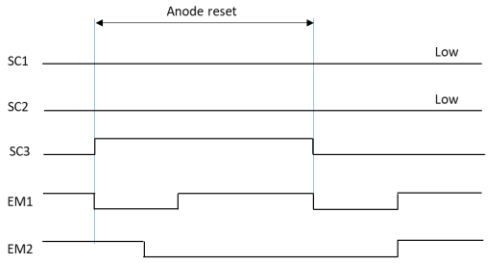


Figure 7. Timing diagram of low frame rate driving

4. 16-inch UHD+ nanoLED display

4.1. NanoLED

The proposed pixel circuit has been utilized to create a 16-inch UHD+ panel. In this demo sample, nanoLEDs have been employed as the front plane [3]. The structure of the nanoLED is illustrated in Figure 8. NanoLEDs are commonly referred to as QD-LED or QD-EL and are light-emitting devices that utilize quantum dots. The configuration is similar to that of OLEDs, with the quantum dot emission layer formed between the electron transporting layer and the hole transporting layer. NanoLEDs are expected to exhibit superior characteristics such as a wide color

gamut and high brightness compared to OLEDs. Furthermore, it is anticipated that the effective utilization of the LCD manufacturing process will enable low-cost production. Additionally, nanoLEDs can be patterned using photolithography, allowing for the formation of high-resolution pixels with a high aperture ratio. Given these advantages, we believe that nanoLEDs have the potential to be applied across a wide range of applications, from VR/AR to large-scale displays.

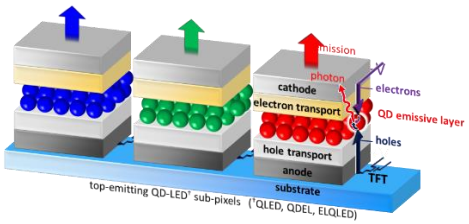
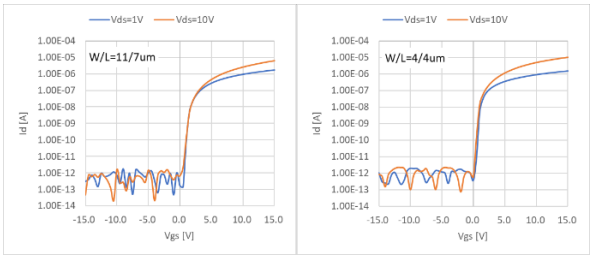


Figure 8. Structure of NanoLED

4.2. IGZO TFT

All the TFTs that constitute this demo panel utilize top-gate IGZO technology. Figure 9 presents the characteristics of the IGZO used in this demonstration. Figure 9(a) shows the characteristics of the driving TFT T4. Figure 9(b) illustrates the characteristics of the switching TFTs, excluding T4. The driving TFT employs a double-gate structure with the source grounded.



(a) (b)

Figure 9. IGZO TFT Vg-Id curve (a) Driving TFT (b) Switching TFT

4.3. Demo sample

Using these devices, a demo sample has been created. Table 1 provides detailed specifications, with the display designed for a 16-inch UHD+ notebook. The panel supports a variable refresh rate (VRR) ranging from 1 to 120 Hz. Figure 10 illustrates the illuminated state of the demo panel.

Panel size	16.0 inch
Resolution	3840×RGB×2400
Pixel density	283 ppi
Pixel pitch	89.76 um
Frame rate	1~120Hz
1H period	3.2 usec.
TFT	IGZO

Table1. Specifications of demo sample panel

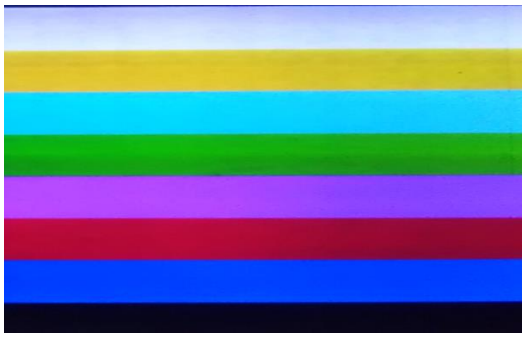


Figure 10. 16-inch UHD+ demo sample

5. Conclusion

In summary, we have developed a new pixel circuit. By utilizing this circuit, we can achieve high-speed and stable operation for medium-sized notebook displays while ensuring excellent display quality. Additionally, by using only IGZO, we eliminate the need for a hybrid process involving LTPS and IGZO, as seen in LTPO technologies, thereby enabling lower-cost manufacturing. We prototyped this demo panel using nanoLEDs. By combining the characteristics of nanoLEDs—such as a wide color gamut, high brightness, and long lifetime—we anticipate being able to deliver displays with even greater value in the near future.

6. Reference

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