Integrated Glass Substrates for Advanced Display and Electronic Applications

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Abstract

Engineered glass substrates optimized for material attributes, form factors, and innovative processing capabilities are crucial for emerging high-performance display and non-display applications. Through system-level optimization, these advanced substrates enable the heterogeneous assembly of electronic and opto-electronic devices supporting current applications, as well as, shaping the future technology roadmap.

Author Keywords

glass substrates; displays; electronics; opto-electronics; engineered substrates

Glass substrates are currently used for a wide variety of display and non-display applications. Engineered glass compositions and forming methods have been specifically optimized to enable innovative progress in active-matrix backplanes, display technologies, and mechanically durable cover glass. Similarly, glass wafers are being used for semiconductor device processing and packaging, including fan-out and 2.5D/3D packaging, wafer thinning, 3D bonding, and temporary carriers.[1] These display and non-display applications value a key set of glass intrinsic and extrinsic attributes, such as surface quality, low warp and Total Thickness Variation (TTV), optical performance, thermo-mechanical stability, thermal expansion, Youngs modulus, hermeticity, and environmental durability. Optimized unique attribute sets for these applications have been scaled up to Gen10 glass sheets and 450 mm wafers.

Emerging high-performance display and non-display devices, however, require a new level of substrate integration. In addition to attributes that derived from the glass compositions and forming methods, new substrate and device processing capabilities are required. Beyond the now standard additive and subtractive processes, substrates must be designed for and truly enable heterogenous assembly of hybrid electronic and opto-electronic devices. New assembly approaches such as pick-and-place and micro-transfer printing are being explored. This heterogenous integration utilizes the optimal material for each functionality and achieves new device designs, high-throughput manufacturing methods, and enhanced performance levels. Examples of these emerging applications include: microLED displays, micro-driver ICs, glass core, co-packaged optics, mmWave communication, die-embedded packaging, frequency-selective and refractive-impedance surfaces, foldable displays, LIDAR, as well as, lighting and photovoltaics.[2,-8] These emerging applications require the substrate to have a higher level of integration within the device design and functionality through its material attributes, form factor, and processing capability.

Substrate material attributes can be tailored over wide ranges to meet device and application requirements. As the degree of integration increases, a system-level optimization is required. The substrate is not a stand-alone element but is highly influential in the device and system performance. It should be noted that although glass is referred to, glass-ceramic and ceramic substrates may be the optimal material depending on the application. The substrate can also be comprised of laminates or multi-layers that include these material families. Identifying the correct substrate composition is a multi-parameter optimization. Table 1 illustrates example glass attribute ranges that different applications may value combinations of. By engaging in technically challenging research & development, glass scientists have often been able to balance many competing composition and manufacturing factors and exploit new and unexpected behaviors of glass materials to achieve desired substrate attributes. Similar to glass, ceramic substrates such as alumina are options that can achieve low RF loss ($\sim 10^{-4}$), and high thermal conductivity (>36W/mK) to enable high power electronics.[8]

Substrate form factors and processing capabilities are also critical for device integration. As mentioned, both wafer and sheet formats are possible, and thicknesses can range from <100 µm to >2 mm. Corning's advanced fusion forming capability provides as-formed surfaces with Ra roughness < 3Å, TTV < 2 µm, and panel warp << 500 µm.[1] After forming, the substrate can be further processed to create device-level features

ISSN 0097-996X/25/5602-1227-$1.00 © 2025

required for true integration. Examples of this include the formation of surface features, through-glass vias (TGV), ion-exchange for strengthening or waveguide formation, and laser-written waveguides.[1,8-12] Singulation after device fabrication is also critical [13], especially for applications such as tiled microLED displays that require precision sizes. Capabilities exist for precision cutting and edge finishing within 100 µm of device structures that have edge accuracy ~10 µm and chamfer widths <60 µm.[14]

Table 1. Glass substrate example attribute ranges.

Attribute	Example ranges
CTE	3-10 x 10^{-6}/°C
Youngs modulus	65-83 GPa
Dielectric constant and loss tangent (@ 10 GHz)	Dk: 4.6 – ~7 Df: 0.003 – 0.03
Optical transmission, UV cut-off (90% knee)	220-320 nm (320-420 nm)
Strain point	570-750°C
Refractive index (λ = 587 nm)	1.458-2.00

Devices can be fabricated and assembled on these engineered substrates using a variety of high-throughput sheet and wafer capabilities. In addition, carrier substrates and roll-to-roll processing can be utilized with flexible form factors.[8] Examples of device processing include: TGV metallization, redistribution layer (RDL) patterning with line/space dimensions < 5/5 µm, wrap-around electrode patterning (Figure 1) with lines/space dimensions down to 20 µm / 20 µm.[1,4,14-16] In terms of overall device integration, the substrate attributes, form factors, and process capabilities have been utilized in the heterogenous assembly of display and non-display applications with microLED, micro-IC, and Si die components.[2,17]

In summary, engineered glass substrates enable emerging high-performance display and non-display applications by optimizing material attributes, form factors, and innovative processing capabilities. A system-level approach is essential to optimize the specific attribute combinations required for targeted device designs, performance levels, and manufacturing processes. This optimization has enabled the heterogeneous assembly of electronic and opto-electronic integrated devices. These capabilities not only support current applications but also play a critical role in shaping the future technology roadmap.

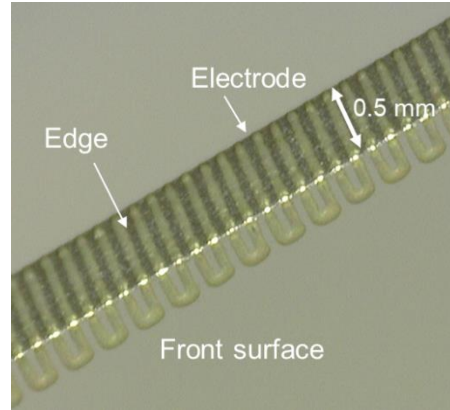

Figure 1. Wrap-around electrode patterning of 50 µm lines and spaces for tiled and borderless displays. The glass substrate has a precision edge finish with a <60 µm chamfer.

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