Silicon-on-Nothing Technology Based on Silicon Migration in Argon Annealing for Display-Sensor Integration

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Abstract

For applications involving interactive display-sensor systems, this study investigates silicon migration technology using argon annealing for low-cost silicon-on-nothing structures to improve integration compatibility. Argon-based rapid thermal processing offers enhanced safety and cost reduction compared to hydrogen-based methods. The results demonstrate the successful formation of in-situ-sealed silicon diaphragms with uniform thickness and varying dimensions for pressure sensing applications.

Author Keywords

MEMS pressure sensor; silicon-on-nothing; silicon migration; silicon diaphragm

1. Introduction

In interactive display-sensor systems and the Internet of Things (IoT), displays serve as the core output interface, while MEMS sensors are crucial for input functions. With their rapid growth, the demand for MEMS sensors, especially those that can integrate with displays and ICs, has increased significantly.[1] This has led to a growing need for MEMS sensors that are cost-effective, efficient to manufacture, and capable of integration with other electronic components.

However, traditional silicon-based MEMS fabrication techniques face several challenges, such as poor dimensional control, process inefficiency, and limited compatibility with display and IC processes.[2-5] The complexity of conventional etching processes and the fragility of MEMS structures hinder the integration of MEMS sensors with displays and IC circuits, restricting the development of interactive and integrated smart systems.

Silicon-on-Nothing (SON) technology offers a promising solution. SON has been successfully applied in the fabrication of high-performance optical, capacitive, and piezoresistive pressure sensors, with significant improvements in cost, efficiency, and performance.[6-8] A major advantage of SON is its suitability for monolithic integration, allowing for the fabrication of suspended MEMS structures with surface integrity, making it compatible with subsequent display and IC processes. Previous studies have demonstrated successful monolithic integration of SON-based tactile sensor arrays with CMOS circuits[9] and gas sensor arrays with active-matrix architecture based on metal oxide thin-film-transistors (TFTs)[10]. These advancements indicate that SON technology has great potential for monolithic integration with silicon-based displays (such as MicroLED and MicroOLED) as Sensor-in-Pixel, enabling the development of next-generation interactive and sensor-integrated smart display systems.

Despite these benefits, the adoption of SON is limited by high costs, specialized equipment, and safety concerns related to hydrogen-assisted processes. Argon provides a safer, more cost-effective alternative for SON production. This study investigates the application of argon annealing to improve the thickness and uniformity of silicon diaphragms, critical for enhancing the performance of MEMS pressure sensors.

2. Principles and Designs

The silicon migration effect arises from the mass transport of silicon atoms driven by surface diffusion at temperatures below the silicon melting point. This migration is governed by a physical phenomenon in which atoms move in response to a chemical potential gradient, driven by surface energy non-uniformity. The chemical potential varies across the surface due to energy disparities, with atoms moving from regions of higher to lower chemical potential. The Gibbs free energy, which quantifies the surface energy state, is expressed in Equation 1:

$$G_S = \gamma A \quad (1)$$

where γ represents the surface energy density and A denotes the surface area.[11] The chemical potential μ_i, associated with surface energy, is derived from the change in Gibbs free energy per particle, as shown in Equation 2:

$$\mu_i = \frac{\partial G_S}{\partial N_i} \quad (2)$$

where N_i is the number of atoms of the i_{th} species.[11] The incremental change in surface area, δA, resulting from the addition or removal of an atom, is given by:

$$\delta A = K\Omega \quad (3)$$

where K is the sum of the principal curvatures and Ω is the atomic volume.[11] This leads to the local chemical potential at the surface:

$$\mu_S = \gamma K \Omega \quad (4)$$

The migration rate of atoms is influenced by the surface diffusion coefficient, temperature, and chemical potential gradient, forming an atomic flux determined by atom concentration and drift velocity. This migration process reshapes the solid surface to minimize energy and optimize its state.

The surface-normal velocity v_n, driven by surface diffusion, is described by Equation 5:

$$v_n = \Omega \nabla_S\left(\frac{D_S X_S}{k_B T} \nabla_S(\gamma K \Omega)\right) \quad (5)$$

where X_S is the surface particle concentration. A key parameter in this process is the surface diffusion coefficient D_S, which influences the migration rate.[11] Previous studies have shown that D_S is affected by annealing temperature, atmosphere, and pressure.[12] Migration rates in various inert gases are similar within experimental error, and silicon migration can occur without hydrogen or ultra-high vacuum environments.[13] This discovery opens the possibility of low-cost silicon migration processes with significant practical applications.

Based on these principles, the following process flow is designed, as shown in Figure 1. First, photolithography is used to create a hole array pattern on a photoresist layer (Figure 1a). Dry etching is then employed to form wells with a specific depth-to-width ratio (Figure 1b). The subsequent thermal treatment triggers silicon surface migration, causing the cavities at the well bottoms to expand and merge, while the well openings close, forming a continuous cavity sealed by a silicon diaphragm (Figure 1c).

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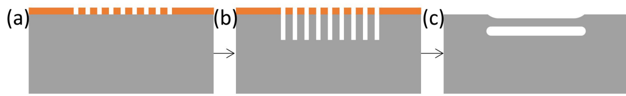

Figure 1. Schematic diagram of the process flow. (a) Lithography. (b) Dry etching. (c) Photoresist removal and annealing.

For the well array design, two layout configurations were explored: an orthogonal matrix (Figure 2a) and a hexagonal matrix (Figure 2b). The diameter (d) of each cylindrical well and the inter-well spacing (s) are key design parameters that influence the formation of a continuous diaphragm and cavity, as well as their respective thicknesses. Seven different s/d ratios and five silicon diaphragm sizes, ranging from 100 × 100 μm to 200 × 200 μm, were designed. The well arrays for each diaphragm were uniformly arranged, maintaining constant s and d throughout.

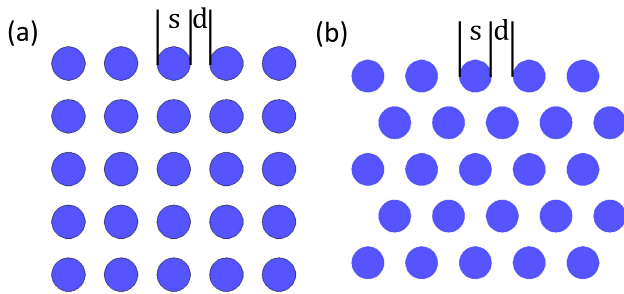

Figure 2. Layout configurations: (a) an orthogonal matrix and (b) a hexagonal matrix**.**

3. Experiments

In this experiment, 8-inch phosphorus-doped Czochralski (CZ) silicon wafers with a resistivity of 1-10 Ω·cm were used as substrates. The process began with photolithography, using an i-line stepper system to transfer patterns from a mask onto a photoresist layer. Critical dimensions were controlled to ensure uniformity within and between wafers. Uniformity is crucial because, during annealing, large wells may form spherical cavities due to surface energy reduction (Figure 3). For well arrays, an optimal inter-well distance ensures the merging of multiple spherical cavities into a larger one. Consistent aperture size and well spacing promote pore closure. Irregularities, such as sparse or smaller apertures, can result in discontinuous cavities or silicon pillars, while dense or enlarged apertures may lead to unclosable large openings. The photoresist layer and aperture profile after development were examined using FIB-SEM (Figure 4).

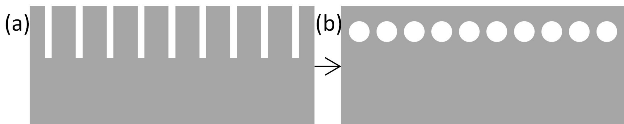

Figure 3. Schematic diagram of annealing morphology changes resulting from excessive s/d. (a) Before annealing. (b) After annealing.

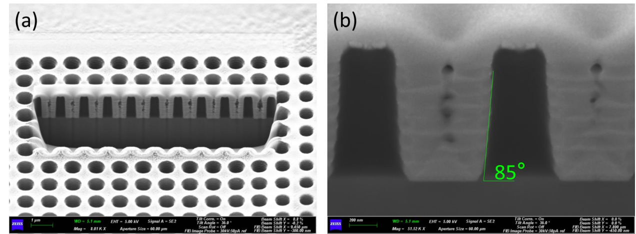

Figure 4. (a) A FIB-SEM image of the photoresist layer after development. (b) The profile of apertures.

After photolithography, the wafer underwent well array etching, with the photoresist acting as a dry etching mask, enhanced by pre-treatment for aperture accuracy. Bosch DRIE etched wells 3-6 microns deep, with varying depths to study the effect of aspect ratio on diaphragm formation. Etching results, shown in Figure 5, include FIB and SEM cross-sections. Sidewall etching slightly enlarged the top apertures, with verticality at 88-89 degrees and narrowing at the well bottom.

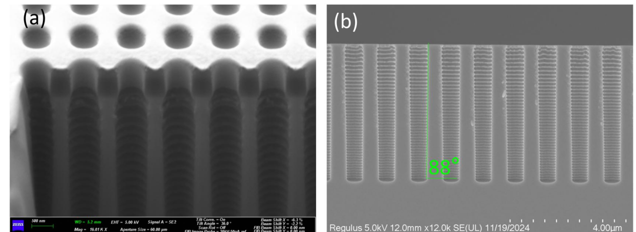

Figure 5. (a) A FIB-SEM image of the well arrays with a photoresist layer as a mask after DRIE etching. (b) The SEM profile view of wells after photoresist removal.

The silicon wafer was then subjected to high-temperature annealing after pre-treatment to promote silicon atom migration. Annealing took place in a reduced-pressure argon environment in an RTP furnace, heated above 1000 °C but below the melting point of single-crystal silicon. Various annealing temperatures and durations from 5 to 30 minutes were tested to examine their impact on diaphragm formation. RTP heating, primarily through thermal radiation, provided the energy necessary for silicon atom migration, ensuring pore merging into a uniform diaphragm with continuous cavities. During cooling, constant pressure within the RTP chamber was maintained to prevent diaphragm bending and re-fusion due to pressure differences. After cooling, the wafer was removed at atmospheric pressure. Although the silicon film curved due to the pressure difference, it did not adhere to the substrate.

4. Results and Analysis

As shown in Figure 6, silicon diaphragms were successfully fabricated under argon RTP annealing conditions, using various well array designs with different aperture spacings. The diaphragms, ranging in size from 100 to 200 μm, exhibited no adhesion to the substrate in the largest samples, confirming the method's reliability and versatility. Notably, the concave silicon diaphragms displayed a mirror-like effect under optical microscopy, indicating complete sealing and the absence of silicon pillars within the cavity. Under optimal design and processing conditions, the diaphragm formation rate exceeded 99%, providing a solid foundation for future research and applications.

Figure 6. Seven designs of s/d with two types of well array arrangement and their respective five different scale sizes were capable of forming diaphragms.

Figure 7 presents optical microscope images of 200×200 µm, 150×150 µm, and 100×100 µm silicon diaphragms, displaying clear concentric ring patterns, or Newton's rings, formed by diaphragm deformation due to external pressure. This effect further confirms the diaphragm's effective sealing and the integrity of the cavity, which remains isolated from the external environment. Under identical atmospheric pressure conditions, larger silicon diaphragms experience greater deflection, resulting in varying gaps with the substrate and producing distinct interference fringe patterns. Notably, the number of Newton's rings remains consistent for the 200 µm and 150 µm diaphragms, as shown in Figures 7(a) and 7(b). This consistency occurs because the center of the 200 µm diaphragm contacts the substrate at standard atmospheric pressure, preventing any further gap changes.

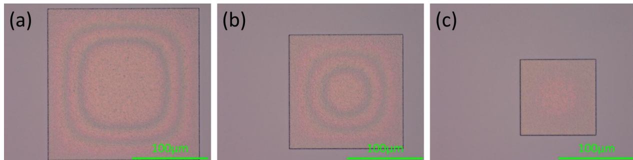

Figure 7. Under an optical microscope, the shapes or numbers of Newton's rings exhibited on silicon diaphragms of sizes (a) 200 × 200 µm, (b) 150 × 150 µm, and (c) 100 × 100 µm differ.

To assess diaphragm deformation, COMSOL simulations were conducted. The deformation simulations for silicon diaphragms with sizes of 200 µm, 150 µm, and 100 µm at one atmosphere on one-side are shown in Figures 8(a), 8(b), and 8(c), respectively. For the 200 µm diaphragm, the maximum deformation of 2.04 µm occurs at the center. Given the cavity thickness of 0.8 µm, contact between the diaphragm and substrate occurs at this pressure. The correlation between deformation and diaphragm size at 1 atm is shown in Figure 9(a). The relationship between deformation and applied differential pressure for the 200 µm diaphragm is shown in Figure 9(b), suggesting the potential of the silicon diaphragm as an pressure sensor.

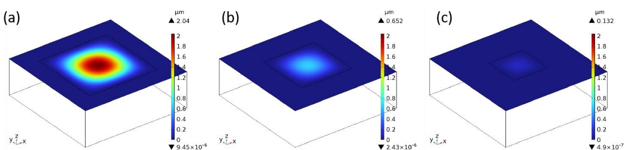

Figure 8. Simulation of maximal deformation at one atmosphere of silicon diaphragms are (a) 2.04 µm of sizes 200 × 200 µm, (b) 0.652 µm of 150 × 150 µm, and (c) 0.132 µm of 100 × 100 µm.

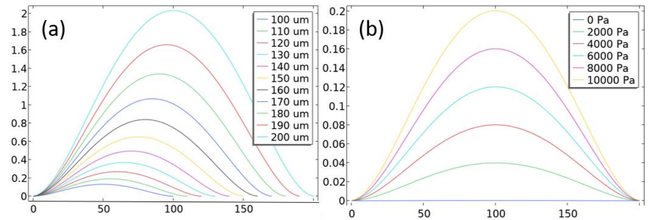

Figure 9. (a) The relationship between deformation and diaphragm size under a pressure of 1 atm. (b) The correlation between deformation and external pressure of 200 µm diaphragm.

The 200 µm diaphragms of two designs with different s/d ratios, along with their corresponding cross-sectional images obtained via FIB cutting, are shown in Figure 10. As illustrated in Figures 10(a) and (b), at the silicon diaphragm-substrate junction, the upper surface of the diaphragm was slightly lower than the substrate surface, likely due to silicon vacancy migration during annealing. Vacancies migrated to the lower side of the diaphragm, forming the cavity, while others shifted to the upper side. As shown in Figures 10(c) and (d), after cutting, internal and external pressures were equalized, and the diaphragm returned to a flat state, confirming no adhesion to the substrate. Measurements at multiple points confirmed the uniformity of the diaphragm and cavity thicknesses. Specifically, Design 1 has a diaphragm thickness of 2 ± 0.1 µm and a cavity thickness of 0.75 ± 0.1 µm, while Design 2 has a diaphragm thickness of 2 ± 0.1 µm and a cavity thickness of 0.95 ± 0.1 µm. Both designs exhibit no fractures, and the cavities have smooth walls without silicon pillars.

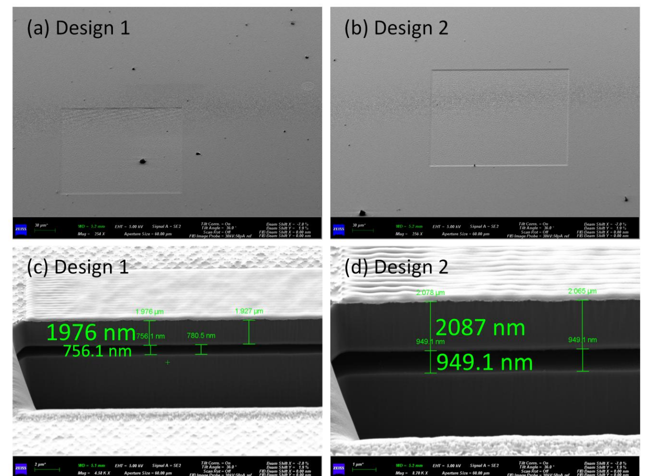

Figure 10. (a) Silicon diaphragm of design 1. (b) Silicon diaphragm of design 2. (c) Diaphragm cross-section of design 1. (d) Diaphragm cross-section of design 2.

It is important to note that diaphragm and cavity thicknesses cannot be directly predicted from the well array aperture spacing and etching depth alone, as these depend on the distribution of vacancies and annealing conditions. However, under consistent annealing and etching conditions, the ratio of diaphragm thickness to cavity thickness correlates with the well array's s/d ratio. Larger s/d ratios result in fewer vacancies and a higher diaphragm-to-cavity thickness ratio, while smaller ratios lead to more vacancies and a lower ratio. As shown in Figures 10(c) and

(d), Design 1, with a slightly larger s/d ratio than Design 2, yielded thicker diaphragms and thinner cavities, providing insights for tailoring diaphragm thickness in MEMS sensor design.

Post-annealing, traces of the well array pattern remained on the diaphragm surface, as shown in Figure 11(a), exhibiting a roughness of approximately tens of nanometers, as shown in Figure 11(b). This roughness is likely due to surface barriers in the annealing atmosphere, which hindered further silicon migration and prevented complete flattening of the surface. The elimination of this roughness will be studied by extending the annealing time to investigate whether silicon migration can continue. Irregular surface roughening was also observed on the silicon substrate, potentially due to the formation of volatile silicon oxide during oxygen interaction in the RTP chamber.[14] The reaction between silicon and native oxide may have caused non-uniform etching of the surface, as shown in Figure 11(a). Future work will focus on using higher-flow argon to purge oxidative components, reducing the native oxide layer, ensuring better chamber sealing, and thus reducing surface roughness, which will improve the quality and of the silicon diaphragms.

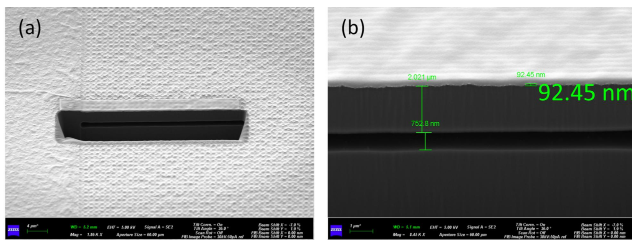

Figure 11. (a) FIB cutting at the diaphragm-substrate junction. (b) Enlarge cross-section view of the traces of the well array pattern.

5. Discussion

Pressure-sensitive diaphragms are crucial for MEMS sensor performance. Traditional silicon etching techniques face challenges in precision, uniformity, and scalability, primarily due to high costs and complexity. While SOI wafers address some of these issues, their inefficiency and expense remain drawbacks.

SON technology simplifies the fabrication process, enabling the cost-effective production of high-quality diaphragms and cavities. It offers precise patterning, prevents lateral expansion, and produces ultra-thin diaphragms with controlled thickness, making it suitable for MEMS sensors. Furthermore, SON integrates seamlessly with other semiconductor processes, especially for monolithic IC integration.

This study demonstrates the successful application of argon RTP annealing for SON thin diaphragms, providing a safer, more environmentally friendly alternative to hydrogen annealing. Surface roughness remains a challenge, but further improvements in annealing process and chamber conditions will enhance diaphragm quality.

SON technology not only shows great promise for silicon-based display applications, but also is suitable for heterogeneous integration with glass-based displays, particularly for under-display sensors. This is because the ultra-thin diaphragm and cavity allow the sensing units to have a thickness ranging from several microns to tens of microns. Thus, it has potential in applications such as touch sensing and fingerprint recognition.

6. Conclusion

This study demonstrates the successful application of SON with argon annealing in MEMS pressure sensor fabrication. SON simplifies the process, reduces costs, and enhances diaphragm integration. Compared to traditional methods, SON offers advantages in uniformity, thickness control, and monolithic IC integration. Argon RTP annealing addresses safety and cost issues associated with hydrogen annealing, providing a safer and more efficient alternative for large-scale production. Furthermore, it demonstrates potential for the integration of MEMS and displays, paving the way for future interactive smart display systems.

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