Process Development for Active-Matrix-Addressed Liquid-Crystal Reconfigurable Intelligent Surfaces

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Abstract

This work presents the design and development of an active matrix addressed liquid crystal based RIS for 28 GHz centre frequency as well as the fabrication and characterization of a column-wise direct-addressed 16x16 unit-cell prototype. For the implementation of low loss RF electrodes, a micro-galvanic copper deposition process has been integrated and optimized and the process compatibility with a-Si:H TFTs has been shown.

Author Keywords

Reconfigurable intelligent surface; liquid crystal; 6G; copper; micro-galvanic deposition; active matrix; thin film transistor.

1. Introduction

With the demand for higher data throughputs and transfer speeds, the bandwidth and thus frequency of telecommunication systems are steadily increasing. With that arise new challenges such as increased impact of line of sight blockage resulting in weak to no signal reception indoors or behind obstacles. Reconfigurable intelligent surfaces (RIS) are therefore gaining increasing attention for their potential to extend the coverage of wireless networks at significantly lower costs compared to alternative solutions such as additional base stations or repeaters. RIS allow steering the reflection of impinging waves in a desired, configurable direction. This can be achieved by an array of reflective unit cells which can be separately addressed and tuned to individually change the phase of the wave. The most common technologies to achieve the required phase change include PIN diodes, varactor diodes and liquid crystal. Among these, liquid crystal is in a unique position as it is suitable for frequencies far beyond 1 GHz with costs estimated to be comparatively low due to the mass adoption in display technology, while also offering a continuous tunabilty at low energy consumption.

2. Multi Resonant RIS Based on Liquid Crystal

In contrast to other LC based prototypes [1, 2], the design proposed in this work is based on multi resonant structures, designed for a centre frequency of 28 GHz. The size of the unit-cell was chosen to 4.5 mm x 4.5 mm, which is below $\lambda/2$ to avoid grating lobes but large enough for the two dipoles to resonate with minimal coupling to adjacent cells. [3]

The proposed unit cell design, as illustrated in Figure 1, consists of two dipoles of different lengths and a slotted patch separated by liquid crystal material. This way, the unit cell has several resonances, which increases the bandwidth of the RIS.

Most RIS concepts based on liquid crystal are designed for LC thicknesses between $0.1\ \lambda$ to $0.01\ \lambda$ [4, 5], while the design in this work is aimed at approximately 20 µm, which is $< 0.002\ \lambda$. This way, not only the switching times can be significantly reduced but also the amount of liquid crystal needed.

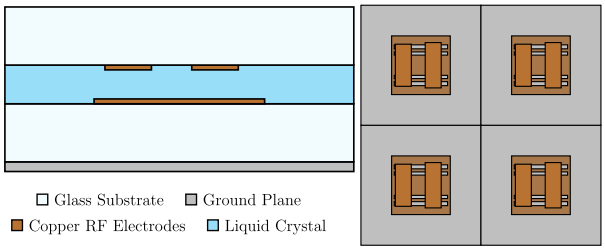

Figure 1. Simplified schematic of the multi-resonance RIS: Cross-section (left) and top view (right, LC not shown).

As the permittivity of the liquid crystal molecules is different along their long and short axes, the resonances can be influenced continuously by applying a bias voltage that changes the orientation of the molecules and therefore the effective permittivity around the resonant structures which ultimately influences the phase of the unit cell.

3. Process Technology for the Fabrication of Liquid-Crystal-Based RIS

Low-loss electrodes for a frequency range around 28 GHz pose unique challenges for the manufacturing processes of these RIS devices. As thicknesses of several micrometres are required, typical thin-film technologies, which are designed for film thicknesses of a few tens to a few hundred nanometres, are no longer suitable. Furthermore, the fabrication of liquid crystal cells comprising these electrodes is equally challenging, as the cell gap must be at least four to six times greater than in display technology in order to be able to sufficiently tune the individual elements. For this, special fabrication processes have been developed on which the presented 16x16 direct-addressed RIS prototype is, and future active matrix devices shall be based on.

Micro-Galvanic Deposition of Copper on Glass: Micro-galvanic deposition combines photolithographic processes (to form a mould) with electroplating. This allows for high lateral resolution at large film thicknesses. Compared to typical thin-film deposition techniques, micro-galvanic deposition allows for thicker films and therefore higher conductivities, while maintaining lateral feature sizes <10 µm (line and space). Electrochemical depositions require a conductive substrate surface. Gold (Au) is a very well-suited material as a seed layer, as it has not only good electrical properties, but it is also not susceptible to oxidation. However, gold does not adhere well to most dielectric materials and therefore an intermediate adhesion layer is required. For this, chromium (Cr) was chosen for its exceptional adhesive properties.

Unlike typical subtractive processes, in which the functional layer is deposited across the entire surface and then removed where not

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needed, the Cu depositions performed in this work are additive. The copper is grown into a photoresist mould that is inverse to the desired pattern. A cross-section of the basic deposition scheme is shown in Figure 2.

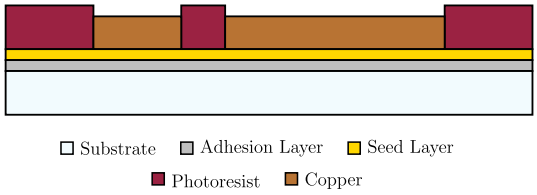

Figure 2. Schematic cross-section of a basic micro-galvanic deposition of copper into a photoresist mould.

This approach offers many advantages over other alternatives. One of them being that there is no subsequent etching step required to structure the thick copper layer. An alternative approach would be to pattern the seed and adhesion layers first and then deposit copper. However, this entails that copper would not only grow in height but also in lateral dimensions, decreasing lateral resolution. Additionally, the current density during the copper deposition would be altered locally depending on feature sizes, resulting in very inhomogeneous layer properties. This would also require all the patterns to be interconnected electrically, making mask design and further processing challenging at best, especially with the integration of an active matrix.

For the process depicted above, several photoresists were experimentally investigated for their pattern profiles at thicknesses of approximately 5 µm, as well as their stability regarding the electroplating chemicals. The negative tone photoresist AZ® 15nXT was chosen for its exceptionally steep edge profiles as shown in Figure 3. As the copper is grown into the photoresist mould, the edge profile of the Cu is determined by the resist profile.

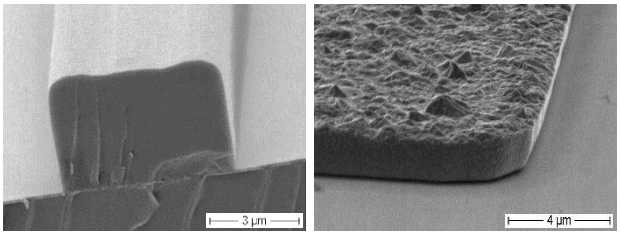

Figure 3. SEM images of the edge profiles of ~5 µm thick AZ® 15nXT (left) and ~2.5 µm thick copper (right).

The film growth during the electroplating process is dependent on the conductivity of the substrate's seed layer. Therefore, inhomogeneities in thickness, roughness as well as conductivity of the resulting copper layer can be expected with faster growth close to the contacts of the power supply. The coefficient of variation, i.e. the normalized root-mean-square deviation, of the thickness of more than 48 % across 72 mm for initial depositions could be reduced significantly to 20 % by decreasing the deposition current and even further, down to 8 % by adding additional contacts on the opposite side of the substrate.

Wet-etching of adhesion and seed layers turned out to be difficult as it requires techniques which can etch gold and chromium selectively to copper. Although also etching copper, sputter etching proved to be most reliable for the removal of the thin adhesion and seed layers. Due to its comparably high thickness, less than 10 % of the copper was removed while removing the exposed areas of the underlying Au and Cr layers entirely.

Fabrication of Liquid-Crystal-Based RIS Cells: In liquid crystal displays (LCDs), the liquid crystal (LC) is commonly addressed via indium tin oxide (ITO) electrodes, however this is not possible in this case as the losses of ITO are too high at the considered frequency. Instead, the RF electrodes are used to bias the LC material, by interconnecting them column-wise with thin lines. The width of the lines was chosen to be 10 µm, the minimum according to the design rules, keeping losses to a minimum.

A thin layer of silicon nitride (Si_3N_4) was deposited on top of the copper RF electrodes to prevent direct contact with the liquid crystal and protect the copper from oxidation and corrosion.

To achieve a well-defined cell thickness of ~20 µm between the copper electrodes, typical spherical spacers sprayed onto the entire substrate are not suitable as the cell thickness would deviate by the thickness of the electrodes. Instead, photolithographic spacers made from SU-8 photoresist have been implemented as they can be positioned precisely.

For the initial orientation of the LC molecule a polyimide film is spin coated on top which is subsequently rubbed to create a microstructure to which the molecules align to. This rubbing step is usually performed using a fast-rotating velvet roller which is moved across the polyimide film. However, due to the high aspect ratio of the lithographic spacer this may cause the spacers to detach. As an alternative, the rubbing was performed with a modified screen printer by swiping a carbon fibre brush across the substrates, as shown on the left in Figure 4. With both methods the spacers cast a "shadow", i.e. an area behind the spacers which cannot be reached by the fibres. Placement of the spacers is therefore critical to not influence the performance of the unit cell.

Precise cell assembly and curing of the glue frame was performed with a mask aligner using a special vacuum chuck as shown on the right in Figure 4. With that, the glass substrates can be aligned with a precision < 10 µm.

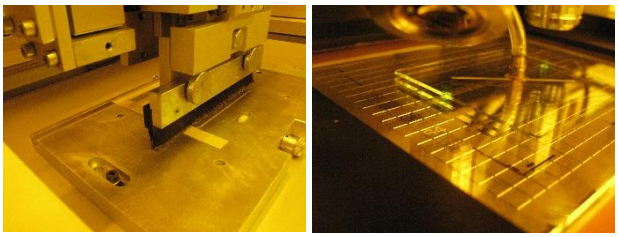

Figure 4. Rubbing process (left) and cell assembly (right).

Due to the comparatively thick cell gap and thus larger amounts of required LC material, a special filling procedure was needed. Filling is performed in a vacuum chamber where the cell and a container with sufficient LC material are placed on a tilt table. After pumping down the chamber to a medium vacuum, the table is tilted such that the LC flows to the cell opening, wetting and sealing it. Upon venting, the pressure introduced back into the chamber pushes the LC material into the cell.

4. Active Matrix Addressing for RIS

To achieve a high reconfigurability in large RIS implementations, the phase shift of hundreds and thousands of unit cells needs to be controlled individually. For that, an active matrix addressing scheme, similar to large LCDs, is most suitable. Though at increased manufacturing complexity and costs by introducing a thin

film transistor (TFT) in each unit-cell, the required connections for driving are significantly reduced compared to a direct-addressed scheme. The transistor of a unit cell acts as a switch via which the cell can be addressed. Thereby, the state written to unit cell is maintained while the transistor is switched off. The introduction of TFTs in each cell makes them independent to a certain extent, which prevents crosstalk and a reduction in the voltage selection ratio (SR), as can be observed in passive matrix systems [6]. This results in a wide range for tuning the phase, which is essential for the RIS.

Co-Fabrication of TFTs and Cu Electrode: Compared to LCDs, the main difference in terms of technology is the thick RF Cu electrodes instead of thin ITO pixel electrodes. Therefore, it is necessary to combine the processes for fabricating TFTs with the processes of micro-galvanic deposition. As a proven backplane technology for active matrix liquid crystal displays (AMLCDs), amorphous silicon (a-Si:H) TFT technology [7] was chosen for a first active matrix RIS prototype.

Figure 5 depicts the front view and schematic cross-section of a fabricated inverted-staggered a-Si:H TFT with Cu electrode. The first step in the TFT process is sputtering and structuring of the molybdenum-tantalum (MoTa) gate layer. Subsequently, a triple layer consisting of silicon nitride (SiN) as gate insulator, intrinsic amorphous silicon (a-Si:H) as semiconductor, and phosphorous doped amorphous silicon (n^+ a-Si:H) is deposited by plasma-enhanced chemical vapour deposition (PECVD). This is directly followed by another deposition and patterning of a MoTa layer for the drain and source electrodes. Afterwards, the semiconductor is structured by plasma etching and the layers are passivated with SiN. A via is etched through the passivation layer to allow for the drain / source to be in contact with the RF electrode, which is deposited subsequently via micro-galvanic deposition as described above.

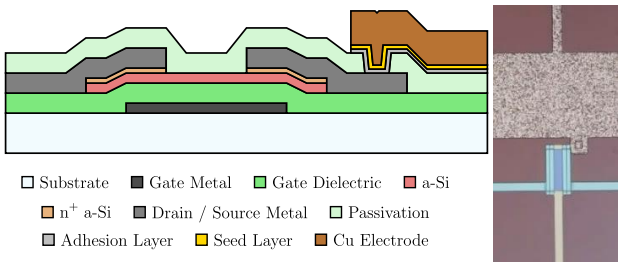

Figure 5. Schematic cross-section of an a-Si:H TFT connected to a Cu electrode (left) and a fabricated device (right).

In Figure 6 the input characteristics of the fabricated transistors are presented. The measurements were carried out before and after performing the micro-galvanic deposition processes. Aside from a slight increase of the off-current, the performance of the TFTs is barely influenced in the operating region.

Design of the Active Matrix RIS: On the basis of AMLCD technology, an active matrix LCRIS has been designed with various changes for RF applications. As mentioned earlier, the LC layer thickness is around 20 µm, which is larger than in optical devices and will lead to a longer response time. According to chapter 2 the unit cell size is designed to be 4.5 mm × 4.5 mm, much larger than a pixel in LCDs. Furthermore, the considered LC mixture GT7-29001 has higher permittivity values than typical display mixtures. As a result, the equivalent capacitance C_{LC} of an LCRIS unit cell is significantly larger. To meet these requirements, a 200 µm × 10 µm TFT and a 16 pF storage capacitor C_{SC} are implemented in every unit cell.

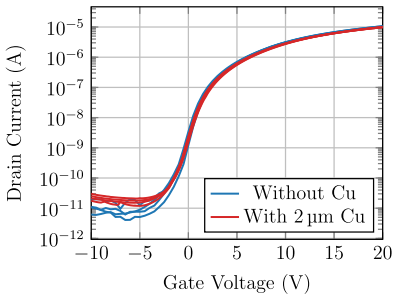

Figure 6. Input characteristics of TFTs before and after the micro-galvanic deposition of copper.

Figure 7 shows the mask design of the unit cell of an active matrix RIS layout. The top resonant structures are interconnected through bias lines, acting as common electrode on the front plane. The bottom patches are linked to the TFTs via metal lines on the backplane. To avoid affecting the RF performance of the RIS, the connection between the metal line and the patch is placed in the centre of the patch, where the current from the high frequency signal is minimal so that no RF power gets into the line [8].

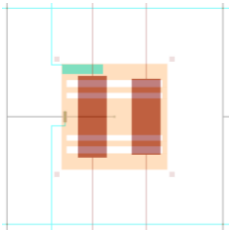

Figure 7. Mask design of a unit cell with TFT and storage capacitance.

5. Experimental Results

Based on the processes described above, a column-wise direct-addressed LCRIS prototype was fabricated and subsequently characterized. It comprises 16 × 16 unit cells on glass substrates and custom driving electronics with 8 bit digital-to-analogue converters (DACs). The direct-addressed prototype acts as a precursor for current and future efforts for developing and fabricating active matrix devices.

Column-wise direct-addressed RIS: The finished prototype fixture including driving electronics and absorber material can be seen on the left and mounted in the calibration setup [9] on the right in Figure 8.

Figure 8. Direct-addressed RIS prototype (left) and array calibration setup (right).

Although designed for 28 GHz, the largest phase change of 276 ° could be observed at 29.5 GHz by addressing the RIS with voltages between ±10 V at a refresh rate of 120 Hz (see Figure 9).

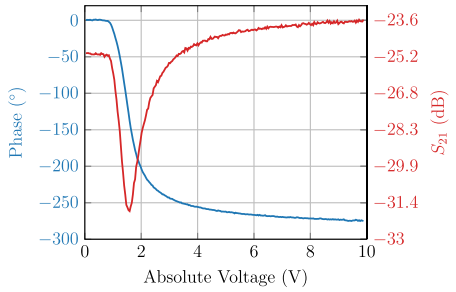

Figure 9. Array calibration results at 29.5 GHz.

The characterization was conducted in an anechoic chamber as shown in Figure 10. The prototype (DUT) was mounted to a stationary but turnable pole and was illuminated broadside. Therefore, the relative orientation of the arm, to which the transmit-antenna (TX) is attached to, and the RIS had to be maintained when revolving around the axis of the pole during the measurement of the reflection by the fixed receive-antenna (RX).

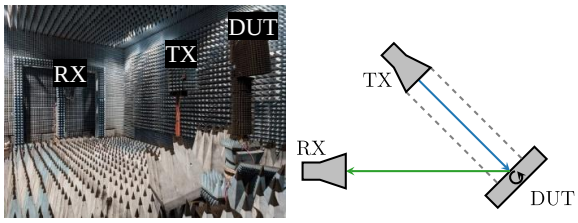

Figure 10. Measurement setup in the anechoic chamber.

The measurement results of a 30 ° reflection and the corresponding phase distribution pattern, the RIS was configured with, is shown in Figure 11. From the raw measurement data, the radar cross-section (RCS) was determined and additionally normalized to the RCS of a simple metal plate. This shows that the RIS has roughly 5 dB_{sm} losses compared to a metal plate reflecting into the same direction.

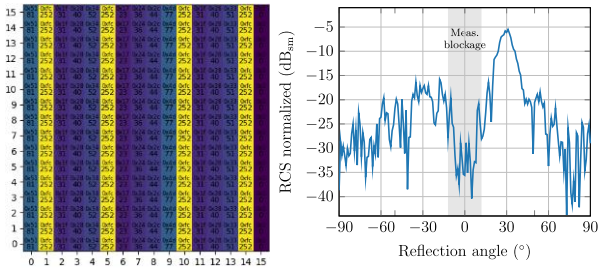

Figure 11. Phase distribution pattern (left) and normalized measurement results of a 30 ° reflection (right).

Active-matrix RIS: Several active-matrix-based LCRIS prototypes have been fabricated based on the design discussed above. Although they have not yet been characterized, the functionality of the devices has been successfully verified optically with the use of polarizers as shown in Figure 12. When cells are addressed a noticeably higher light transmission can be observed around overlapping structures compared to the off state.

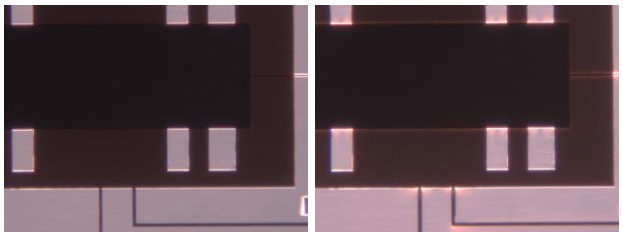

Figure 12. Optical verification: Off (left) and on (right).

6. Conclusion

This work presented the process technology for the fabrication as well as the characterization of a column-wise direct-addressed RIS prototype showing promising results, it was shown that the introduced micro-galvanic processes are compatible with a:Si TFT processes without influencing their performance significantly and finally combining all these findings to fabricate a yet to be characterized, functioning active matrix RIS device.

7. Acknowledgements

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