Multilayer Glass Structure for Advancing Packaging and Substrate Technologies

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Abstract

The rising power demands of AI technologies highlight the need for energy-efficient solutions. While efforts to maximize performance per watt have driven the development of high-density chip integration, traditional organic substrates are reaching their mechanical and electrical limitations.
As a groundbreaking solution, glass substrates have garnered increasing attention for their superior properties. However, challenges such as processing issues associated with Through-Glass Via (TGV) manufacturing and susceptibility to breakage must be addressed to enable their practical application.
This paper introduces a novel multilayer glass structure as a comprehensive solution by sharing these innovative concepts, exploring the technical challenges in glass substrate applications, and discussing their potential impact on advancing packaging and substrate technologies.

Author Keywords

TGV; Metallization; Glass Substrate; Packaging; All-Layer Z-Connection Structure; G-ALCS (Glass All-Layer Z-Connection Structure); Optical Interconnect; 2.5D; 2.3D; 2.1D, 3D Vertical Integration

1. What is G-ALCS

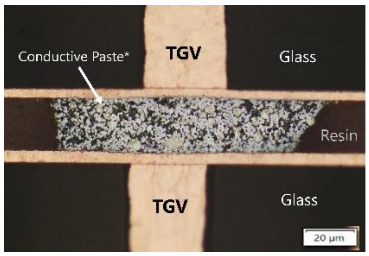
In recent years, the integration of integrated circuits (ICs) into large packages for chiplets and the utilization of glass as a mounting platform for low-energy devices have garnered significant attention.

In fact, the limitations of organic packages, particularly in terms of size, precision mounting, and microfabrication, have driven the need for new solutions.

Glass, recognized for its superior flatness, dimensional stability, and favorable electrical properties compared to silicon and organic materials, has the potential to overcome these constraints and introduce a new paradigm in the packaging industry.

However, one of the major issues facing the practical application of glass substrates is the yielding of high aspect ratio TGV process.

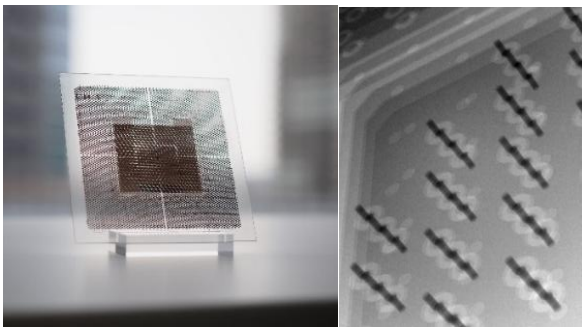
In response to these challenges, we have introduced a new concept consisting in stacking low aspect glass layers that we call G-ALCS (Glass All-Layer Z-Connection Structure). This technology uses our unique conductive paste and an adhesive resin to interconnect glass layers.



*FICT Limited's conductive copper alloy paste originally used for All-Layer Z-Connection Structure Technology (F-ALCS Technology [1]) connecting all the layers in a single lamination process.

Figure 1. Multi-glass core substrate for transmission evaluation

This structure lifts the important limits we encounter in the manufacturing of TGV while proposing a new generation of packaging structure with vertically integrated functions.



(a) Four layers Glass Core (b) X-ray image of TGV

Figure 2. G-ALCS Sample

2. TGV Fabrication Challenges

The conventional Through-Glass Via (TGV) formation process involves modifying the glass layer through laser irradiation using a short pulse wavelength, followed by chemical etching with a hydrofluoric acid solution. For TGVs with high aspect ratios, the aperture ratio (B/A) is low, and the dimensional variation of the diameter is large across the panel, as illustrated in Figure 3 where A and B are indicated. This affects the quality and time of the plating process.

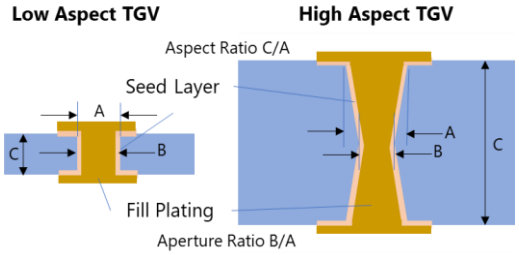


Figure 3. Typical TGV Structure

The challenge in the plating process is to ensure proper adhesion of copper (Cu) and completely fill the TGV during the metallization process.

Below are several challenges that arise during the metallization process:

- **Limited Sputtering Depth for High Aspect Ratios (AR):** When a Ti/Cu seed layer is sputtered to enhance adhesion, the deposition cannot effectively reach the full depth of the via if the aspect ratio is too high, leading to insufficient coverage.
- **Voiding and Incomplete Plating:** As the aspect ratio increases, issues such as void formation in the fill plating and partial non-plating become more prominent, affecting connection reliability.

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- **Trade-off Between Aspect Ratio and Plating Time:** Higher aspect ratios require lower current densities during electroplating, resulting in significantly longer plating times. This presents substantial challenges in maintaining economically viable production methods.

Table 1 presents a productivity comparison based on TGV aspect ratios, where higher aspect ratios correlate with lower yield and reduced productivity.

Table 1. Low AR vs High AR TGV Comparison

TGV critical issue	Low AR	<->	High AR
Aperture ratio	High	<->	Low
Seed layer(PVD)	Easy	<->	Difficult
Fill plating	Easy	<->	Difficult
Plating time	Short	<->	Long
Yielding	High	<->	Low
Productivity	High	<->	Low

3. Productivity Improvement By Stacking Thinner Glass Layers

To solve the issues encountered with high-aspect TGV at the metallization process, we propose a multi-layer glass core with low-aspect TGV layers. This method offers a drastic reduction of the plating time to improve productivity.

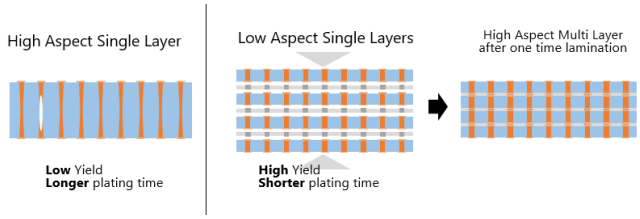

Figure 4. High aspect multi-layer structure with Low aspect TGV

With G-ALCS we manufacture and inspect each glass layer in parallel and select only the non-defective ones for the one-time lamination process to form the glass core.

4. Other Advantages of Multi- Glass Layers Structure

Below is a list of features obtained by the multilayer structure:

- Narrow pitch and high aspect ratio
- CTE stress relaxation enabling the increase of the build-up layers
- Wiring into the core (High-speed global wiring, etc.)
- Ensuring power supply capacity through all fill-vias
- Suitable for Parts embedded
- Photoelectric fusion and integration with optical computing

5. Glass Multilayer Technology for Advanced Semiconductor Package Substrate

Our company unique ALCS technology allows the formation of Any Layer IVH (Interstitial Via Hole) structure.

This brings a new package structure approach consisting in installing a part of the wirings, conventionally situated in the build-up layers, inside the core, and coupling the wirings with built-in components and fine RDL wirings.

Compared to conventional organic packages, it is possible to take advantage of the characteristics of glass substrates while further expanding them to a high level.

Below are examples of advanced packaging substrate structures:

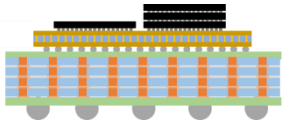

Figure 5. 2.5D structure

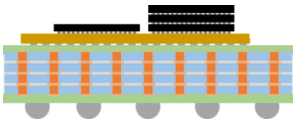

Figure 6. 2.3D structure

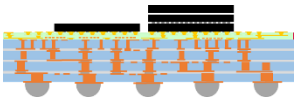

Figure 7. 2.1D Structure

By combining the high-precision mounting and dimensional stability of glass with vertical interconnect technology (G-ALCS), it is possible to form a new function layer in which each layer acts as a function and is vertically integrated.

The function layer would be equipped with specific functions such as power, light, cooling, and chiplets, and designed to be integrated into the substrate in three dimensions (Figure 8).

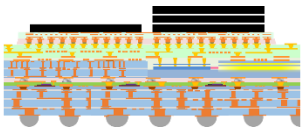

Figure 8. 3D Vertical Integration Semiconductor packaging structure

6. Conclusion

In this paper, we proposed a novel multilayer glass structure to address the challenges we meet toward the development of high-density chip integration, as traditional organic substrates face mechanical and electrical limitations.

By adopting a multilayer approach, it is possible to improve TGV yield and productivity, demonstrating that laminating low-aspect-ratio glass layers is an effective method to achieve a high-aspect-ratio core with enhanced performance.
We also showed that by adapting the multilayering approach new functional value can be achieved, leading to next-generation high-value-added product applications for 3D vertical integration.

To realize advanced semiconductor packaging structures, it is essential to continue advancing substrate technology as an intermediary process that bridges semiconductor microfabrication and large glass panel processing.

Collaboration across various industries remains crucial in leveraging each sector's strengths within the semiconductor value chain. Moving forward, we will continue working with industry partners to refine and expand the application of multilayer glass technology, driving the next generation of high-performance electronic components.

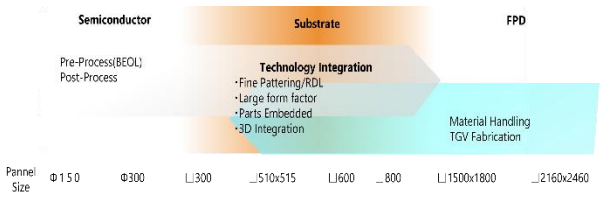

Figure 9. Cross-industry collaboration

7. Acknowledgements

The Author, Takahisa Amemiya, wishes to express gratitude to Akira Tamura, FICT Limited corporate executive advisor, and the R&D team for their invaluable support in the writing of this paper.

8. References

1. F-ALCS (F-All Layer Connection Structure) is an advanced printed wiring board (PWB) technology developed by FICT Limited.
www.fict-g.com/en/technology/falcs.html