Advanced IC Substrate Exploiting Flat Panel Display Technology

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Abstract

The substrate for advanced IC packages is now being plagued by an increasing number of challenges. This paper introduces development activities of JDI (Japan Display Inc.) to address these challenges by leveraging the flat panel display manufacturing technology. This approach is expected to enable finer L/S (line and space), larger substrate size, lower cost, and enhanced performance in this market.

Author Keywords

IC substrate, RDL, package, flat panel display technology

1. Introduction

Along with the rapid growth of the advanced semiconductor market, such as HPC (High Performance Computing) or AI (Artificial Intelligence) Cloud computing, the new semiconductor packaging technologies are being constantly developed. Although these technologies referred to as 2.3D, 2.5D or 3D packaging impose various requirements, the key factors include finer L/S patterning and smaller vias with robust yield and quality on larger substrates to obtain larger and less expensive packages [1].

In this field, the silicon wafer process-based technology has played a significant role [1], [2], and as the next solution, the PLP (Panel Level Package) technology is expected. In addition, based on certain studies indicating the advantageous nature of "chip last" technology, a carrier or core substrate is required to fabricate circuits [3].

For large substrates, glass is highly promising not only from a size perspective but also because of its favorable electrical and mechanical properties [4]. Moreover, JDI has MP (Mass Production) lines based on large-format glass substrates for display production with a size of 730 x 920 mm (Gen. 4.5).

This study conducted an initial evaluation to determine whether proposed concept of the display manufacturing process is compatible with advanced IC substrate manufacturing. Although certain studies address warpage or dimensional fluctuations primarily caused by CTE (Coefficient of thermal expansion) mismatch in packages [5], this study focused solely on the wiring fabrication process. This constitutes a first step toward the realization of the fine-pitch RDL (Redistribution Layer) interposer fabrication on a 730 x 920 mm glass substrate.

2. Experience of Display Manufacturing

Backplane Structure: JDI has MP lines with 730 x 920 mm (Gen. 4.5) mother glass for display backplane production. For typical displays such as LCD, OLED or micro-LED display, the backplane excluding TFT elements comprises 2 or 3 Al wiring layers, ITO layers, insulation layers made of acrylic or PI (polyimide) resin, and inorganic insulation films such as SiN or SiO. For flexible displays, the circuit is fabricated on a PI layer that includes an ablation layer. This enables detachment from the support glass during the LLO (Laser Lift Off) process, which typically occurs at the end of the backplane process. Figure 1 shows part of the backplane structure, indicating that JDI has successfully realized line widths and hole diameters below 2 and 1.5 µm, respectively. However, Al wiring has been adopted for small-size display designs, consequently, we are now considering a Cu process for this technology.

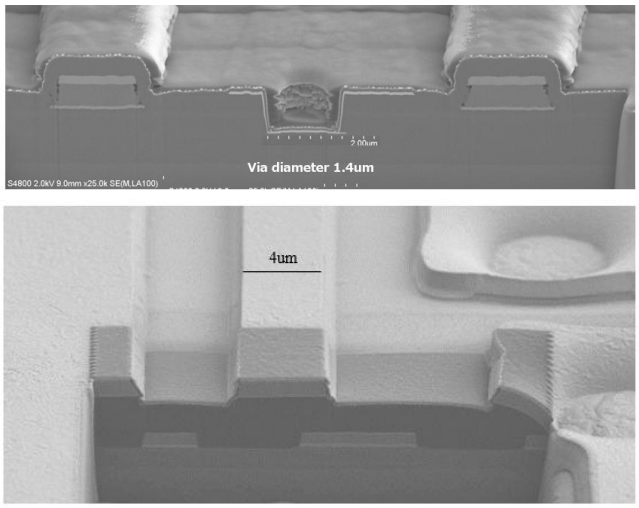
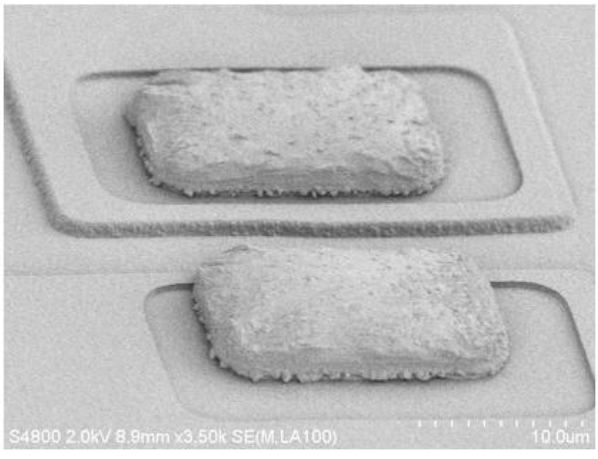


Figure 1. FIB images of the wiring and contact hole on the JDI's display backplane.

JDI has been developing micro-LED display technology, in which more than 10,000 LEDs must be mounted concurrently owing to the high pixel density. Several solutions for bonding LEDs on the backplane have been examined. One option is Sn-Au eutectic bonding; accordingly, we have developed micro bump technology. Figure 2 shows electroplated Cu-Ni-Sn micro bumps with dimensions of 12 x 18 µm and a gap of 10 µm. Over 7.7 million micro bumps are fabricated on a 10-inch diagonal backplane.



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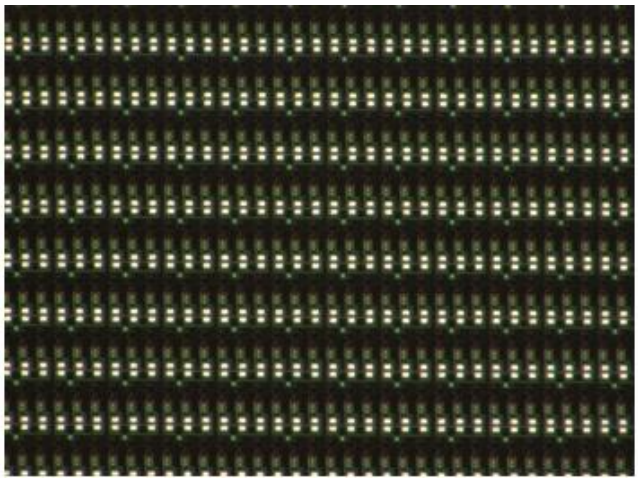


Figure 2. SEM image and microscope photograph of the Cu-Ni-Sn micro bumps on a micro-LED display backplane.

Warpage and dimension fluctuation during the display backplane process: To achieve finer fabrication technology in the display backplane process, we have carefully monitored substrate behavior. Substrates do not remain stationary during fabrication. Figure 3 illustrates the substrate warpage values for various film stack designs. It indicates the warpage value is affected in response to compressive or tensile stress of each film. Figure 4 shows process-to-process dimensional fluctuations. Typically, a strategy of offset dimension design is required at each exposure process. These behaviors vary according to design combinations, including glass thickness, glass size, layer count, and individual layer materials. Therefore, these factors must be carefully evaluated when handling advanced IC substrates or packages with increased layer counts and thicker layers.

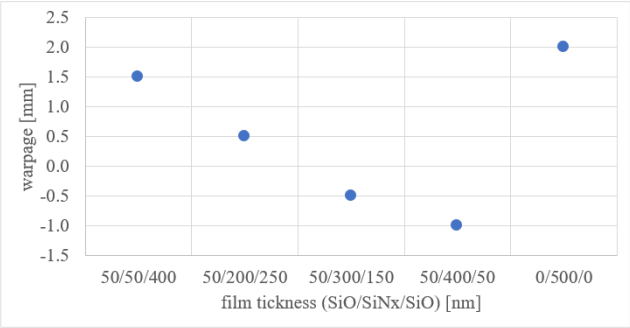


Figure 3. Example of substrate warpage against film structures (display backplane).

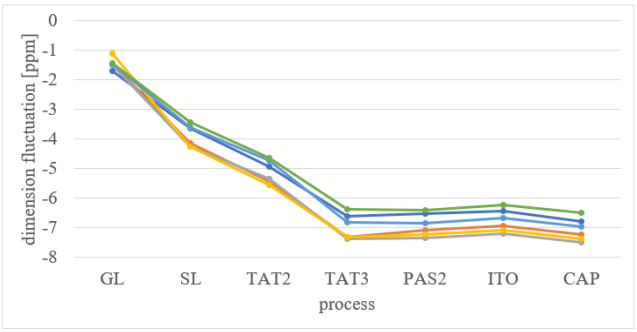


Figure 4. Example of dimensional fluctuation on process by process (display backplane).

3. Sample Trial of Presumable Wiring for Advanced IC Substrate

JDI operates a development line alongside the Gen. 4.5 MP line, where a 6-inch glass wafer (150 mm diameter, circular) is used with Cu sputtering, Cu plating, i-Line MPA (Mirror Projection Mask Aligner) and CO_2 laser drilling.

First, we fabricated samples using a dry process that comprise two patterning layers with Al sputtering and dry etching. The samples also feature acrylic resin around the wiring, resembling our conventional display backplane process. Figure 5 shows an example of 2 µm thick Al wiring on a glass substrate.

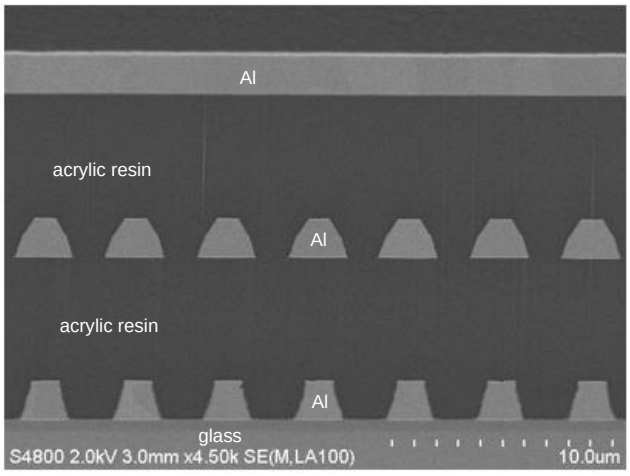


Figure 5. Two layers of L/S = 2/2 µm Al wiring produced by sputtering and dry etching process.

As a second step, we applied the SAP (semi additive process) patterning with Cu plating on a 6-inch glass wafer. We employed a Ti/Cu layer as the seed metal, electroplated Cu for wiring and filled vias on the glass substrate. Figure 6 shows the L/S = 2/2 µm wiring produced by SAP patterning and a filled via with Cu plating. The results demonstrate the successful realization of L/S = 2/2 µm patterns and Cu-filled vias through PSPI (photo sensitive polyimide).

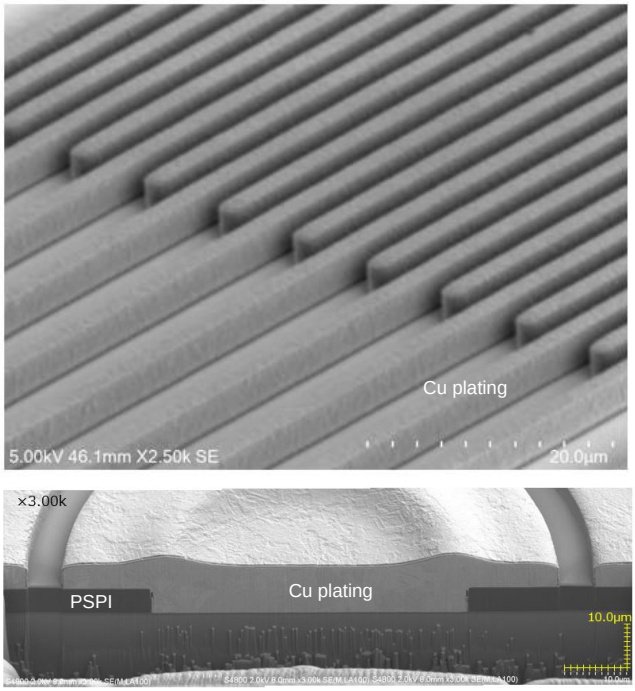


Figure 6. L/S = 2/2 μm Cu wiring with SAP patterning and a filled via with Cu plating.

In addition, we fabricated small diameter vias and filled them with Cu plating. Figure 7 shows approximately 3 μm vias through a PSPI layer. This result demonstrates that 3 μm vias were filled with Cu plating, yielding a flat surface.

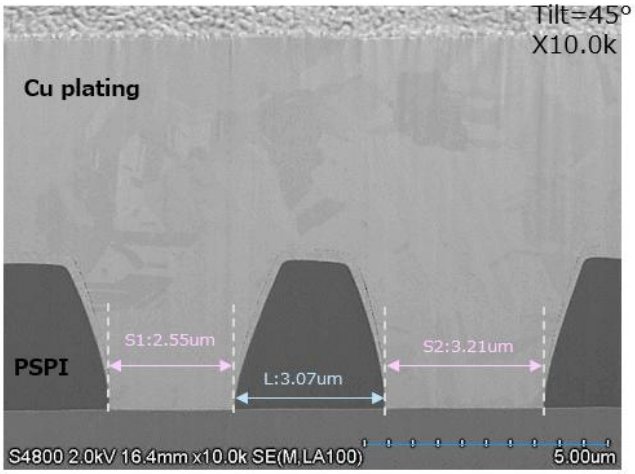
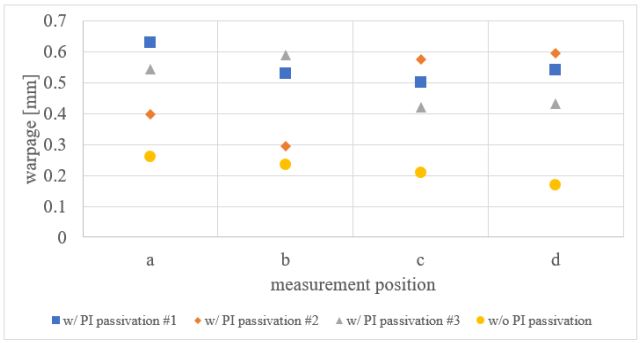


Figure 7. Approximately 3 μm vias through PSPI layer filled with Cu plating.

We evaluated substrate warpage after the patterning process. The substrate comprised 500 μm thick glass, a 5.5 μm thick base PI, 4 μm thick Cu wiring and an 8 μm thick PI protection layer. Figure 8 presents the warpage evaluation results which indicate that even with a single metal layer structure, significant warpage was observed and primarily influenced by the PI resin.

Figure 9 shows the measurements of the dimension from the wafer center to the wafer edge. The variation in these measurement result, affected by the warpage, can be deduced from the warpage evaluation results. This outcome suggests that additional factors may contribute to dimensional fluctuation. As anticipated, we confirmed that dimensions fluctuated significantly owing to film stress and thermal history during processes as observed in the display manufacturing process.

Although these results depend on the substrate design, they underscore the importance of design and material choices for achieving a robust process.



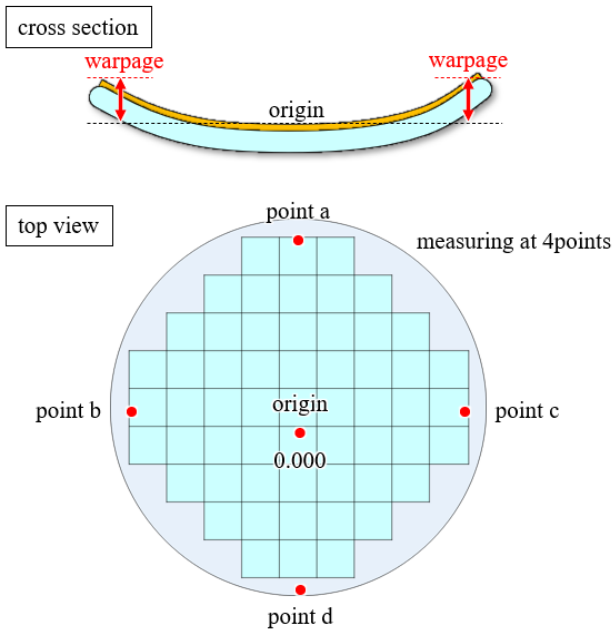


Figure 8. Warpage measurement result of the glass substrate after the patterning process (500 μm thick glass, 5.5 μm thick base PI, 4 μm thick Cu wiring and 8 μm thick PI protection layer).

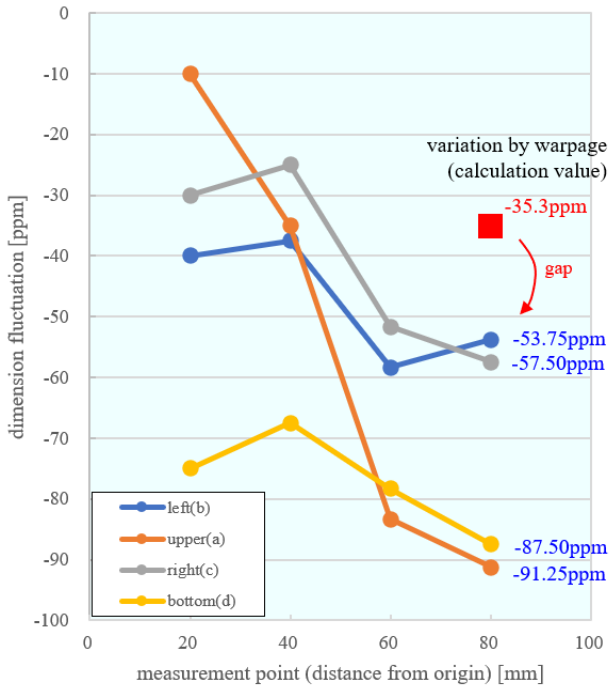


Figure 9. Results of dimension fluctuation measurments after SAP patterning.

4. Future Perspective

We verified the most fundamental process, which includes SAP patterning with electroplated Cu, vias through PSPI layer and via filling with electroplated Cu, on 6-inch glass wafer in our development line.

We plan to extend the process to patterning with vias through additional layers on 730 x 920 mm glass substrate to meet market expectations. Extending the substrate size presents significant challenges in terms of warpage, dimension fluctuation and substrate handling.

Furthermore, the exploration of finer wiring designs suggests that SiO and SiNx film-forming and dry etching technologies hold great potential for achieving highly reliable and flexible wiring structures.

5. Conclusion

JDI has already owned the main equipment to evaluate the processes involved in the advanced IC substrate technology for MP on a 730 x 920 mm (Gen. 4.5) glass substrate, except for the Cu plating process at this moment.

This paper presented our experience in fabricating fine multi-layer wiring based on the display backplane manufacturing. The samples featured L/S = 2/2 µm Al wiring and 1.5 µm diameter via holes. Understanding the issues of warpage and dimension fluctuation was crucial in this process.

Our development line, based on a 6-inch wafer, incorporates key processes for advanced IC substrate development, including Cu-sputtering, Cu plating, i-Line exposure and CO_2 laser drilling. Within this line, we successfully demonstrated a basic sample build employing SAP patterning with 2/2 µm wiring and Cu filled vias. This evaluation underscored the importance of design and material selection in common with the display backplane manufacturing when assessing substrate warpage and dimension fluctuation.

As the next step, we aim to evaluate patterning and via formation on 730 x 920 mm glass substrate. In further explorations, SiO or SiN_x film-forming and dry etching processes may offer viable solutions.

We believe our work will contribute to the realization of the next generation advanced IC packages, leveraging fine fabrication technology of display manufacturing.

6. References

1. Lau JH, “Recent Advances and Trends in Advanced Packaging,” IEEE Transactions on Components, Packaging and Manufacturing Technology, 2022, pp. 228-252.
2. Lau J, Tzeng P, Zhan C, Lee C, Dai M, Chen J, et al, “Large Size Silicon Interposer and 3D IC Integration for System-in-Packaging (SiP),” IMAPS 45th, San Diego, California, USA, 2012, pp.1209-1214.
3. Li J, Tsai F, Li J, Pan G, Chan M, Zheng L, et al, “Large Size Multilayered Fan-Out RDL Packaging for Heterogeneous Integration,” IEEE 23rd Electronics Packaging Technology Conference, 2021.
4. Kuramochi S, Kudo H, Akazawa M, Mawatari H, Tanaka M, Fukuoka Y, “Glass Interposer for Advanced Packaging Solution,” IEEE 6th Electronic System-Integration Technology Conference, 2016.
5. Pan G, Kao N, Lai D, Wang Y, “Warpage Assessment of Chip Module in Chip Last FO-MCM Platform for Non-Wetting Risk Evaluation,” 15th International Microsystems, Packaging, Assembly and Circuits Technology Conference, 2020.
6. Shimizu N, Kaneda W, Arisaka H, Koizumi N, Sunohara S, Rokugawa A, Koyama T, “Development of Organic Multi Chip Package for High Performance Application,” IMAPS 46th, Orland, Florida, US, 2013, pp. 414-419.