Low-Thermal-Stress TGV Leadless Wafer-Level-Package for MEMS High-Temperature Pressure Sensors

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Abstract

Due to high insulation, low cost and low thermal stress of glass wafer, glass is considered as a promising material for advanced package in MEMS sensor. In this paper, a low-thermal-stress Silicon on insulator high temperature pressure sensor was developed by using TGV interconnect technology and glass-based wafer-level packaging technology.

Author Keywords

TGV; Leadless Package; Wafer-Level-Package; SOI high-temperature pressure sensor.

1. Introduction

MEMS pressure sensors[1,2] are designed for pressure measurement, extensively utilized in aerospace, automotive electronics, industrial control, and other sectors. Silicon-based MEMS pressure sensors have increasingly taken a large share of the pressure sensor market due to their high performance and low cost advantages. With the advancement of next-generation aircraft and vehicles towards intelligence and energy efficiency, pressure sensors in aircraft hydraulic systems and automotive new energy thermal management systems are required to achieve an overall accuracy of ±0.3% FS or better, a temperature[3,4] range of -55°C to 150°C, as well as a compact size and high integration per unit area.

Over the past few decades, MEMS technology has enabled the miniaturization, cost reduction, and performance enhancement of various signal sensing chip components.

However, the miniaturization of sensor packaging structures has proven challenging. After integrating the sensing chip with the packaging structure, the overall size often increases by a factor of two to several times. This severely restricts the miniaturization development process of MEMS sensors. MEMS pressure sensors face increasing pressure for miniaturization and high performance, posing significant challenges to their packaging processes. The traditional mainstream packaging solutions include three categories: ceramic capacitive (represented by Sensata), MEMS lead-filled piezoresistive (represented by Kyowa), and MEMS leadless piezoresistive (represented by Kulite[4,5]). Among them, MEMS leadless packaged piezoresistive pressure sensors offer wide temperature ranges, high design flexibility, and high reliability. However, the existing Kulite leadless packaging is limited to single-device packaging formats, making it difficult to further reduce sensor size and post-processing costs, thereby failing to meet the needs of more intelligent application scenarios.

The development of wafer-level TGV leadless advanced packaging technology[6] has become a key solution to the miniaturization and reliability challenges faced by MEMS sensors. It represents a trend in the development of applications such as new energy vehicles. The traditional packaging method for pressure sensors primarily relies on gold wire bonding, which has poor environmental adaptability and prevents the chip from directly contacting the liquid pressure medium. This paper employs Flip-chip technology for the pressure chip to address the above issues. This technology connects the chip directly to the substrate.

Therefore, this invention proposes the use of TGV deep via interconnect technology, wafer-level leadless packaging[6], and SOI high-temperature resistant design schemes to achieve a miniaturized design of low-stress, wide-temperature-range, and highly reliable immersed MEMS pressure sensors. This greatly enhances the systematic design capabilities of high-performance pressure sensors and further reduces process costs.

2. Piezoresistive Sensitivity Mechanism

Piezoresistive pressure sensors typically utilize a full-bridge circuit configuration of a Wheatstone bridge. The four bridge arm resistors change in resistance value when subjected to external pressure, resulting in a change in output voltage. The actual external pressure value can be obtained through the linear relationship between voltage and pressure. The equivalent circuit is shown in Figure 1.

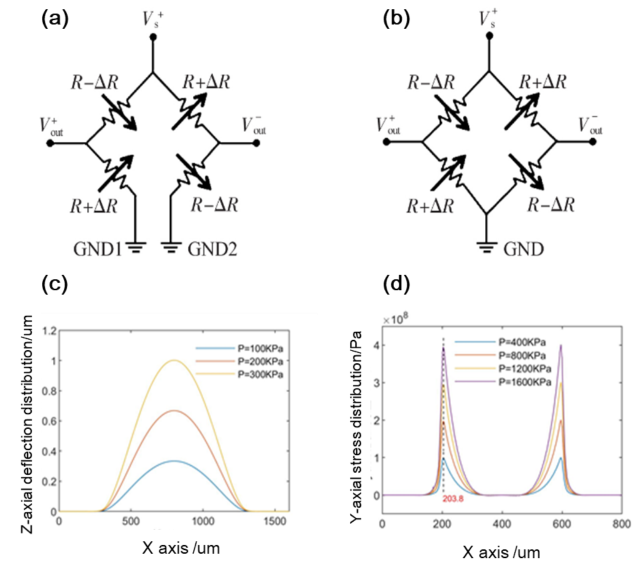

Figure 1. Wheatstone bridge equivalent circuit diagram. (a) open-loop structure, (b) closed-loop structure, (c) Typical piezoresister pressure sensor deflection and (d) stress distribution of sensitive film under different pressures.

Wheatstone bridge voltage output formula is shown in (1) :

$$V_{out} = \frac{\Delta R}{R} V_s^+ \qquad (1)$$

Where V_{out} is the bridge output voltage signal value, mV; R is the bridge resistance value, Ω; ΔR is the change in the resistance value of the bridge caused by the measured pressure, Ω; V_s^+ is the bridge excitation voltage, mV.

$$\frac{\Delta R}{R} = \pi_l \sigma_l + \pi_t \sigma_t \qquad (2)$$

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Where π_l, π_t are the longitudinal and transverse piezoresistive coefficients, Pa^-1, respectively; σ_l, σ_t are the longitudinal and transverse stresses on the sensitive resistor, Pa, respectively.

$$\pi_l = \frac{1}{2}(\pi_{11} + \pi_{12} + \pi_{44}) \approx \frac{1}{2}\pi_{44} \tag{3}$$

$$\pi_t = \frac{1}{2}(\pi_{11} + \pi_{12} - \pi_{44}) \approx -\frac{1}{2}\pi_{44} \tag{4}$$

In the formula, $\pi_{11}, \pi_{12}, \pi_{44}$ are the longitudinal, transverse and shear piezoresistivity coefficients of monocrystalline silicon spindle system, Pa.
Equation (5) can be obtained by bringing (2-4) into equation (1), which is the voltage output formula of the MEMS piezoresistive pressure sensor under a certain power supply excitation, comprehensively reflecting the strong correlation between its output response and the stress of the structural film and the piezoresistive coefficient of the material.

$$V_{out} = \frac{1}{2}\pi_{44}(\sigma_l - \sigma_t)V_s^+ \tag{5}$$

3. Traditional Design

Based on silicon-on-insulator (SOI) substrates, a Wheatstone bridge structure is formed on the front side, while a pressure-sensitive membrane is created on the back side. The vacuum cavity is formed by anodic bonding of the front silicon with glass. The bonding process between the silicon substrate and SiO2 introduces minimal additional stress, offering advantages such as self-isolation, resistance to electromagnetic radiation, good stability, and high-temperature endurance. Kulite[4,5] utilizes a device-level single-chip packaging method, where glass paste filling and valve needle insertion are employed to extract signals, resulting in the fabrication of highly reliable pressure sensors. However, the introduction of device-level packaging process steps increases the cost of pressure sensors and leads to larger dimensions.

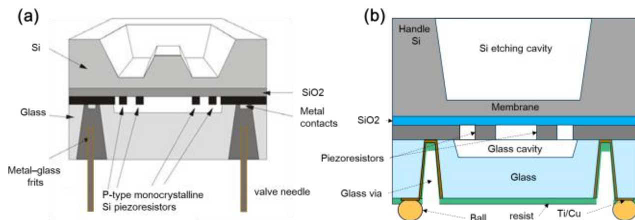

Figure 2. Leadless high temperature pressure sensor package structure. (a) Kulite device level package structure [2], (b) Structure in this paper.

4. Optimal Design

Due to issues such as large device size and high processing costs in device-level packaging design, this paper proposes an integrated glass cavity design for the first time. It utilizes Laser Induced Deep Etching (LIDE) to achieve the fabrication of high aspect ratio interconnecting through-via and vacuum-sealed cavity structures, significantly reducing the size of a single chip. Additionally, 3D deep via electroplating technology is introduced as a replacement for the "metal-glass frits + valve needle" approach, enabling high automation in wafer-level interconnection processing. This not only reduces size and costs but also incorporates a conformal metal structure design to ensure minimal performance loss due to low thermal stress between materials.

The packaging structure design mainly includes stress optimization of the anodic bonding silicon-glass structure and the metal-glass interconnection structure. As shown in Figure 3(a), finite element simulation software is used to analyze the deflection-temperature characteristics of a 1/4 silicon-glass bonded wafer, ultimately determining that a silicon-to-glass thickness ratio of approximately 1:2 results in minimal warping of the wafer. Under solid mechanics and thermal coupling simulation analysis of the single chip, it is confirmed that the miniaturized chip structure design achieves minimal interfacial thermal stress within the temperature range of -55 to 150°C, ensuring optimal process compatibility.

The glass through-via interconnects utilize metals Ti/Cu, with the CTE (Coefficient of Thermal Expansion) of Cu and Glass specified. To ensure minimal thermal stress between materials at different temperatures, a conformal filling structure design is employed. The simulation results are shown in Figure 3, where (c) illustrates the thermal stress between metals and glass under a fully filled structure design, and (d) shows the thermal stress under a conformal filling structure design at 150°C and 0 MPa conditions. Under the same temperature and pressure conditions, the latter exhibits lower thermal stress by several MPa compared to the former. This design theoretically meets the requirements for low-stress packaging, ensuring that the output signal of the MEMS pressure sensor is not affected by thermal strain from interconnecting metals, thus enhancing the reliability of the device signal.

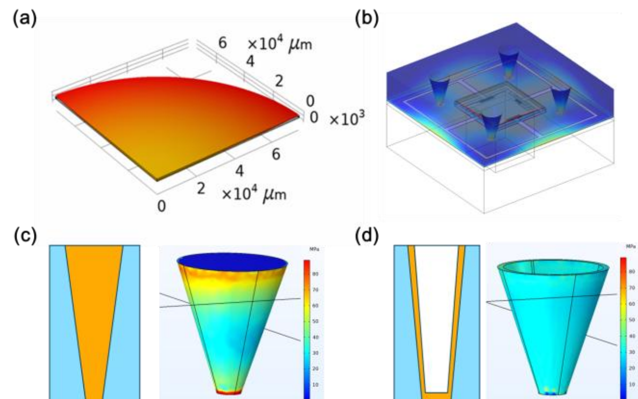

Figure 3. Finite element simulation analysis of the packaging structure. (a) Deflection variation of a 1/4 silicon-glass wafer at different temperatures, (b) Thermal stress distribution cloud map at the bonding interface under 5 MPa pressure and 150°C temperature, (c) Thermal stress distribution cloud map at the interface of glass/Cu with full filled structure, and (d) conformal filling structure.

At the same time, considering the actual processing capabilities, practical verification and recipe control are conducted for both LIDE and PVD electroplating process capabilities.

First, regarding TGV processing capabilities, as shown in the Figure 4, the actual processing images demonstrate the ability for high aspect ratio laser modification and etching processing, achieving a deep-to-width ratio of 1:1 to 10:1 for 6/8 inch glass wafers, which meets the design requirements of this packaging structure.

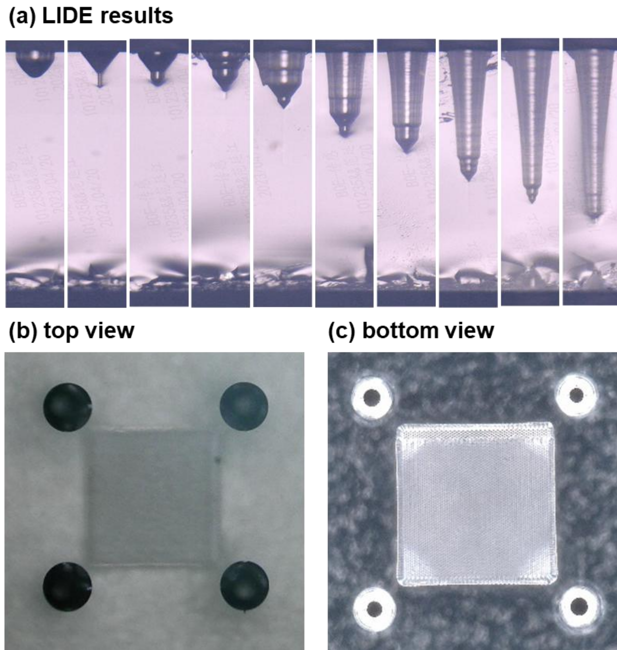

Figure 4. TGV glass Laser Induced Deep Etching (LIDE) process capabilities. (a) LIDE results with different aspect ratios(1:1~10:1), (b) top view of the glass wafer packaging deep via and vacuum cavity structure, and (c) bottom view.

Secondly, the challenges of electroplating deposition[7] in small-diameter, high aspect ratio via lie in the unique distributions of electric potential, flow field, and concentration within the via, which cannot be inferred from empirical knowledge applicable to macroscopic bodies or larger via (shown in Figure 5). To address the issues of increased non-uniformity of the electric field in high aspect ratio via and the confinement effects influencing the flow field and concentration distribution, this paper adjusts the process recipes based on different aspect ratio structures, dielectric environments, and electroplating parameters to derive matching electroplating process conditions. Ultimately, key properties such as metal thickness, thermal expansion characteristics, and conductivity are controllable and adjustable, achieving a conformal filling metal structure that meets design requirements, as shown in Figure 5.

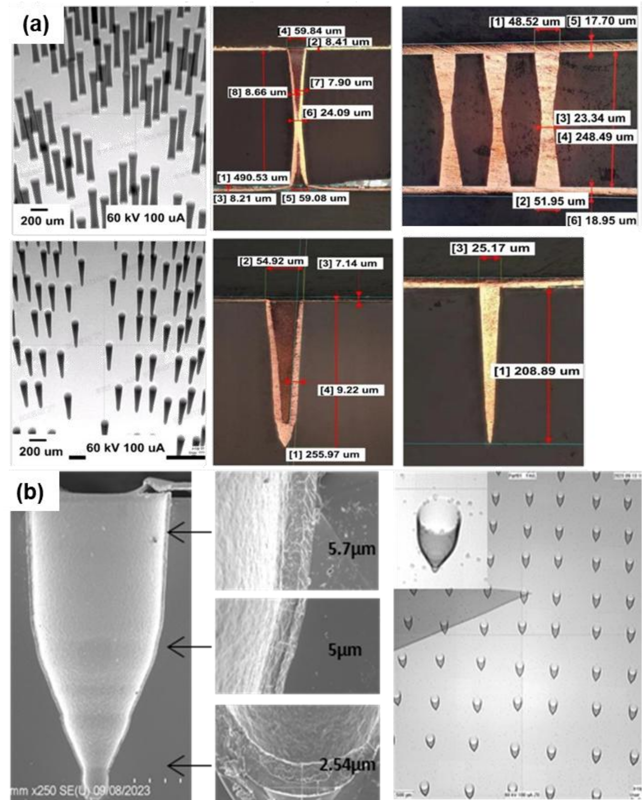

Figure 5. 3D deep via electroplating working fundamentals. (a) Electroplating results in deep via with aspect ratios of 5:1 and 10:1. (b) SEM image of conformal deposition of metal on a glass blind via using PVD and electroplating processes.

5. Results

The designed wafer-level packaged SOI high-temperature pressure sensor underwent cyclic testing with a pressure range of 0 to 5 MPa in a testing fixture, and was subjected to temperature cycling tests in an environmental chamber at temperatures ranging from -55 to 150°C. The final results showed that under a 5V condition at room temperature, the full-scale output signal reached over 100 mV, with a zero offset of less than 10 mV and non-linearity of less than 0.3% FS(as shown in Figure 6(a-b)). Within the temperature range of -55 to +150°C, the zero point temperature coefficient was less than ±0.02% FS/°C, and the sensitivity temperature coefficient was less than -0.22% FS/°C(as shown in Figure 6(c-d)).

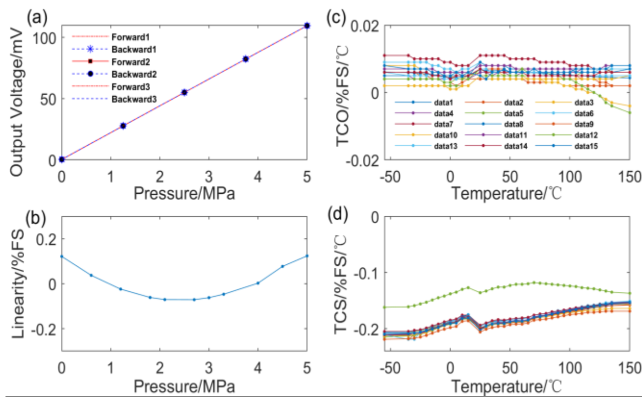

Figure 6. Results of the experimental test.
(a-b) Sensitivity and linearity of the SOI high-temperature pressure sensor, (c-d) TCO and TCS within the temperature range of -55 to +150°C.

6. Conclusion

The low-thermal-stress high-temperature pressure sensor designed in this paper utilizes the SOI intermediate silicon dioxide dielectric to achieve isolation between the pressure-sensitive resistive elements and the substrate, solving the leakage failure issues associated with the traditional PN junction isolation method under high-temperatures conditions above 125℃. Additionally, a TGV wafer-level package is introduced to resolve the problems of traditional wire-bonded packages, such as large size and reliability concerns, as well as issues related to low automation levels and high costs in device-level leadless packaging processes. The pressure chip crafted in this paper has successfully reached initial goals of miniaturization, cost-effectiveness, and high-temperature durability. Moving forward, the focus will be on further improving critical performance indicators and lowering production costs for mass manufacturing.

7. References

1. Kirankumar Balavalad, Sheeparamatti BG. Study & Analysis of junction leakage current in Si & SOI based micro piezoresistive pressure sensor. RTESIT. 2019 Jul 2.
2. Tulaev AT, Kozlov AS, Belyaev JV, Loboda VV, Bellavin MA, Korotkov AS. MEMS Pressure Sensors Design, Simulation, Manufacturing, Interface Circuits: A Review. IEEE Sensors Journal. 2024 Mar 15;24(6): 7395–405.
3. Suski J, Mosser V, Goss J. Polysilicon SOI pressure sensor. Sensors and Actuators. 1989 May;17(3-4):405–14.
4. Kurtz AD, Ned AA, Epstein AH. Ultra High Temperature, Miniature, SOI Sensors for Extreme Environments. 2009.
5. Kurtz A, Ned A, Epstein A. Kulite Semiconductor Products, Inc. Presented at the IMAPS International HiTEC. 2004. Available from: https://kulite.com/assets/media/2018/01/UltraHighTemp.pdf
6. Han X, Huang M, Wu Z, Gao Y, Xia Y, Yang P, et al. Advances in high-performance MEMS pressure sensors: design, fabrication, and packaging. Microsystems & Nanoengineering. 2023 Dec 19;9(1):1–34. 1.
7. Shi S, Wang X, Xu C, Yuan J, Fang J, Jiang S, et al. Modeling and simulation of Cu TSV electroplating for wafer-level MEMS vacuum packaging. 2013 Aug 1.