Research on Low-Power OLED Display Technology Based on SDP Scheme

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Abstract
This paper mentions a new driving circuit scheme, SDP (Separate Driving Pixel), which can reduce the voltage margin of power supply by independent control of the R/G/B pixel unit and effectively reduce power consumption of the OLED panel.

Author Keywords
OLED; Low power; Driving pixel; Voltage margin; VDD drop.

1. Introduction
We live on the beautiful and magical Earth. Energy conservation, environmental protection and green development are the eternal themes of all industries. With the development of OLED display technology, the demand for low power OLED display has never changed. Therefore, a design scheme of Separate Driving Pixel (SDP) that can reduce power consumption is proposed.

In conventional OLED display technologies, the displayed image is composed of R/G/B pixels. A set of VDD and VSS signals will be designed as the power supply for the pixel unit. When all pixels are in operation, the driving current required by the R/G/B pixels will flow from the VDD to the VSS signal. Due to the distinct luminescence characteristics of R/G/B OLED devices, the luminance ratios of R/G/B pixels in white image also differ. When displaying white image, there will also be differences in current and voltage distributions in the circuits of R/G/B pixels. Figure 1. shows the normal pixel schematic.

Referring to the capabilities of existing OLED devices, the B pixel requires the highest voltage, followed by the R pixel, and the G pixel requires the lowest voltage. When the VDD and VSS of the R/G/B pixels share the same voltage, satisfying the voltage required by the B pixel will cause the applied voltages on the R/G pixels to be higher than the voltage required for their respective luminance. We refer to this as the power supply voltage margin. An excessive power supply margin for the R/G pixels will lead to an increase in the overall power consumption of the panel. As shown in Figure 2.

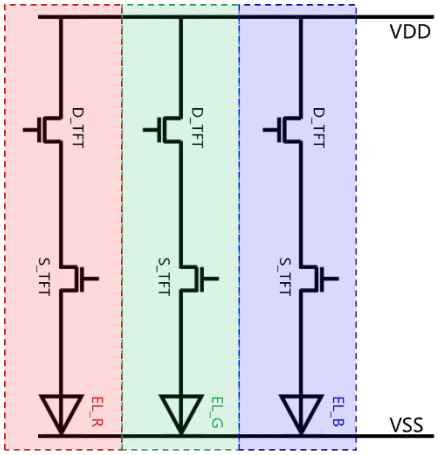

Figure 1. Normal pixel schematic

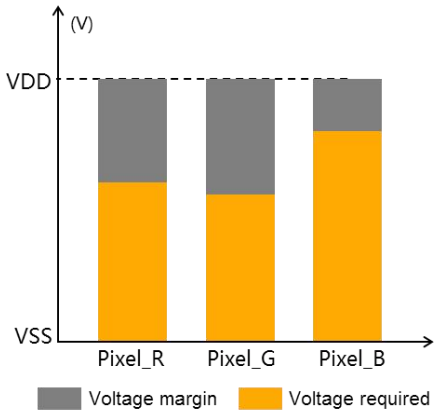

Figure 2. Power supply voltage margin of R/G/B pixels

2. Concept and method
2.1 Analysis of the working principle of pixels

In conventional OLED display design scheme, the schematic diagram of the pixel circuit can be simplified to consist of VDD/VSS power supplies, Switch TFT (Thin Film Transistor)/Driving TFT, and OLED device. When VDD and VSS are set to appropriate voltage values and the Switch TFT/Driving TFT are turned on, the pixel will emit light when current passes through the OLED device. Different pixel luminance can be obtained by controlling the gate voltage of the Driving TFT.

Referring to the existing design rules, in the simplified schematic diagram of the pixel circuit, we define the voltage from the Source to the Drain of the Driving TFT as Vd. We define the voltage from the Anode to the Cathode of the OLED device as Vel. We define the current passing through the pixel circuit as Id. In addition, when the circuit is in operation, the voltage allocated to the Switch TFT can generally be neglected.

Due to the different efficiencies of R/G/B OLED devices, when each pixel is in operation, the current required to pass through the pixel circuit also differs. We define the currents passing through the R/G/B pixels as Id_R, Id_G, and Id_B respectively. Under normal circumstances, when displaying the white image, the operating current requirement for R/G/B pixels are as Id_B > Id_R > Id_G.

According to the working principle of pixels and the characteristic curve of the Driving TFT, it is required that the currents of R/G/B pixels operate in the saturation region of the Id/Vd characteristic curve, as shown in Figure 3. At this time, we find that in order to match the currents required for the white image, the voltages from the Source to the Drain of the Driving TFT in R/G/B pixels are in the order of Vd_B > Vd_R > Vd_G.

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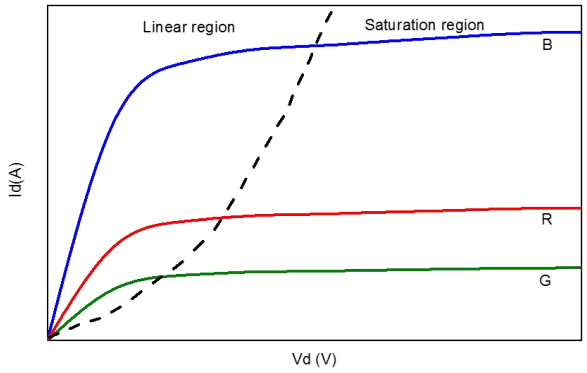

Figure 3. Characteristic curve of Driving TFT

In addition, we found that, when the OLED screen is displaying the white image, in order to match the currents required, the voltages from the Anode to the Cathode of the OLED devices in R/G/B pixels are in the order of Vel_B > Vel_R > Vel_G. As the characteristic curves of R/G/B OLED devices shown in Figure 4.

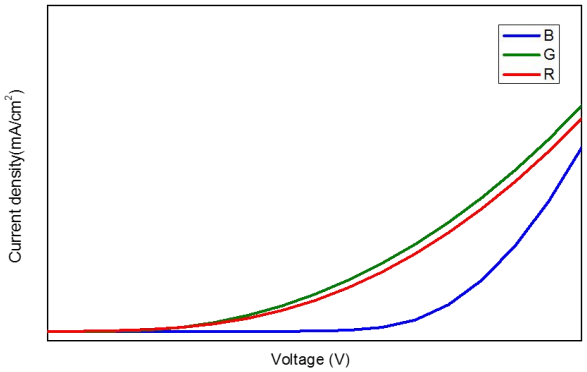

Figure 4. Characteristic curve of OLED device

In the normal pixel design scheme, R, G, and B share a set of VDD and VSS signals, so the voltages between VDD and VSS of R/G/B pixels are the same. According to the above analysis, when displaying the white image, in the driving current path formed from VDD to VSS, the voltages from the Source to the Drain of the Driving TFT are Vd_B > Vd_R > Vd_G, and the voltages from the Anode to the Cathode of the OLED device are Vel_B > Vel_R > Vel_G. It can be found that the B pixel requires the highest operating voltage to achieve the target current. When R, G, and B pixels are at the same voltage between VDD and VSS, there is a certain power supply voltage excess for R and G pixels.

2.2 The design concept of SDP (Separate Driving Pixel)

To achieve the low power OLED display, we can appropriately reduce the power supply excess of R/G pixels based on the actual voltage operating conditions in the panel. During the production process of OLED panel, the VDD signal is connected to the pixels by metal line, while the VSS signal is fabricated through vacuum evaporation to form a continuous metal thin film within the display area, which is the Cathode layer in the OLED device. Currently, the cathode layer is rather difficult to achieve patterning based on existing technologies. We consider dividing the original set of VDD signal into three groups, corresponding to the R/G/B pixels respectively. So that the R/G/B pixels can be driven by different VDD voltages. As shown in Figure 5. When the OLED screen is displaying white image, compared with the B pixel, the R/G pixels require a smaller Id, a lower Vd, and a lower Vel. The VDD voltage of the R/G pixels can be decreased according to their respective power supply , while the VSS voltage remains unchanged. As the voltages of the R/G pixels decrease, the power consumption of the R/G pixels will also decrease. Consequently, we can effectively reduce the overall power consumption of the OLED panel. As shown in Figure 6.

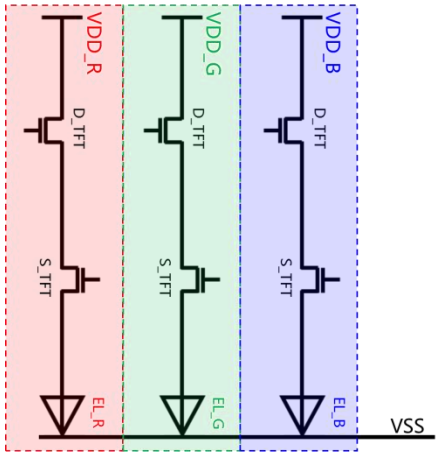

Figure 5. SDP schematic

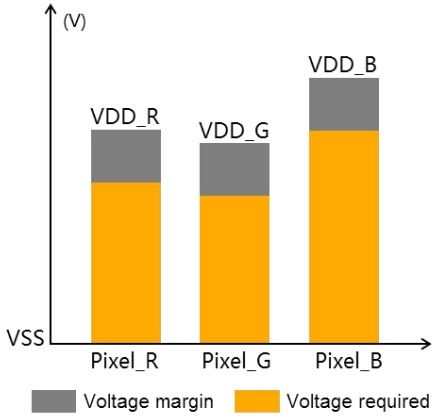

Figure 6. Power supply voltage margin of SDP

2.3 The connection of the VDD signal in the SDP scheme

In the conventional OLED display technology, we often use the LTPS (Low Temperature Polycrystalline Silicon) process to fabricate TFT devices. In combination with the requirements of the driving principle of the OLED pixel compensation circuit, the design of the VDD signal is highly relevant to the luminance uniformity of the OLED panel. To address this issue, the normal pixel design adopts the method of connecting the VDD signal in the metal mesh pattern within the panel active area, which can effectively reduce the voltage drop of VDD signal. In the SDP scheme, since the VDD signals of R/G/B pixels are separated into three independent groups, it is impossible to achieve a mesh-like VDD connection through each pixel. We have designed to independently connect the VDD signal of R/G/B pixels into a mesh structure, and through separately adjusting the density of the metal connections and the width of the metal

lines, we can control the differences in the VDD voltage drop of R/G/B pixels. Figure 7. shows the VDD connection of SDP.

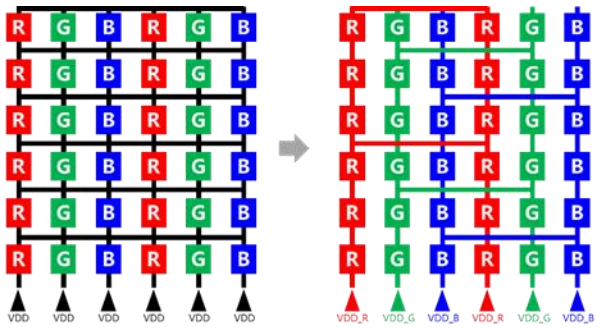

Figure 7. VDD connection of SDP

3. Results and discussion

3.1 Voltage setting of SDP scheme

In the design process of OLED display panel, it is common to evaluate the feasibility and confirm the effects of new design schemes by circuit simulation. We can incorporate the appropriate TFT model data and OLED device model data, along with the actual loading conditions, into the pixel circuit simulation architecture. Once the pixel circuit simulation architecture has been established, we will set the target current required for displaying white image, and thus obtain the respective power supply voltage margins of the R/G/B pixels, which are not the same. Next, by adjusting the VDD signal voltage to make the power supply margins of R and G consistent with that of B, we can obtain the actual VDD voltage of R/G pixels. As shown in Figure 8.

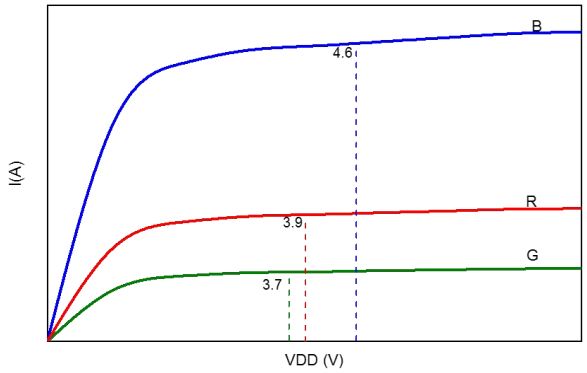

Figure 8.VDD voltage of SDP scheme

Based on the above analysis, we plan to confirm it on the platform of 6.58-inch FHD+ OLED display panel for mobile phone applications. We made two types of sample.

1) Normal sample: The R/G/B pixels share the same VDD signal.
2) SDP sample: Three sets of VDD are designed to drive the R/G/B pixels separately.

According to the actual test results, when the power supply margins of the R/G/B pixels in the SDP sample are designed to be the same, the VDD voltage of R pixel can be reduced by 0.7 V, of G pixel can be reduced by 0.9 V, while the VDD voltage of the B pixel remains unchanged. Table 1. shows the VDD setting of SDP and Normal samples.

	Normal			SDP		
	R	G	B	R	G	B
VDD Voltage (V)	4.6			3.9	3.7	4.6

Table 1. VDD setting of SDP and Normal samples

3.2 Low power consumption of SDP

We evaluated two types of sample of 6.58-inch FHD+ OLED display panels for mobile phone applications. By comparing the SDP sample with the Normal sample, it was found that under the white image, the panel power consumption could be reduced by ~6%; under the red image, the power consumption could be reduced by ~17%; and under the green image, the power consumption could be reduced by ~27%. Subsequently, we carried out optical performance tests and reliability tests on the SDP sample and the Normal sample. There was basically no difference in the OLED display performance between the two types of sample. As shown in Figure 9.

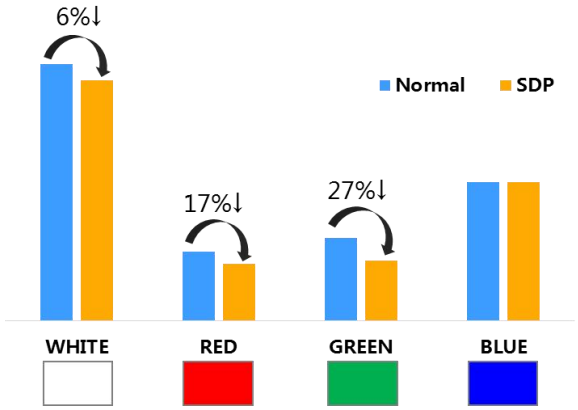

Figure 9. The benefit of panel power consumption between SDP and Normal samples

3.3 Demonstration of SDP scheme.

We have made the demo of the 6.58-inch FHD+ OLED display panel, which includes SDP scheme and Normal scheme. Panel specifications are shown in Table 2. We have integrated a power meter into the prototype, enabling it to display the power consumption data of the OLED panel in real time. As shown in Figure 10, when the same image is displayed at the brightness of 500 nits, it can be observed that the panel power consumption of the SDP demo is approximately 6.4% lower than that of the Normal demo.

Specification information		
Size		6.58 inch
PPI		460
Aspect ratio		20 : 9
Contrast ratio		5000000 : 1
Border	Left & Rignt	0.8 mm
	Top	0.65 mm
	Bottom	0.98 mm (typ.)
Demo luminance		500 nits

Table 2. Panel Specifications

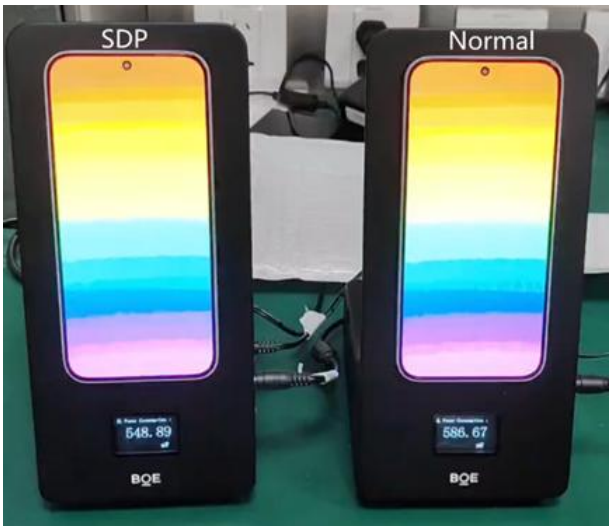

Figure 10. Demonstration of SDP scheme

4. Conclusion

In this paper, we introduced the 6.58-inch FHD+ OLED display demo. Adopting the SDP design scheme, the power consumption of the OLED panel can be effectively reduced by adjusting the voltage setting of VDD. The display performance of the SDP sample was evaluated, and the evaluation results showed no difference from the display performance of the existing mass-produced products. Therefore, this technology can be applied to future OLED display products.

The technology for reducing power consumption in OLED display can enhance the battery life of display devices, prolong the service life of the equipment, and decrease the overall energy consumption, which is of great significance for future environmental protection. This is a long-term and challenging task. We need to continuously promote technological innovation and apply more low-power consumption technologies to OLED display, thereby making contributions to the construction of a beautiful homeland on Earth.

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