Partial Update LCD Based on LTPS Backplane Using a New Gate Driver on Array Combined with Multiplexing Architecture

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Abstract

This paper introduces a new GOA combined with 2-MUX architecture to realize partial update function in a 16-inch LCD panel based on LTPS backplane. The power consumptions of proposed GOA and 2-MUX architecture are respectively improved by up to 29% and 40% between full and 2/5 partial update modes.

Author Keywords

Gate driver on array (GOA), partial update, power consumption, liquid crystal display (LCD), low temperature poly-silicon (LTPS), multiplexing (MUX)

1. Introduction

Recently, integrated gate driver circuits on glass have been widely used in liquid crystal displays (LCDs) due to the superior characteristic of high system reliability, compactness, and low cost by eliminating driver integrated circuits (ICs) [1]-[2]. Moreover, power consumption is an important issue for portable laptops with limited battery capacity. To save power consumption, decreasing the frame rate of a display panel is an intuitive and effective method [3]. However, the display panel must operate at the same frame rate owing to the conventional gate driver on array (GOA) circuit using a row-by-row scanning method [4], as shown in Fig. 1(a). Therefore, Chen *et al*. proposed a new partial scan GOA based on a-Si:H thin film transistors (TFTs) that can realize dynamic local refresh function at any position and with different refresh rates at different areas in an LCD panel [5]. However, a-Si:H TFTs increase the bezel and reduce the aperture ratio of LCD panels owing to low mobility and stability, resulting in poor user experience of portable laptops. Furthermore, to reduce the cost of source ICs, a multiplexing (MUX) circuit is commonly applied to the display panel [6], which is also unsuitable for realization by a-Si:H TFTs. Compared with a-Si:H TFTs that have advantages on large display panels, low temperature poly-silicon (LTPS) TFTs have high mobility and stability that are generally applied to small and medium display panels [7]. Thus, for promoting laptop applications, a new GOA with MUX technology based on LTPS TFT that can save power consumption and cost of source ICs is required to be designed.

This paper proposes a new GOA combined with a 2-MUX architecture based on LTPS TFTs to achieve multi areas at several frame rates in LCD panels for reducing power consumption and the number of source driver ICs, as shown in Fig. 1(b). The proposed GOA separates the enable gate line output module from the signal transmission output module to prevent the response time of signals for transmitting to the previous or next stages from the effect of the gate line loading. Simultaneously, the enable gate line output module can be applied to generate the required scan signal when only specific row lines need to turn on pixels for the partial update function. In addition, the 2-MUX architecture decreases the number of source driver ICs to achieve lower cost of LCD panels. Measurement results show that the proposed GOA with 2-MUX architecture successfully generates the required output waveforms to drive 5 areas of a display panel at several frame rates. The reductions of power consumption are respectively 29% and 40% between full update mode and partial update mode for the proposed GOA and 2-MUX architectures in a 16-inch LCD panel with a resolution of 2560 × 1600 (WQXGA). Therefore, the proposed GOA with the 2-MUX architecture is applicable to use in the portable laptop.

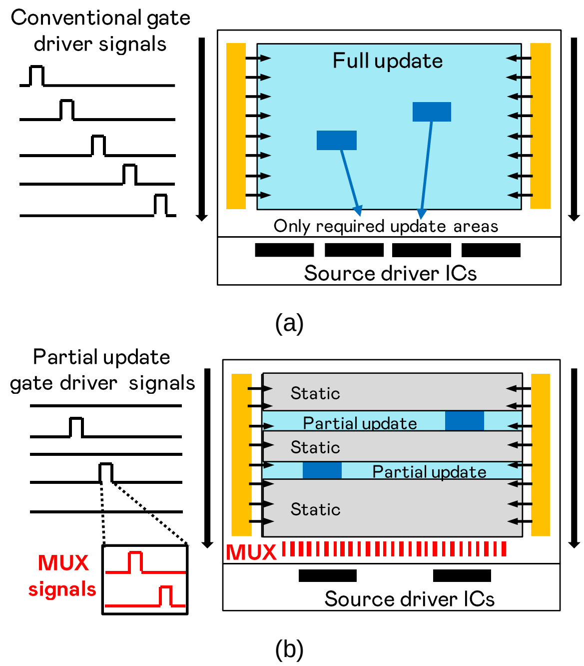

Figure 1. Schematic diagrams of display system for (a) conventional design and (b) this work.

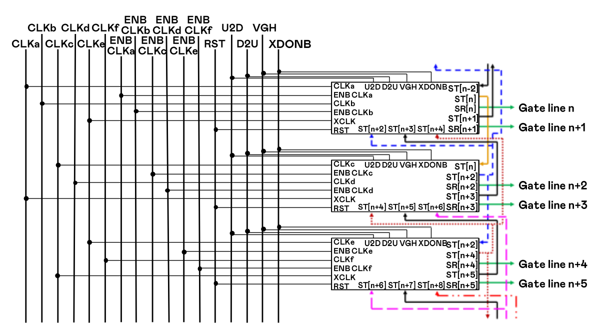

Figure 2. System diagram of proposed GOA.

2. Method

2.1 Design of GOA and 2-MUX architectures for partial update LCD panel:

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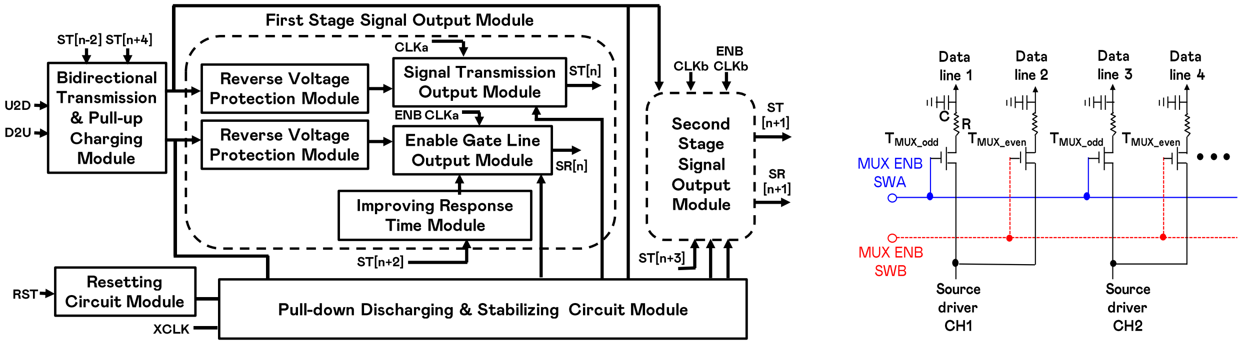
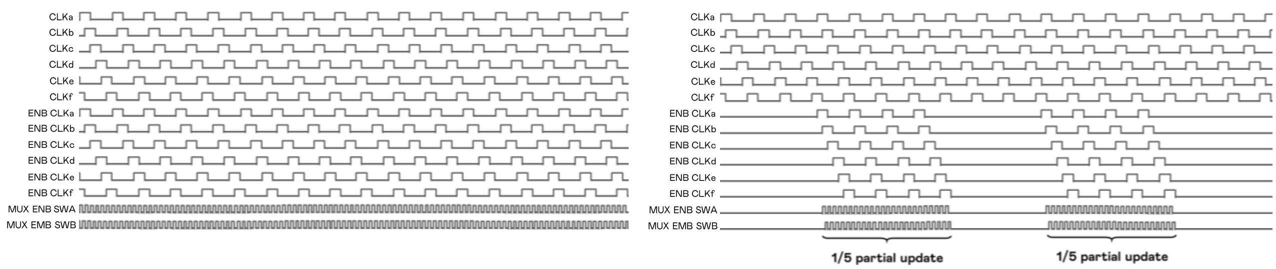


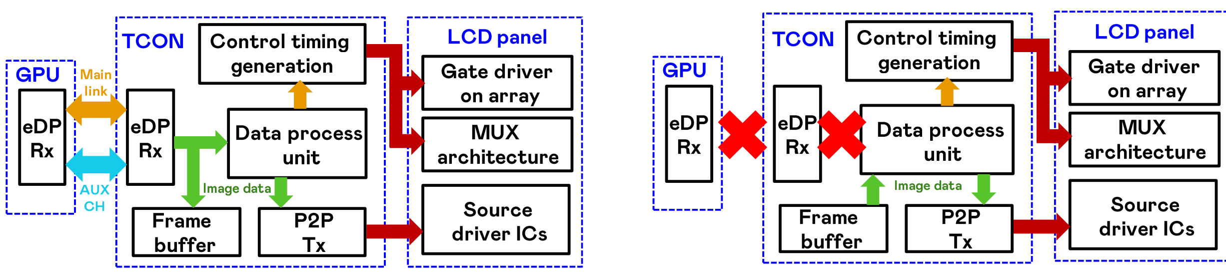
(a) (b)

Figure 3. (a) Module of one proposed GOA unit. (b) Schematics of 2-MUX architecture.



(a) (b)

Figure 4. Timing diagrams of (a) full update mode and (b) 2/5 partial update mode.



(a) (b)

Figure 5. Block diagrams of TCON design in partial update LCD panel for (a) partial update areas (b) static areas.

Fig. 2 presents the system diagram of the proposed GOA, and Fig. 3(a) shows a schematic of one GOA unit with several modules. The bidirectional transmission and pull-up charging module is applied to decide the forward transmission and backward transmission of display panels and receive the previous stage signal to activate this stage module. The resetting circuit module can reset the voltage of the internal nodes of GOA before starting circuit operation, improving the stability of system. After generating output waveforms, the pull-down discharging and stabilizing circuit module can discharge and keep the internal nodes of GOA at a low voltage to ensure the stability of a display system. Moreover, several modules are shared for two stages signal output modules to reduce the required layout areas of one GOA unit, achieving lower bezel of an LCD panel. One stage signal output module consists of reverse voltage protection, signal transmission output, enable gate line output, and improving response time modules. To avoid the effect of the gate line loading that directly affects the response time of the signals for use to input to other stages, the signal transmission output module is only applied to generate the ST signals for transmitting to the previous or next stages. Owing to the separation from the signal transmission output module, the enable gate line output module can determine when the SR signals are generated to achieve a partial update function according to the ENB clock signals. Particularly, the improving response time module can further the falling time of SR signals to meet the requirement of high resolution or high frame rate. Fig. 3 (b) demonstrates a 2-MUX architecture in an LCD panel. When the ENB CLK signals are applied to enable gate line output module, two MUX ENB SW signals alternately turn on T_{MUX_odd} and T_{MUX_even} to make the source driver ICs input the data voltage to the data lines. Therefore, the number of the source driver ICs can be reduced, achieving lower cost from ICs in the LCD panel. Furthermore, the panel in partial update mode can be divided into areas equal to the number of row lines at most. In this work, the panel is divided into 3 areas or 5 areas to simply and quickly evaluate the performance of proposed GOA and 2-MUX architecture. Fig. 4(a) and Fig. 4(b) indicate the timing diagrams of full update mode and two-fifths (2/5) partial update mode. The ENB CLK and MUX ENB SW signals can both disable clock signals to the static

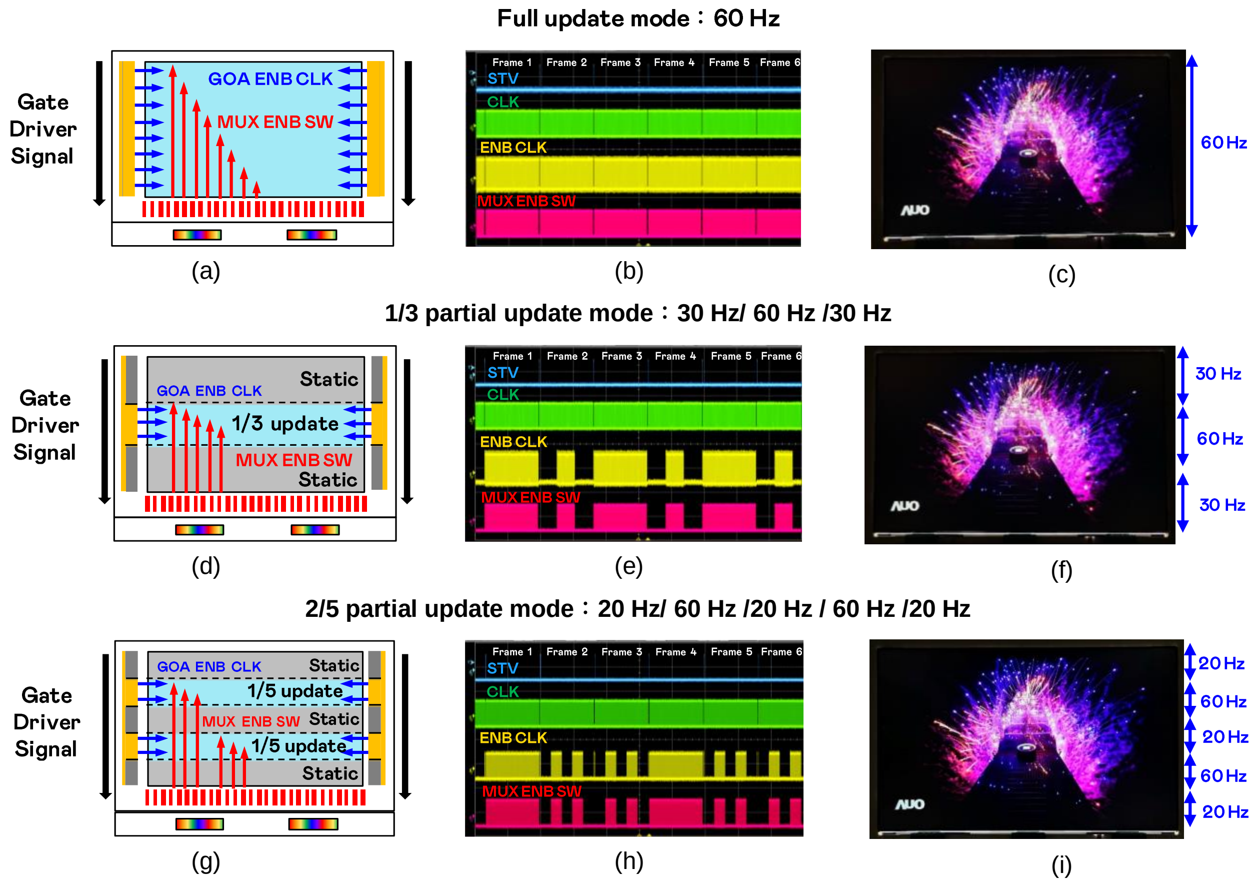


Figure 6. Schematic diagrams, measured clock signals, and light-on color images between three types of update modes.

Table 1. SPECIFICATION OF PROPOSED LCD PANEL.

Proposed partial update panel	
Process	LTPS
Panel Size (inch)	16
Resolution	2560 ×RGB ×1600
Frame rate (Hz)	20 - 120
MUX	2-MUX

areas and provide clock signals to the partial update areas according to the requirement of partial update mode. Thus, the power consumption can also be decreased as clock signals are disabled.

2.2 Design of TCON for partial update LCD panel:

To realize the partial update function, an LCD panel is divided into partial update and static areas. Fig. 5(a) and Fig. 5(b) respectively illustrate the operation of block diagrams of a new timing controller (TCON) design for partial update and static areas. In the partial update areas, image data in the frame buffer is updated, and then the control timing generation and P2P Tx are simultaneously outputted the required signals from TCON to GOA, MUX, and source driver ICs. Compared with the partial update areas, the main difference in the static areas is that the image data is provided from the frame buffer. Therefore, the proposed GOA and 2-MUX architecture can successfully generate the required output waveforms through the TCON design, achieving a partial update function in an LCD panel.

3. Results and Discussions

3.1 Partial update function:

To investigate the function and integration of the proposed GOA and 2-MUX architecture, a 16-inch LCD panel based on LTPS technology is fabricated. Table 1 depicts the design specification of the LCD panel. The resolution of the LCD panel is 2560 × 1600. The LCD panel can be divided into several areas according to the number of row lines. Each area can be matched at several frame rates from 20 Hz to 120 Hz to realize the partial update function. The 2-MUX architecture can also reduce the quantity of the required source driver ICs used. Fig. 6 shows schematic diagrams, measured clock signals, and light-on color images between the full update, one-third (1/3) partial update, and two-fifths (2/5) partial update modes. In the full update mode, CLK, ENB CLK, and MUX ENB SW signals can continuously be outputted from frame 1 to frame 6 after the STV signal starts. The 1/3 partial update mode can stop outputting two-thirds part of ENB CLK and MUX ENB SW in frame 2, frame 4, and frame 6 for static areas with a frame rate of 30 Hz. Moreover, the 2/5 partial update mode can also stop outputting three-fifths part of ENB CLK and MUX ENB SW in frame 2, frame 3, frame 5, and frame 6 for static areas with a frame rate of 20 Hz. The light-on color images in three types of update modes are almost identical, proving the partial update function and high integration of the proposed GOA and 2-MUX architecture.

Table 2. POWER CONSUMPTION OF GOA AND MUX.

Measured power consumption for L0 (mW)					
Full update mode					
Case 1			Case 2		
60 Hz	GOA	MUX	120 Hz	GOA	MUX
	55	182		108	389
1/3 Partial update mode					
Case 1			Case 2		
30/60/30 Hz	GOA	MUX	60/120/60 Hz	GOA	MUX
	41 (-25%)	130 (-29%)		80 (-26%)	257 (-34%)
2/5 Partial update mode					
Case 1			Case 2		
20/60/20/ 60/20 Hz	GOA	MUX	40/120/40 /120/40 Hz	GOA	MUX
	39 (-29%)	119 (-35%)		77 (-29%)	232 (-40%)

3.2 Power consumption analysis

Table 2 presents the power consumption of the proposed GOA and 2-MUX architecture between three types of update modes with several frame rates in the two cases. The power consumptions of proposed GOA and 2-MUX architecture for L0 in case 1 are respectively 55 mW and 182 mW in the full update mode for a frame rate of 60 Hz, 41 mW, and 130 mW in the 1/3 partial update mode for frame rates of 60 Hz and 30 Hz, and 39 mW and 119 mW in the 2/5 update mode for frame rates of 60 Hz and 20 Hz. As the frame rates become twice in case 2, the power consumptions of proposed GOA and 2-MUX architecture in L0 are respectively 108 mW and 389 mW in the full update mode, 80 mW and 257 mW in the 1/3 partial update mode, and 77 mW and 232 mW in the 2/5 update mode. Generally, the power consumption can be represented by the following relationship:

$$P \propto f \times c \times v^2$$

where f is the driving frequency, c is the capacitance of loading, and v is the driving voltage. The difference between the two cases is that only frame rates become twice, and the capacitance of loading and driving voltage are fixed. Compared with case 1, the power consumption of case 2 is nearly twice in the three types of update modes. Furthermore, the reductions of the power consumption for the proposed GOA and 2-MUX architecture are up to 29% and 40 % in case 2 for 2/5 partial update mode. Thus, the proposed partial update design successfully reduces the power consumption, being suitable for the portable laptop.

4. Conclusion

This paper proposes a new GOA combined with a 2-MUX architecture using LTPS TFTs to reduce power consumption and cost for a partial update LCD panel. The signal transmission output module in the proposed GOA outputs the signals only applied to transmit to the previous or next stages. Therefore, the response time of the signals for input to other stages prevents the effect of gate line loading. At the same time, the enable gate line output module does not need to consider the transmission function and can only generate the SR signals according to the ENB clock signals for the specific row lines, achieving the partial update function. Moreover, the 2-MUX architecture also decreases the number of source driver ICs for low cost. Measurement results prove that the power consumptions of the proposed GOA and 2-MUX architectures are reduced by 29% and 40% between the full update mode and 2/5 partial update mode in a 16-inch LCD panel with a resolution of 2560 × 1600. Based on measurement results, the proposed GOA and 2-MUX architecture are well-suited for the portable laptop.

5. References

[1] Zhang C, Liu L, Chen Y, Li J, and Shi S. P-51:Design of integrated gate drivers with low-temperature poly-silicon thin film transistor. SID Symp Digest.2019;50(1):1425–8. https://doi.org/10.1002/sdtp.13206

[2] Lin CL, Chen FH, Wang MX, Lai PC, Tseng CH. Gate driver based on a-Si:H thin-film transistors with two-step-bootstrapping structure for high-resolution and high-frame-rate displays. IEEE Trans Electron Devices. 2017;64(8) :3494-7. https://doi.org/10.1109/TED.2017.2710180

[3] Nakamura T, Tada M, Kimura H. A 550-PPI LCD using 1.5 µm channel width LTPS TFTs with low frame rate driving. J Soc Inf Disp. 2015;23(12):580-6. https://doi.org/10.1002/jsid.405

[4] Lin CL, Cheng MH, Tu CD, Wu CE, Chen FH. Low-power a-Si:H gate driver circuit with threshold-voltage-shift recovery and synchronously controlled pull-down scheme. IEEE Trans Electron Devices. 2015;62(1):136-42. https://doi.org/10.1109/TED.2014.2372820

[5] Chen D, Yang T, Shao X, Liu D, Miao Y, Ma W, et al. P-8: Realization of dynamic local refresh on LCD with novel partial scan GOA. SID Symp Digest. 2024;55(1): 1392–5. https://doi.org/10.1002/sdtp.17807

[6] Kim HS, Lee WS, Yoon JS, Kim SD, Kim SH, Kim BK. P-39:Low power and fast response driving method for MUX circuit using polarity MUX technology. SID Symp Digest. 2016;47(1):1265-8. https://doi.org/10.1002/sdtp.10880

[7] Ibaraki N. Low temperature poly-Si TFT technology. SID Symp Digest. 2012; 30(1):172-5. https://doi.org/10.1889/1.1833987