Pixel Design Techniques for 1 Hz Refresh Rate LTPS Emissive Displays Leveraging Multimodal Transistor On- and Off-State Current Characteristics

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Abstract
Mixed-mode simulation of simple multimodal transistor (MMT)-based pixel circuits demonstrate the viability of LTPS-only implementations for low refresh rate active-matrix emissive displays down to 1 Hz. The MMT allows >20x longer image retention TFT-based designs, owing to the reduced off-current of the MMT switch, the minimal dependence of MMT drain current on input voltage, and the low transconductance of the MMT.

Author Keywords
Pixel circuit; multimodal transistor; LTPS; variable refresh rate, 1 Hz.

1. Objectives and Background
In recent years, the success and pervasiveness of emissive mobile displays has created the drive for increased energy efficiency while maintaining image quality and user experience. While advances in materials are improving the efficiency of the light emitting devices, transistor- and circuit-level innovations also play an important role (1). Accounting for the nature of the displayed content, pixel circuits are now required to simultaneously be able to provide high refresh (60 – 240 Hz) rate for seamless scrolling and video content consumption (2–5), and low refresh rate (1-10 Hz) for saving power when display information changes less frequently, including always-on display conditions (6,7). This means that the pixel circuit should be capable of rapid programming and compensation and of a long retention time (e.g. 1 s), while providing high-current driving to the emissive device e.g. organic light emitting diode (OLED). For this reason, the low-temperature polysilicon and oxide (LTPO) technology is preferred, due to the low leakage current of the oxide transistors and the high-on current of low temperature polycrystalline silicon (LTPS) transistors (1,6,8). Evidently, this solution is successful (9), but comes at increased processing complexity and therefore cost.

Here, we explore the advantages brought by using multimodal transistors (MMTs) (10) as both driver and switch devices in an LTPS-only implementation of a simple (2T1C-equivalent) pixel which maintains a stable OLED current for refresh rates as low as 1 Hz.

Simulations were calibrated using high-performance LTPS measurements (11–13) and compare the performance of the MMT implementation with that of a conventional TFT circuit.

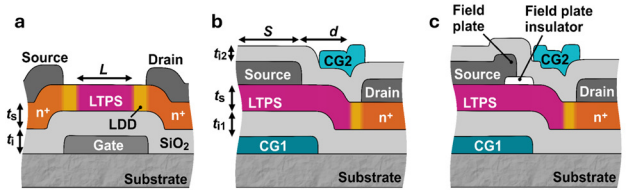

Figure 1. Schematic cross-section of simulated: **a)** TFT; **b)** MMT; **c)** MMT comprising a field relief structure.

2. Methods
Silvaco ALTAS was used to simulate *n*-channel LTPS TFTs and MMTs (Fig. 1) with parameters shown in Table 1. Electrical characteristics are shown in Figures 2 – 4. ATLAS Mixed-Mode was used to run circuit simulations (Figures 5 – 8). *n*-type LTPS has been used due to long-standing experience with contact-controlled devices in this material (12,14,15), as well as verified models for off-state leakage in TFTs (11), even though a *p*-type implementation may be preferred practically. For the present functional demonstration, all transistors have width W = 3 µm. Capacitor values C1 is 0.3 pF for the 1T1C and 2T1C TFT circuits. C1 and C2 add up to C_{TOT} = 0.3 pF, respectively.

3. Results and Discussion
From the outset, it should be mentioned that, as proposed, the device structures considered have both benefits and limitations. Significant optimization may be made in a practical application, considering the specifics of the fabrication process.

MMT Operational Characteristics: A self-aligned staggered electrode LTPS TFT with Ohmic contacts (Fig. 1a) served as the reference structure. MMTs were devised in a dual-gate configuration with control gate 1 (CG1) opposite the source, and control gate (CG2) disposed over the channel, coplanar to the weakly rectifying source (S) and drain (D). The contact-controlled MMT (Fig. 1b) is further refined to include a field relief structure (field plate, FP (15)) as in Fig. 1c.

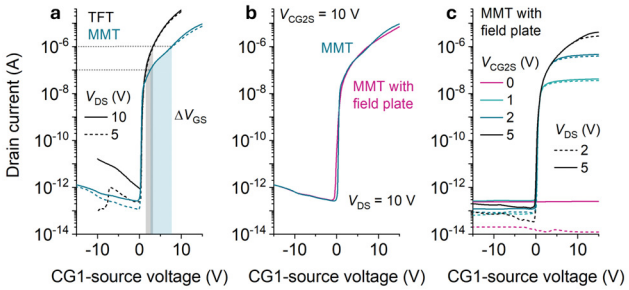

Figure 2. Transfer characteristics for TFT and MMT with respect to source gate (CG1) terminal.

Table 1. Principal design parameters of simulated transistors

Parameter	MMT	TFT
Contact work function, *WF*	4.52 eV	4.17 eV
SiO_2 permittivity, ε_i	3.9	
Gate insulator thickness, t_i, t_{i1}, t_{i2}	60, 100, 60 nm	
LTPS thickness, t_s	30 nm	
LTPS electron, hole mobility	300, 30 $cm^2V^{-1}s^{-1}$	
Source-CG1 overlap, *S*	3 µm (M1), 2 µm (M2, M3)	-
Source-drain separation, *L* or *d*	3 µm	
Field plate extension	0.5 µm	-
Field plate height	20 nm	-

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Fig. 2a compares the transfer characteristics of the TFT and MMT. The on-current is reduced in the MMT due to its contact-controlled nature (10). At the same time, the dynamic range of on-current above threshold (see hashed area in Fig. 2a) is reduced, relative to of the TFT. Concerning the off-current, the MMT has a significant advantage due to the presence of the rectifying source contact. Both characteristics are essential for achieving the operation presented in this study.

Fig. 2b shows the effect of including a FP within the MMT design. While the subthreshold swing and on-current degrade marginally, the off-current is unaffected. Therefore, for operation as a switch, the structure without FP is preferred. Fig. 2c illustrates the operation of the MMT (10), whereby a sufficiently high channel control gate (CG2) potential (e.g. > 2 V) allows the modulation of drain current by source control gate CG1-source voltage independent from the precise value of CG2 voltage, a feature that can be exploited functionally in emissive pixels (16). The same behavior is shown in Fig. 3, which additionally indicates that, if using the MMT as the drive transistors, the structure comprising a FP is preferred.

Fig. 4 shows TFT and MMT output characteristics, confirming the superior performance of the MMT as an energy-efficient voltage controlled current source. Especially in FP configuration, the MMT has low saturation voltage and low drain voltage dependence of saturated drain current.

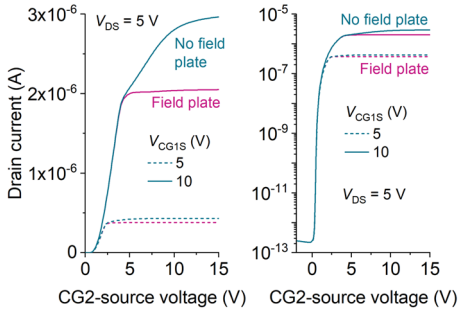

Figure 3. MMT transfer characteristics with respect to the CG2 gate (linear and semilogarithmic representation).

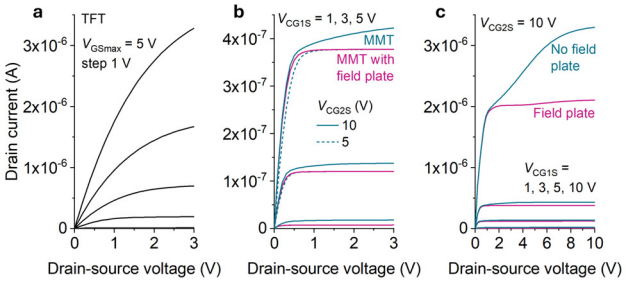

Figure 4. Output characteristics for: **a)** TFT; **b)** and **c)** MMT under different biasing conditions.

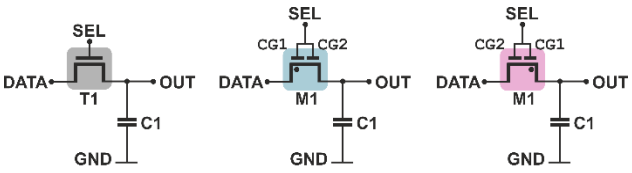

Figure 5. 1T1C circuits for transient time investigation implemented with TFT, MMT connected with the S terminal to the DATA node (MMT_A), and MMT connected with the D terminal to the DATA node.

Pixel Circuit Operation: While the on-state characteristics of contact-controlled transistors have been widely studied owing to the remarkable saturation performance (17–21), the proposed pixel circuit also exploits the superior off-state of these devices.

A concern about using contact-controlled transistors as switches is the relatively low on-current, which may increase the time required for programming in the context of a pixel circuit. To investigate this, a simple 1T1C circuit (Fig. 5) was first simulated, with the active device being a TFT, a MMT without FP with its source connected to the DATA node (MMT_A) configuration, and the same MMT connected with the source to the OUT node (MMT_B).

Transient signals were applied to the DATA and SEL nodes to simulate the operation within an emissive pixel circuit, i.e. charging and discharging capacitor C1 to/from a given voltage. The results in Fig. 6 show that the MMT_A topology only requires ~12% more time than the TFT to charge the capacitor, while MMT_B requires almost 30% longer. The situation is reversed when discharging, with MMT_A being slower. This is a result of the asymmetrical configuration of the MMT. Specifically, due to the biases applied in MMT_A, the Ohmic contact of the MMT is the effective source, and the Schottky contact is the drain, therefore allowing the transistor to pass significantly more current than in the reverse configuration. The performance of MMT_A is close enough to that of the TFT to permit the use of the MMT as a switch for charging C1.

Next, a 2T1C TFT circuit (and its equivalent MMT version) were simulated (Fig. 7) in order to compare data retention time. For reasons of convergence and simulation time, the emissive element D1 was omitted. Signal timing is as expected for a typical 2T1C circuit, with the DATA node being at 0 V during emission.

The MMT switches M2 and M3 are positioned so that their sources are at a lower potential during the emission phase (configuration MMT_A above, which is simultaneously beneficial for rapid programming). The MMT circuit takes advantage of the fact that the MMT drain current is controlled by CG1 potential. Therefore, capacitors C1 and C2 add to the same value as C1 in the TFT circuit, and the split between them can be heavily biased toward C1, as is shown in Fig. 8a.

Fig. 8b compares the evolution of the output current of the drive transistor in the TFT and MMT schematics for three brightness levels corresponding roughly to 75%, 20%, and 5% of white level. The average error rate over 1 s emission time for the TFT circuit is -45.1%, -58.5%, and -61.9%. To maintain 2% error rate, the reference design would only be capable of operating for 31.8 ms, 22.5 ms, and 13.6 ms, respectively, adequate for the 60 Hz standard refresh rate, but nowhere near sufficient for < 10 Hz operation. The MMT design achieves 2.07%, -2.2%, and -11.3% respectively, showing that 1 Hz operation is possible in a LTPS-only implementation, here using *n*-channel transistors. This performance results from the concomitant exploitation of the following MMT attributes:

- The low off-current of the switches, contributing to the long retention time of the voltage on C1 and C2.
- The relative independence of driver drain current on CG2 voltage.
- The reduced dynamic range of above-threshold current compared to that of the TFT, resulting in a smaller change in drain current for a given change of CG1 (gate) voltage.

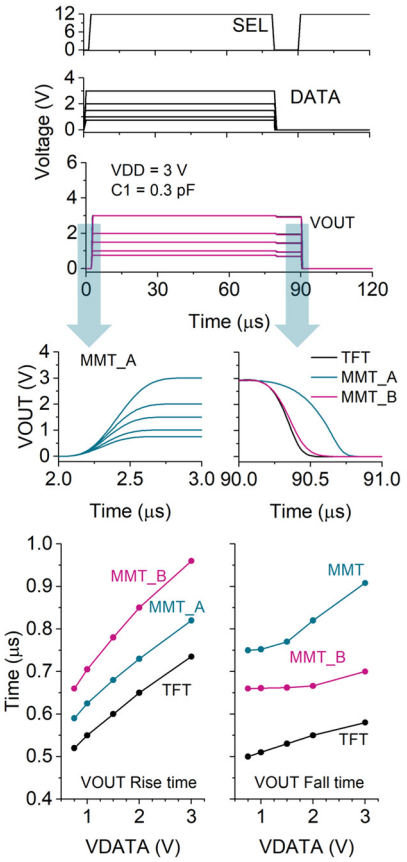

Figure 6. Simulated timing diagram for the circuits in Fig. 5 showing the evolution of charging and discharging times with DATA voltage.

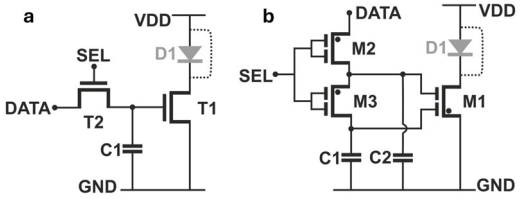

Figure 7. Schematics of the simulated equivalent circuits **a)** 2T1C using TFTs; **b)** 3T2C using MMTs.

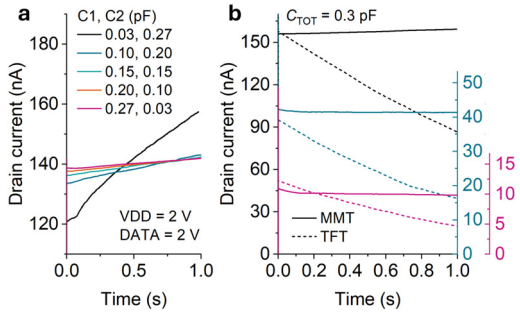

Figure 8. Evolution of current during the 1 s emission time for circuits in Fig. 7 **a)** for the MMT design and different capacitor values totaling 300 fF; **b)** comparing TFT and MMT implementation performance for three brightness levels (~75%, 20%, 5%).

4. Impact and Outlook

This work has shown, through mixed-mode numerical simulations, that the structural and operational features of contact-controlled transistors (specifically MMTs) can be used constructively to achieve long data retention times. Low refresh rates down to 1 Hz should be possible in simple pixel circuits, realized exclusively in LTPS. A limitation of the work conducted so far is that the optimal MMT placement in the circuit allows rapid charging of the capacitor when the switch is conducting and slow discharge when the switch is turned off. However, the same placement would not be able to rapidly discharge the capacitor (see Fig. 6), imposing some restrictions on the driving scheme of more refined pixel circuits. The present study also assumes that, during emission, the voltage stored on the capacitors is higher than the potential at the DATA node. Future work will focus on expanding the range of operating conditions in which the MMT structure is viable as a switch.

While the structure of the MMT is more complex than that of the TFT, it can provide superior functionality in a compact footprint, potentially reducing the requirement for additional signal lines, LDD implants, and the costs associated with these patterning steps. Moreover, achieving the variable refresh rate functionality while using a simplified LTPS process only, i.e. without resorting to additional oxide semiconductor transistors, may provide additional and substantial economic benefits. Naturally, such simplifications would be practical in a production environment only if all circuitry is suitably optimised (e.g. LTPS-only gate-driver on-array – GOA designs). Moreover, the functionality presented in this study would also apply to *p*-channel transistor implementations, which may be preferred for OLED integration reasons. Although the simulations have been judiciously calibrated with existing data, physical implementation is the essential next step required to confirm functionality and performance.

Even though the advantageous on-state traits of the MMT are best applied to current-driven pixel designs, the reduced off-state leakage would remain beneficial to voltage-driven configurations such as LCD pixels.

It is worth noting that using source-gated transistors (SGTs) rather than MMTs would have the same benefits concerning leakage current of the switch, on-current dynamic range, and saturation characteristics of the drive transistor. In this case, the superior versatility afforded by the independent CG1 and CG2 control mechanisms of the MMT would be lost.

5. Acknowledgements

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6. References

1. Gao H, Zou M, Zhong C, Zhuang J, Lin J, Lu Z, et al. Advances in pixel driving technology for micro-LED displays. Nanoscale. 2023;15:17232.

2. Luo H, Wang S, Kang J, Wang YM, Zhao J, Tsong T, et al. Complementary LTPO technology, pixel circuits and integrated gate drivers for AMOLED displays supporting variable refresh rates. Dig Tech Pap - SID Int Symp. 2020;51(1):351–4.

3. Zeumault A, Mendez JE, Brewer J. Innovations in thin-film electronics for the new generation of displays. J Soc Inf Disp. 2024;32(4):121–35.

4. Hoffman DM, Johnson P V., Kim JS, Vargas AD, Banks

MS. 240 Hz OLED technology properties that can enable improved image quality. J Soc Inf Disp. 2014;22(7):346–56.

5. Hsiang E-L, Yang Z, Yang Q, Lan Y-F, Wu S-T. Prospects and challenges of mini-LED, OLED, and micro-LED displays. J Soc Inf Disp. 2021;29(6):446–65.
6. Kim JC, Lee IS, Kim HT, An J Bin, Kim JS, Yoo JS, et al. A novel LTPO AMOLED pixel circuit and driving scheme for variable refresh rate. J Inf Disp [Internet]. 2023;24(4):283–98. Available from: https://doi.org/10.1080/15980316.2023.2213848
7. Hong YH, Jung EK, Jeong YR, Im H, Kim YS. Micro light-emitting diode pixel circuit based on p-type low-temperature polycrystalline silicon thin-film transistor for mobile displays. IEEE Trans Electron Devices. 2023;70(9):4662–8.
8. Jung EK, Hong Y-H, Hong S, Park K, Lee S-Y, Kim Y-S. A new pixel circuit based on LTPO backplane technology for micro-lLED display using PWM method. Dig Tech Pap - SID Int Symp. 2021;52(1):876–9.
9. Chang TK, Lin CW, Chang S. LTPO TFT technology for amoleds. Dig Tech Pap - SID Int Symp. 2019;50(1):545–8.
10. Bestelink E, de Sagazan O, Motte L, Schultes B, Silva SRP, Sporea RA. Versatile thin-film transistor with independent control of charge injection and transport for mixed signal and analog computation. Adv Intell Syst. 2020;3:2000199.
11. Kimura M, Nakashima A, Sagawa Y. Mechanism Analysis of Off-Leakage Current in Poly-Si TFTs with LDD Structure Mechanism Analysis of Off-Leakage Current in Poly-Si TFTs with LDD Structure. Electrochamical Solid-State Lett. 2010;13(12):H409.
12. Sporea RA, Trainor MJ, Young ND, Shannon JM, Silva SRP. Intrinsic gain in self-aligned polysilicon source-gated transistors. IEEE Trans Electron Devices. 2010;57(10):2434–9.
13. Bestelink E, Landers T, Sporea RA. Turn-off mechanisms in thin-film source-gated transistors with applications to power devices and rectification. Appl Phys Lett. 2019 May 6;114:182103.
14. Sporea RA, Trainor MJ, Young ND, Shannon JM, Silva SRP. Source-gated transistors for order-of-magnitude performance improvements in thin-film digital circuits. Sci Rep. 2014;4:4295.
15. Sporea RA, Trainor MJ, Young ND, Shannon JM, Silva SRP. Field plate optimization in low-power high-gain source-gated transistors. IEEE Trans Electron Devices. 2012;59(8):2180–6.
16. Bestelink E, Sporea RA. Multimodal Transistor-Based 7T2C LTPS Pixel Circuit for Simultaneous PAM and PWM Control in µLED Display. Dig Tech Pap - SID Int Symp. 2024;55(1):493–6.
17. Wang G, Zhuang X, Huang W, Yu J, Zhang H, Facchetti A, et al. New opportunities for high-performance source-gated transistors using unconventional materials. Adv Sci. 2021;2101473.
18. Hemmi Y, Ikeda Y, Sporea RA, Takeda Y, Tokito S, Matsui H. N-type printed organic source-gated transistors with high intrinsic gain. Nanomaterials. 2022;12:4441.
19. Zhang J, Wilson J, Auton G, Wang Y, Xu M, Xin Q, et al. Extremely high-gain source-gated transistors. Proc Natl Acad Sci U S A. 2019;116(11):4843–8.
20. Li Y, Zhou Y, Zou S, Lan L, Gong Z. Insight into the evolution of electrical properties for Schottky-barrier IGZO thin-film transistors with Cu-based Schottky contacts. Appl Phys Lett. 2023;123(10).
21. Bestelink E, Zschieschang U, Bandara R M I, Klauk H, Sporea RA. The secret ingredient for exceptional contact-controlled transistors. Adv Electron Mater. 2021;8:2101101.