Design-Technology Co-Optimization of TFT Backplane for Ultrasound Pulse-Echo Systems

Florian De Roose*, Nikolas Papadopoulos*, Yannick Baines*, Raf Appeltans*
***imec, Leuven, Belgium**

Abstract
This paper contains an analysis of an ultrasound pulse-echo system with a TFT backplane, and considers how the trade-off between resistance, capacitance and voltage tolerance can be navigated during technology development. To this end, the link budget is calculated, the losses in the backplane are quantified, the optimal device width is calculated and a contour plot with the trade-off between the performance and voltage tolerance is shown.

Author Keywords
DTCO, optimization, ultrasound, TFT, pulse-echo, arrays

1. Introduction
The use of ultrasound (US) pulse-echo systems is common in many places, from medical uses to automotive ranging. Most applications use bulk piezoelectric transducers to transmit (TX) an ultrasound pulse and receive (RX) the echo bouncing off an object. However, the transducer elements are usually individually wired to a Si readout chip, limiting the amount of transducers that can be integrated in a practical form factor. For future US array generations, different transducers are considered, like piezo-electric micromachined US transducers (PMUTs) [1,2] or capacitive micromachined US transducers (CMUTs) [1,3]. Some of these can even be integrated on flat-panel-display technology as one of the sensing modalities [4], allowing for active large areas [5]. To drive them, a thin-film transistor (TFT) technology can be used, allowing selective use of parts of the array.

The core question of this work is: what is the best TFT technology for an ultrasound pulse-echo system? There is an intrinsic trade-off in the transistor device architecture between performance and voltage tolerance. The TFT stack constrains the circuit design, which in turn determines the system performance. Starting from basic metrics of the TFT technology (R_{on}, C_{gs}), this work models the full system's circuit performance (both TX and RX), resulting in a graph showing the system's performance (iso-lines) in the technology trade-off space. To reduce the degrees of freedom for the optimization, we restrict this work to only the TFT backplane in the stack, and will assume the midplane (with low-resistance/-capacitance interconnects) and the frontplane (with the micromachined ultrasound transducers, MUT) are fixed, as shown in Figure 1. Technology developers can use this graph as a quantitative tool to compare various device design options (semiconductor material, device polarity, oxide thickness, LDD doping, channel length, ...) for the US pulse-echo application.

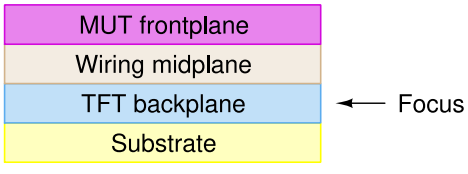

Figure 1. Stack divided in back-, mid- and frontplane

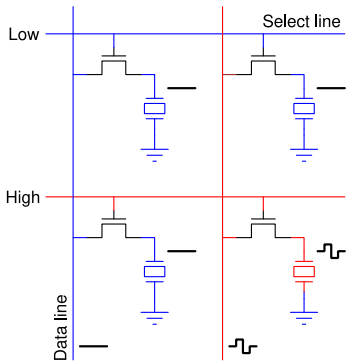

Figure 2. Simplest pixel array for US operation: a single selector switch. Only when both the column is driven (red) and the select line is activated (red), will the MUT transduce. If either the column is not driven (blue) or the row not selected (blue), there is no transduction.

2. System overview
The studied system is hybrid, consisting of a TFT selector backplane, a monolithically integrated ultrasound transducer array on top [5] and a set of standard-CMOS chips creating the high-voltage drive signal and reading back the reflections. This paper assumes the simplest conceivable setup, where the TFT backplane consists of a single selector TFT per pixel [6], but it can be expanded to more complex designs. Figure 2 demonstrates the described pixel array. Using the select lines, multiple rows of the array can be activated. During transmit only some of the columns are actively driven by the CMOS chips. During receive, similarly, only some column signals are used for data acquisition.

A simplified version of the signal flow in the array and the IC is shown in Figure 3. n pixels are connecting to the dataline through their respective pixel transistor. During transmit, a High Voltage (HV) pulser is driving the desired high-frequency pulse signal into the data lines while the receive side is disconnected by an RX/TX switch. During receive, a low-noise amplifier (LNA) – analog-to-digital converter (ADC) combination converts the echo signal generated by the transducers into a digital signal which can be postprocessed.

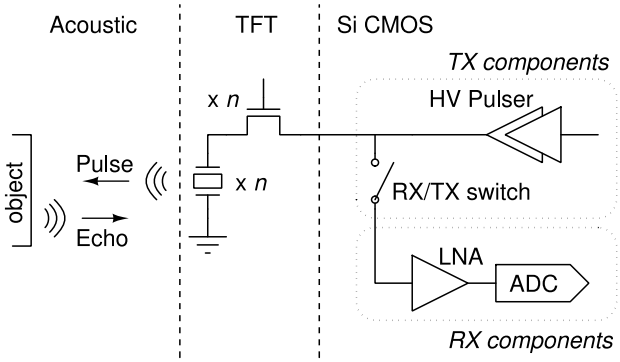

Figure 3. Signal flow in the system

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3. Link budget

The system has the highest sensitivity when the received signal has the highest signal-to-noise ratio (SNR). A link budget, accounting for all losses in every step of the time-of-flight (pulse-echo) sensing, is shown in Figure 4. The pulser creates a pulse voltage with amplitude V_{pulse}. Some of the voltage is lost in the TFT array due to parasitics, with an efficiency η_{TX}. The transducer linearly converts the voltage into an acoustic pressure by $\eta_{TX,MUT}$. The US wave then travels through the medium, reflects off interfaces, meanwhile loosing signal strength, reducing the pressure level by η_{path}. Deeper penetration will result in higher path loss. The return pressure at the receiver is converted into a voltage by $\eta_{RX,MUT}$. To make the link budget easier to understand, we consider the voltage generated by the MUT in isolation, i.e. without external load from the TFTs, array or readout. Due to the parasitic of the TFT array and wiring, this voltage is further reduced by η_{RX}. Finally, the receiver chip has a noise level of $V_{RX,n}$. The overall SNR therefore is

$$SNR = \frac{\eta_{RX}\,\eta_{RX,MUT}\,\eta_{path}\,\eta_{TX,MUT}\,\eta_{TX}\,V_{pulse}}{V_{RX,n}}$$

Since the focus is on the impact of the backplane, we can consider $\eta_{RX,MUT}$, $\eta_{TX,MUT}$ (PMUT dependent), $V_{RX,n}$ (readout IC dependent) and η_{path} (image dependent) as fixed numbers. The parameters we can optimize are η_{RX}, η_{TX} and V_{pulse}.

4. Circuit analysis

To accurately calculate the parameters η_{RX} and η_{TX}, one should simulate the circuit with all parasitic components coming from backplane, midplane and frontplane. These components depend on the exact design and layout that is used and are extracted by a post-layout parasitic extraction (PEX). However, doing so is very time intensive (both labour and computationally) and can only be done for a couple of points, with a very concrete set of assumptions on the exact technology used. We have done these simulations for a few discrete points. However, for the technology development, we want a bird's eye view on the impact of stack and device changes.

Starting from a simplified model, we can describe the system using analytical equations. The RX and TX equivalent schematics are shown in Figure 5 and 6 respectively. The dominant circuit components are the parasitics of the wire (R_{wire}, C_{wire}), the parasitics of the TFT (R_{TFT}, C_{TFT}) and the parasitic capacitance of the MUT (C_{MUT}). When focusing on the backplane, only the TFT parasitics are variables, and the rest is fixed by the midplane design (R_{wire}, C_{wire}) and the MUT design (C_{MUT}).

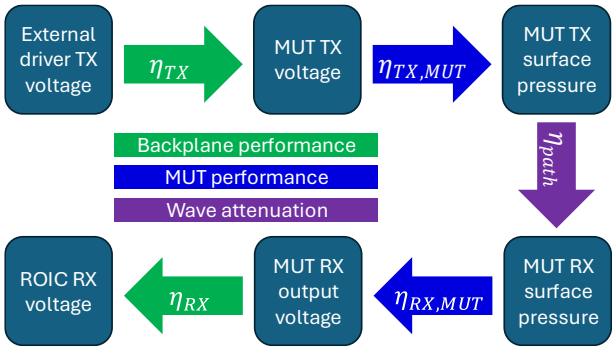

Figure 4. Link budget in the pulse-echo readout chain

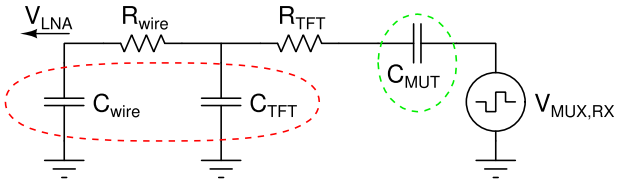

Figure 5. Equivalent circuit in receive

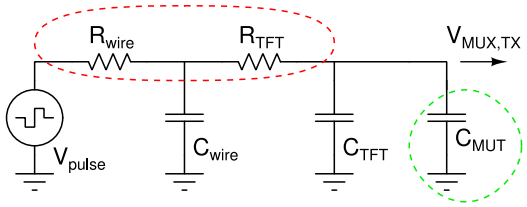

Figure 6. Equivalent circuit in transmit

In this analysis, there is one key assumption: the losses are limited, i.e. η_{RX} and η_{TX} are rather high. This is a reasonable assumption to make if the system performance has to compete with arrays without TFTs: low values of η_{RX} and η_{TX} will ruin the overall performance.

In receive, the model can be further simplified to a pure capacitive divider if the R_{TFT} and R_{wire} can be ignored, as justified later. The receive efficiency is then:

$$\eta_{RX} = \frac{C_{MUT}}{C_{MUT} + C_{TFT} + C_{wire}} \quad (1)$$

This is only dependent on the transistor capacitance C_{TFT}, and not on R_{TFT}. To minimize loss in the RX path, i.e. maximize η_{RX}, the capacitance of TFT and wiring should be much smaller than the capacitance of the MUT, i.e. $C_{MUT} \gg C_{TFT} + C_{wire}$. The veracity of this assumption depends on the exact properties of midplane and frontplane and should be verified on a case-by-case basis.

In transmit, the dominant cause of losses is RC delay. With a time constant τ_{TX}, the signal attenuation at given pulse frequency f is

$$\eta_{TX} = 1/\sqrt{1 + (2\pi f \tau_{TX})^2} \quad (2)$$

According to Elmore's law, we calculate τ_{TX} as

$$\tau_{TX} = R_{wire}C_{wire} + (R_{wire} + R_{TFT})(C_{TFT} + C_{MUT})$$

If we assume that $C_{MUT} \gg C_{TFT}, C_{wire}$ from the requirements in the RX path, we can ignore those terms, simplifying to

$$\tau_{TX} = (R_{wire} + R_{TFT})C_{MUT}$$

This expression only depends on one TFT parameter: R_{TFT}.

Let us return to the initial assumption of negligible resistance in the RX analysis. The time constant for RX according to Elmore's law is

$$\tau_{RX} = (R_{wire} + R_{TFT})C_{wire} + R_{TFT}C_{TFT}$$

If we minimize the loss in the TX path, η_{TX} is close unity, i.e. $\tau_{TX} \ll 1/2\pi f$. If C_{MUT} is much larger than C_{TFT} and C_{wire}, then the RX time constant τ_{RX} is even smaller than τ_{TX}, and the corresponding loss even lower, to the point where it is negligible.

To verify that C_{TFT} (R_{TFT}) does indeed not impact η_{TX} (η_{RX}) in simulations, one can extract the sensitivity S_p^{η} [7]: the relative change in efficiency η caused by a relative change in TFT properties X_{TFT}:

$$S^{\eta}_{X_{TFT}} = \left(\partial\eta/\eta\right)/\left(\partial X_{TFT}/X_{TFT}\right)$$

A large sensitivity means the parameter has a big impact on the efficiency. The manual PEX simulations show numerically that the sensitivity of receive efficiency to changes in R_{TFT} ($S^{\eta_{RX}}_{R_{TFT}}$) is 44x smaller than the sensitivity to C_{TFT} ($S^{\eta_{RX}}_{C_{TFT}}$). Meanwhile for transmit the sensitivity to C_{TFT} ($S^{\eta_{TX}}_{C_{TFT}}$) is 16x smaller than to R_{TFT} ($S^{\eta_{TX}}_{R_{TFT}}$), demonstrating the validity of the model presented above.

In conclusion, we have an expression for $\eta_{RX} = f(C_{TFT})$ and $\eta_{TX} = f(R_{TFT})$, allowing a full decoupling of both parameters. In receive, the loss is caused by the parasitic capacitance, while in transmit the loss is caused by the RC drop over the parasitic resistors.

5. Circuit behavioural modelling

The critical TFT properties are R_{TFT} and C_{TFT}, as shown from the circuit analysis. Because most technology optimizations start from a known reference technology, we compare the R_{TFT} and C_{TFT} to the values in that reference technology and design, and work with the multipliers $\zeta_R = R_{TFT}/R_{TFT,ref}$ and $\zeta_C = C_{TFT}/C_{TFT,ref}$. ζ_R and ζ_C are dimensionless numbers. Figure 7 shows the manually extracted performance parameters η_{RX} and η_{TX} for different changes to our reference technology.

Based on the expected relation between η_{TX} and ζ_R from eq. (1), it is possible to extract a closely-fitting analytic formula for the post-PEX simulation data, as shown in Figure 7:

$$\eta_{TX} = \frac{1}{\sqrt{1 + 0.0324 \times (2.4 + \zeta_R)^2}} \quad (3)$$

Similarly, for η_{RX} and ζ_C based on eq. (2), the relationship is:

$$\eta_{RX} = \frac{0.930}{1 + 0.147 \times \zeta_C} \quad (4)$$

Notice however that even with a given technology/device architecture, ζ_R and ζ_C depend on the W of the transistor. A wider transistor has lower resistance, i.e. $\zeta_R \propto 1/W$, while it also has a higher capacitance, i.e. $\zeta_C \propto W$. The multiplication of the two however is design-invariant, i.e. it is only depending on the device / technology. We propose to call the derivative device parameter $\zeta_{TFT} = \zeta_R\zeta_C$. Consequently, a transistor technology with lower parasitics has a lower ζ_{TFT} factor. Figure 8 shows the trade-off between ζ_R and ζ_C. On the X-axis, ζ_R is plotted, on the Y-axis, the ζ_C is shown. For a given technology, ζ_{TFT} is constant, therefore only a subset of points on a single hyperbola in this space are reachable by changing W as indicated by the dashed lines. The hyperbola shifts if the device improves (light blue hyperbola) or worsens (dark blue hyperbola). Notice that for the curve with $\zeta_{TFT} = 1$, the hyperbola passes through the $\zeta_R, \zeta_C = 1$ point.

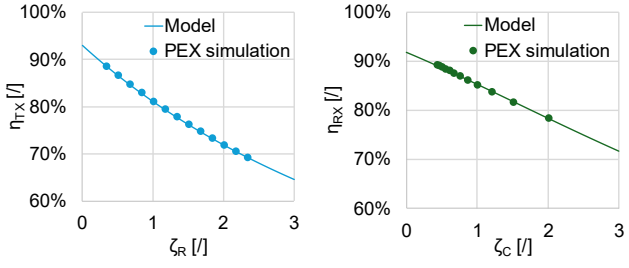

Figure 7. Datapoints for η_{TX} and η_{RX} extracted from a PEX simulation, as well as the fitted analytical equations

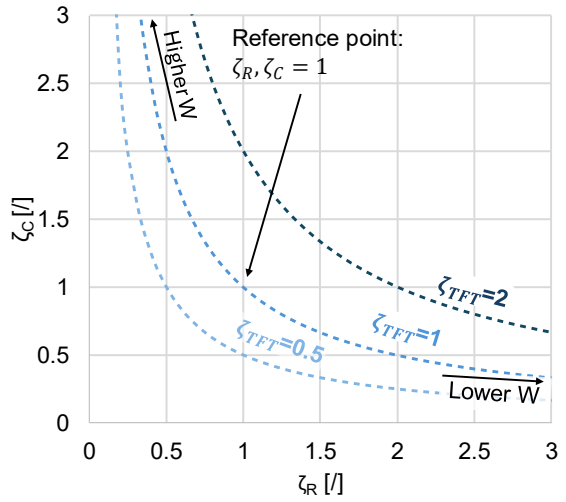

Figure 8. Trade-off between TFT resistance and capacitance by changing W

6. TFT width optimization

The combination of transmit and receive efficiency is described by the performance $H = \eta_{TX}\eta_{RX}$. The goal of the width optimization is to find the best size device to balance the resistance and capacitance. Figure 9 expands on Figure 8 to also shows iso-performance points based on the analytic model for η_{RX} and η_{TX}. These lines, which appear linear at first glance, connect all points with the same performance H. Moving towards the bottom left corner will result in a higher H. The optimum W for highest performance can now be found by selecting the point on the hyperbola which touches the highest iso-H line. For the design with the reference transistor, the performance is 68.1%. The optimal W selection for this technology however, is $W = 0.67 \times W_{ref}$, improving the performance H to 69.6%.

7. Optimal technology trade-off

Finding this optimum value for W, we can find the best possible performance H for a given TFT technology, as marked by the ζ_{TFT}. The resulting graph is shown in Figure 10. As the technology gets better, a lower loss can be achieved.

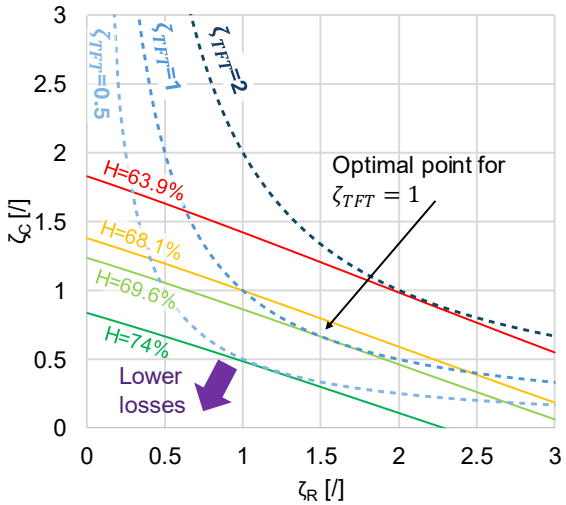

Figure 9. Performance optimization with a fixed technology by changing W

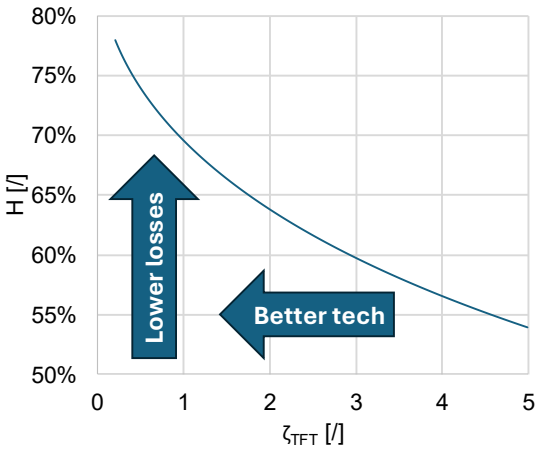

Figure 10. Best possible performance $\boldsymbol{H}$ depending on the transistor performance $\boldsymbol{\zeta_{TFT}}$

The transmit and receive efficiency η_{TX} and η_{RX} are not the only components of the ultrasound backplane performance though. Driving the MUTs in TX with higher voltages V_{pulse} also drives up the SNR of the system. The "backplane equivalent voltage" V_{BP} is the more accurate metric for optimizing the backplane, since it combines both: $V_{BP} = \eta_{TX}\eta_{RX}V_{pulse} = H \times V_{pulse}$. Since voltage tolerance and ζ_{TFT} depend on many technological parameters, the best way to represent the real performance is by plotting iso-V_{BP} lines on the plane with V_{pulse} vs ζ_{TFT}. The resulting graph can be seen in Figure 11. Each line marks all points with the same V_{BP}, as shown on the graph.

As an example of how this graph can be used, consider three imaginary scenarios. First a reference scenario with a technology which tolerates $V_{pulse} = 30V$ and transistor performance $\zeta_{TFT} = 1$. The position is indicated on the figure, it shows that $V_{BP} \approx 20.5V$. For scenario 2, imagine we update the technology, e.g. by making the gate oxide thin. The device is now twice as performant ($\zeta_{TFT} = 1/2$), but the voltage tolerance decreases by 5V. From the graph we can see that the $V_{BP} \approx 18V$. Even though the TFT performance is much better, the system as a whole is worse. Finally, in scenario 3, we imagine adding a LDD region which increases resistance by a factor 4 ($\zeta_{TFT} = 4$). However, thanks to this LDD we can increase the V_{pulse} to 40V. In this case $V_{BP} = 22.5V$, a non-negligible improvement over the reference case. For the numbers used in this calculation, it can be observed that creating a high-voltage transistor is more important for system performance than improving the RC product of the device.

The methodology shown here can be further extended to include extra boundary conditions and compare different circuit topologies. Generally speaking, the graph can be recreated for any application trading these two parameters, and technologists can use this graph to compare and contrast the different technology and device options they have.

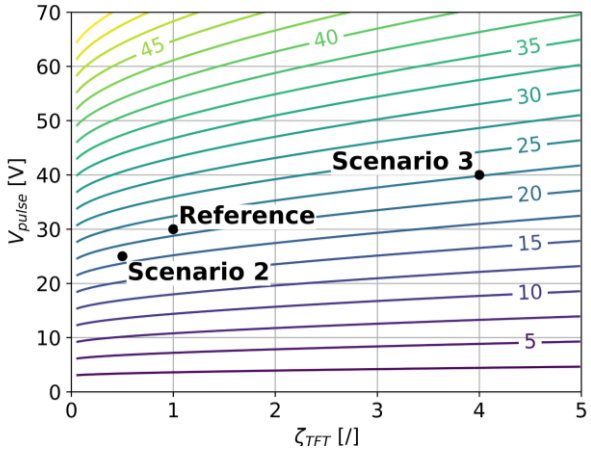

Figure 11. Contour plot of iso-performing $\boldsymbol{V_{BP}}$ lines. This graph allows to compare different variations of technology to each other.

8. Conclusion

In this paper we have presented a method for analysing the performance of a backplane TFT technology for use in a pulse-echo US system. We show TX efficiency only depends on the TFT resistance, and RX efficiency only depends on TFT capacitance. We provide technologists a map to navigate the trade-off between transistor parasitics and voltage tolerance from which the importance of voltage tolerance can clearly observed. The map enables the right technology development for future applications in the field.

9. References

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