A Compact Fully a-Si:H TFT-Based Active Pixel Sensor Circuit for High-Resolution Low-Dose Medical Imaging

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Abstract

In this paper, we proposed a compact fully a-Si:H thin-film transistor (TFT)-based active pixel sensor (APS) circuit using photo-TFT (PT) as sensor device, which is compatible with existing display panel fabrication process. By multiplexing PT and removing readout TFT, this circuit achieves a compact structure with 75-μm pixel pitch and a high charge gain of 34.7, enabling it suitable for high-resolution and low-dose medical imaging.

Author Keywords

Active pixel sensor (APS), hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs), photo-TFT, low-dose medical imaging

1. Introduction

Over the past two decades, TFT-based X-ray imagers have been widely used in the medical field. With the development of flat panel display (FPD), large-scale integration of a-Si:H TFTs arrays on substrates has become a mature technology. Therefore, a-Si:H TFT panels have also become the mainstream choice for large-area flat panel digital imaging due to their low manufacturing cost and good large-area uniformity [1]. Presently, photodiode (PD)-based pixel sensors are commonly used in flat panel imaging [2]-[4]. However, the incompatibility between the switching TFT and PD fabrication processes leads to low yield and high fabrication costs [5].

Recent studies have investigated the use of PTs as sensors due to their compatibility with existing TFT fabrication process, which significantly simplifies manufacturing and improves yield rates [6], [7]. However, PTs operating in conventional negative-biased mode face challenges such as low photoresponsivity (R) （~0.1A/W） and high leakage current, making it difficult to detect weak-light (~1nW/cm²). Additionally, previously reported PTs are commonly integrated into passive pixel sensor (PPS) circuits, which have a low charge gain (≤1), making it challenging to achieve a satisfactory signal-to-noise ratio (SNR) under low-dosage [8]. Furthermore, due to the slow line-by-line charge-transfer readout operations, the conventional PT-TFT based image sensor is not suitable for real-time medical imaging applications [9]. Emerging applications such as breast tomosynthesis require multiple images from different angles for 3D reconstruction, which means that the time and exposure dose per frame must be reduced. Therefore, it is required that the imager can maintain high imaging quality even under high frame rate and low dose exposure [10].

In this paper, we propose a compact 2T-1C APS circuit with 75μm pixel pitch based on PT. By setting the PT in diode-connected mode during the exposure phase, we significantly enhance its photoresponsivity and reduce its leakage current. The proposed circuit suits low-dose detection due to the weak-light detection capability of diode-connected PT and the noise suppression and signal amplification capability of APS circuit structure. The following section will provide a detailed discussion on the circuit design, including transient response simulations and layout design based on the electrical and photo-response characteristics of the switching TFT and PT.

2. The Proposed 2T-1C PT-Based Pixel Sensor

Fig. 1(a) shows the schematic of the proposed pixel sensor. All scan signals are shared by each row of pixels, and sensing lines are shared by entire columns of pixels. The external readout chip is a charge integrator. Each pixel circuit consists of a PT, an amplifier TFT T_{AMP}, and a storage capacitor C_{PIX}. Its working scheme can be divided into three phases, as shown in Fig. 1(b).

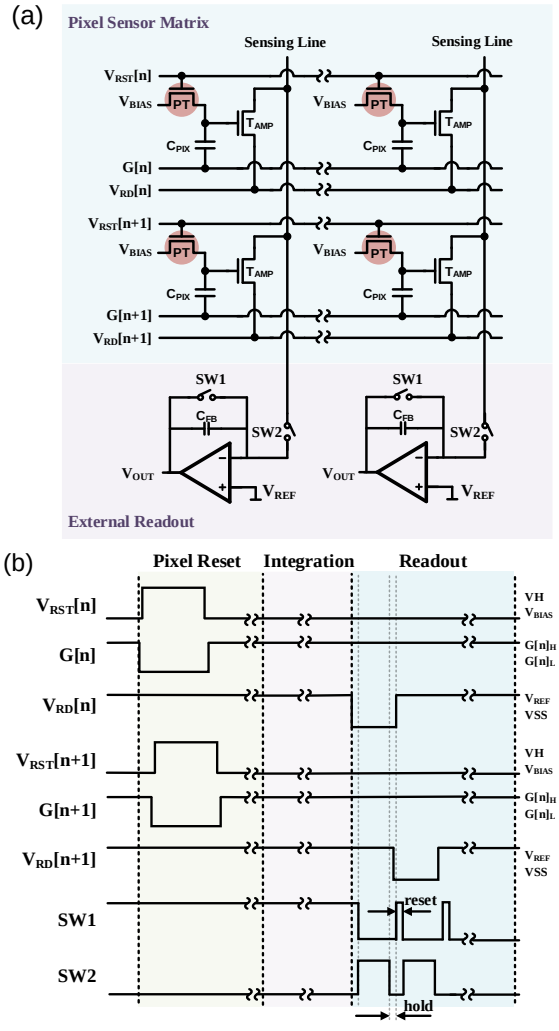

Figure 1. (a) Schematic and (b) timing diagram of the proposed pixel sensor

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(1) Pixel Reset:

In order to avoid generating huge current on the power line during the reset phase, we chose to do a progressive reset instead of a global reset. At the beginning, G[n] couples the gate voltage of TAMP to a low level, followed by V_{RST}[n] rises to turn on the PT as a switching TFT, initializing the gate voltage of TAMP to V_{BIAS}. At the end of pixel reset phase, V_{RST}[n] drop to V_{BIAS} to make the gate voltage of the PT equal to its drain voltage, and the gate voltage of TAMP (expressed by $V_{GATE\_APM\_1}$) is lifted by G[n] due to charge conservation. Ultimately, it becomes:

$$V_{GATE\_APM\_1} = V_{BIAS} + \frac{C_{PIX}}{C_{TOTAL}}(G[n]_H - G[n]_L) \quad (1)$$

$$C_{TOTAL} = C_{PIX} + C_{GS\_PT} + C_{GS\_AMP} + C_{GD\_AMP} \quad (2)$$

C_{GS_PT}, C_{GS_AMP}, C_{GD_AMP} refers to the parasitic capacitance of PT, the gate-source parasitic capacitance of TAMP, and the gate-drain parasitic capacitance of TAMP, respectively.

(2) Integration:

During the exposure and integration phase, the PT works in diode-connected mode and can be equivalently treated as a reverse-biased photodiode ($V_S > V_G = V_D$), so the photocurrent is independent of V_{DS}. The photocurrent flowing out from CPIX and the gate voltage of TAMP continues to decrease. The gate voltage of TAMP at the end of the integration phase is $V_{GATE\_APM\_2}$, it can by expressed as:

$$V_{GATE\_APM\_2} = V_{GATE\_APM\_1} - \frac{Q_{IN}}{C_{TOTAL}}$$

$$= V_{BIAS} + \frac{C_{PIX}}{C_{TOTAL}}(G[n]_H - G[n]_L) - \frac{Q_{IN}}{C_{TOTAL}} \quad (3)$$

During integration period, there exists a correspondence between the photogenerated current and the intensity of illumination, thus the information of illumination intensity is stored on CPIX.

(3) Readout:

During the row-by-row readout phase, the V_{RD}[n] signal drops from V_{REF} to V_{SS}, increasing the V_{GS} of TAMP and generating a readout current I_{OUT}. Due to the presence of the gate-source overlap capacitance CGS of TAMP, the gate voltage is coupled down to V_{GATE_APM3} :

$$V_{GATE\_APM\_3} = V_{GATE\_APM\_2} - \frac{C_{GS\_AMP}}{C_{TOTAL}}(V_{REF} - V_{SS}) \quad (4)$$

The readout current can be expressed as:

$$I_{OUT} = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GATE\_APM\_3} - V_{SS} - V_{TH})^2 \quad (5)$$

V_{TH} represents the threshold voltage of TAMP. Due to the presence of parasitic resistance-capacitance (RC) on the scan lines, the time for the V_{RD}[n] signal to reach pixels in different columns is inconsistent. To overcome this issue, only when SW2 is turns on will I_{OUT} be read out, ensuring the gain uniformity on panel. When SW2 turns off, a hold time of about 1μs is reserved for the analog-to-digital converter (ADC) to sample. After the reset of charge integrator, data from next row of pixels is ready to be read.

3. Results and Discussions

3.1. Characteristics of Devices

The cross-sectional structure diagram of a-Si:H TFTs is shown in Fig. 2. The process adopts the mature back-channel etch (BCE) technology currently used in liquid crystal display (LCD) production lines [15]-[17].

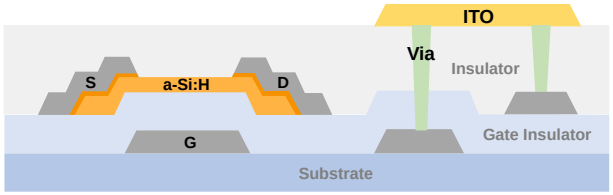

Figure 2. Cross-sectional structure diagram of a-Si:H TFT

The transfer characteristics of the a-Si:H TFT with channel width and length ratio (W/L) of 6μm/3μm are shown in Fig.3. Based on measured data, we have extracted the TFT model for SPICE simulations [18], [19]. The extracted model has a threshold voltage (V_{TH}) of 4.24V and a carrier mobility of 0.41 cm²/(V·s).

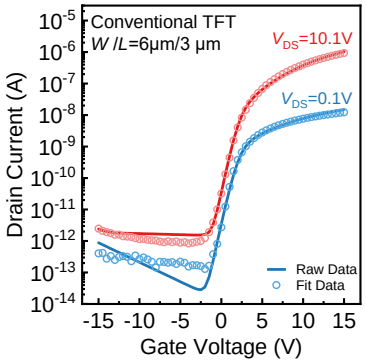

Figure 3. Comparision of the measured and simulated current-voltage transfer curve of a-Si:H TFT samples.

To minimize dark current while maintaining sufficient responsivity, the channel length (L) of the PT used in this circuit is set to 5μm, and a diode-connected structure is used by setting the gate voltage equal to the drain voltage (V_{BIAS}) during exposure. The photo-response characteristics of diode-connected PT under different power intensity (P) of light is shown in Fig.4. Compared to conventional negative-biased PTs, diode-connected PTs exhibit lower leakage current (<1fA/μm), higher responsivity (8~100A/W), and the ability to detect weaker light intensities (~1nW/cm²). These advantages enable the designed pixel circuit to achieve a higher SNR and a more compact structure.

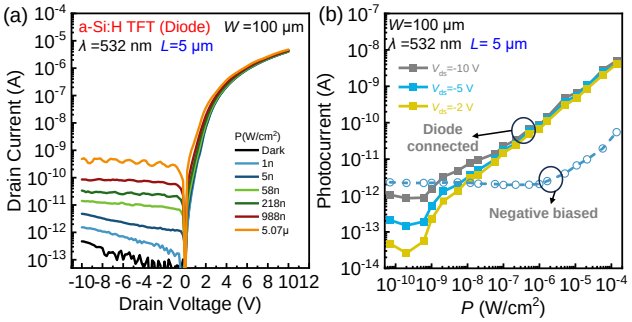

Figure 4. (a) Transfer curve of PT with different Illuminations, and (b) relationship between photocurrent and illumination power

3.2. Transient Response

The basic functionality of the circuit has been verified through simulations. The gate voltage of TAMP and the output voltage of the charge integrator V_{OUT} are shown in Fig. 5. It can be observed that different input charge quantities cause corresponding changes in

the gate voltage of T_{AMP}. During the readout phase, SW1 turns off and SW2 turns on, resulting in an increase in V_{OUT}. After the readout phase, SW2 turns off, and V_{OUT} remains constant. An external ADC performs sampling during this period.

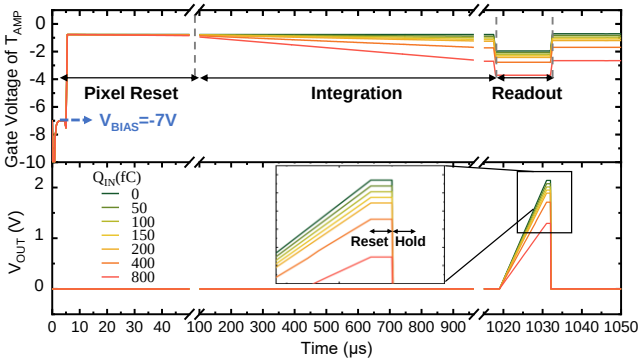

Figure 5. Transient response of proposed APS circuit

Table 1. Parameters of the proposed active pixel sensor

Parameters	Value	Parameters	Value
V_{RST}[n]	-7V~12V	C_{PIX}	0.4pF
G[n]	-7V~0V	C_{FB}	30pF
V_{RD}[n]	-12V~0V	t_{PIXEL_RESET}	4μs
V_{BIAS}	-7V	t_{INT}	1ms
V_{REF}	0V	t_{READ}	12μs
W/L of PT	50μm / 5μm	t_{HOLD}	1μs
W/L of T_{AMP}	144μm / 3μm	t_{RESET}	1μs

3.3 Noise Analysis

The noise sources of an APS circuit mainly include pre-amplification noise $\sigma_{\text{pre-amp}}$ in the front stage and post-amplification noise $\sigma_{\text{post-amp}}$. $\sigma_{\text{pre-amp}}$ consists of three non-correlated noise components: the dark current noise of the PT σ_{sensor}, the reset noise σ_{reset}, and the leakage current noise of TFT $\sigma_{\text{TFT-OFF}}$. Under the parameter setting as indicated in Table 1, $\sigma_{pre-amp}$can be estimated using the following formula:

$$\sigma_{pre-amp} = \sqrt{{\sigma_{sensor}}^2 + {\sigma_{TFT-OFF}}^2 + {\sigma_{reset}}^2} \quad (3.1)$$

$$= \sqrt{\frac{I_{dark} * t_{frame}}{q} + \frac{I_{off} * t_{frame}}{q} + \left(\frac{\sqrt{kTC_{PIX}}}{q}\right)^2}$$

$$= 412e^-$$

Where I_{dark} is the dark current of PT(<1fA/μm), I_{off} refer to the TFT leakage current (the typical value is $10^{-12}A$ for a-Si TFT), and t_{frame} is the frame time(16.17ms for 60fps). The estimated noise of the external readout circuit is [12]:

$$\sigma_{post-amp} = \sqrt{{\sigma_{flicker}}^2 + {\sigma_{thermal}}^2 + {\sigma_{amp}}^2} = 1750e^- \quad (3.2)$$

The $\sigma_{flicker}$ and $\sigma_{thermal}$ refer to flicker noise and thermal noise of TFTs, respectively. The external readout circuit noise σ_{amp} is mainly generated by the switched-capacitor amplifier. So we can get the total noise:

$$\sigma_{total} = \sqrt{{\sigma_{pre-amp}}^2 + \frac{{\sigma_{post-amp}}^2}{G}} = 508e^- \quad (3.3)$$

Where G represents the charge gain of the circuit. Under a low-dose exposure of 200fC, the proposed APS circuit can achieve a high SNR of 67.8dB. We obtained the input signal level that saturates the pixel capacitance through simulation. The Q_{MAX} is 2.625 pC, from which we can derive that the dynamic range of this pixel circuit is 90.2dB.

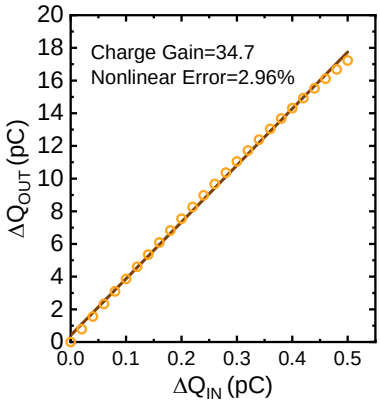

Figure 6. Relationship between the input charges and the output charges

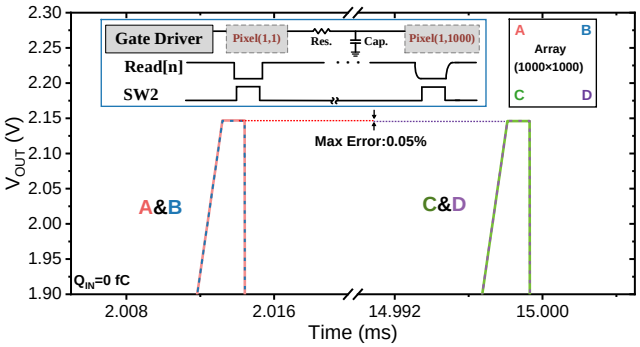

Figure 7. Output voltage of pixels at four corners without illumination

Since the readout signal of this circuit is located at the source of the amplifying TFT T_{AMP}, RC delay may lead to differences in the readout currents among pixels in different columns, as shown in fig. 7. The load on the V_{RD}[n] signal line mainly includes parasitic resistance and capacitance of the metal lines, as well as the gate-source parasitic capacitance of T_{AMP} within all pixels. The estimated load on the V_{RD}[n] line is 4 KΩ and 75 pF. As previously mentioned, to address this issue, SW2 is used to control the readout current, ensuring uniformity across the entire panel. Fig. 7 shows the readout signal error for pixels located at the four corners at $Q_{in} = 0fC$, which is mainly caused by the leakage current of PT and the delay of the readout signal. The V_{OUT} error between Pixel(1,1) and Pixel(1000,1000) is 1.1mV, with an error rate of 0.05%, indicating that the proposed method can guarantee uniformity among different columns.

3.4 Layout Design

The layout design of the proposed pixel circuit is shown in Fig. 8. Due to the reuse of PTFT and the removal of the readout TFT, this circuit achieves a pixel pitch of 75μm, which means it can achieve a resolution comparable to PPS. At this size, the storage capacitance in pixel is 0.4pF. Table 2 presents a comparison of this work with other previous schemes.

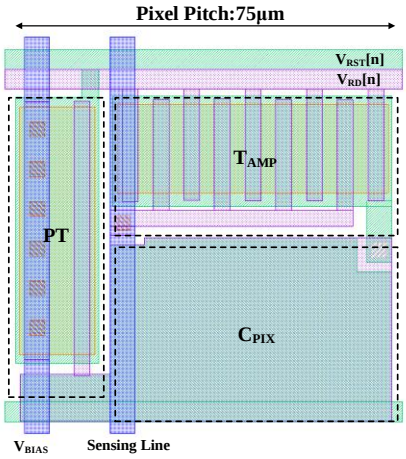

Figure 8. Layout of proposed active pixel sensor

Table 2. Comparison among previous works and this work

Ref.	[11]	[12]	[13]	[14]	This Work
TFT	a-Si:H	a-Si:H	IGZO	a-Si:H	**a-Si:H**
Sensor	a-Se	PD	OPD	a-Se	**PT**
Readout type	APS	APS	APS	PPS	**APS**
Resolution	1K*1K	1K*1K	3K*3K	N/A	**1K*1K**
Pixel Pitch(μm)	100	250	75	125	**75**
Frame Rate(Hz)	30	30	~7	N/A	**60**
Charge Gain	4	13.3	69	1	**34.7**
DR(dB)	N/A	N/A	83	60	**90.2**

4. Conclusions

This paper proposes a compact fully-TFT-based APS circuit that rivals the high resolution of PPS pixel circuits while offering a significantly higher gain and SNR. Simulation results show that the circuit achieves a charge gain of 34.7, a high frame rate of 60 Hz, and an SNR of 67.8 dB under a low-dose exposure of 200 fC. By incorporating the design of SW2, variations between channels are considerably reduced. The research results demonstrate its potential for application in low-cost, low-dose and high-resolution medical imaging.

5. Acknowledgements

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